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AN205334

F²MC-8FX Family, MB95200H/210H Series Clock Supervisor Counter

This Application note describes the functions and operations of Clock Supervisor Counter.

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1 Introduction

This application note describes the functions and operations of Clock Supervisor Counter.

Chapter 2 explains the overview of the Clock Supervisor Counter and composing.

Chapter 3 explains how to set up registers of the Clock Supervisor Counter.

Chapter 4 explains operations of the Clock Supervisor Counter.

The last chapter explains precautions on using the Clock Supervisor Counter.

2 Functions of Clock Supervisor Counter

This chapter introduces Clock Supervisor Counter.

2.1 Overview of Clock Supervisor Counter

The clock supervisor counter can check the external clock frequency to detect the abnormal state of the external clock.

The clock supervisor counter enables and disables the operation based on one of the eight different Timebase timer intervals, and counts up the counter based on the external clock input.

The count clock of this module can be selected from the main oscillation clock and the sub-oscillation clock.

2.2 Key Features

The Clock Supervisor Counter consists of the following blocks:

- Control Circuit

This block controls the start and stop of the counter, counter clock source, and the counter enable period based on the settings of the Clock Monitoring Control Register (CMCR).

- Clock Monitoring Control Register(CMCR)

The register is used to select the counter source clock, select the counter enable period from the eight different Timebase timer intervals, start the counter check whether counter is running or not.

- Clock Monitoring Data Register(CMDR)

This register block is used to read the count value after the counter stop. The software can judge the external clock frequency is correct or not according to the contents of this register.

- Timebase Timer Output Selector

This block is used to select the counter enable period from eight different timebase timer intervals.

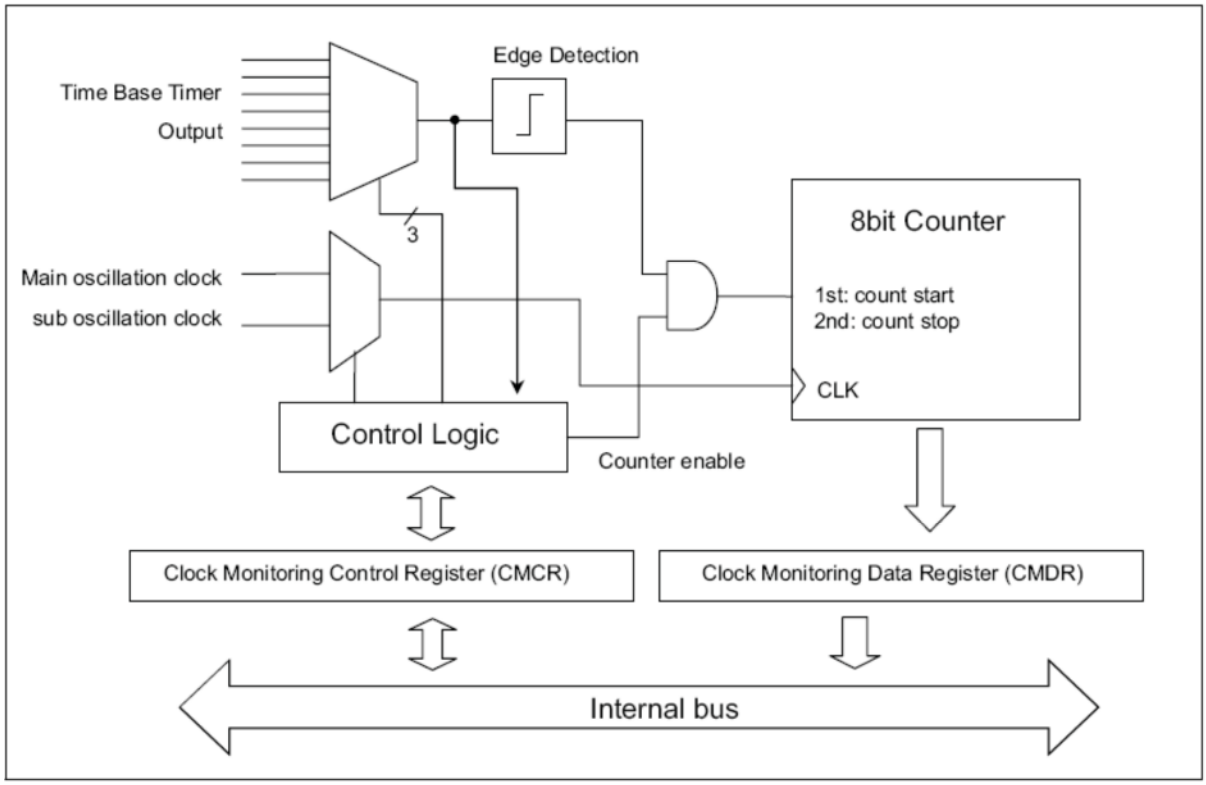
- Counter source clock selector

This block is used to select the counter source clock from the main oscillation clock or the sub oscillation clock.

2.3 Block Diagram of Clock Supervisor Counter

The follows is the block diagram of the Clock Supervisor Counter.

Figure 1. Block Diagram of Clock Supervisor Counter



The control Logic module selects the main oscillation clock or the sub oscillation clock as an 8-bit Counter CLK, and selects one from the eight different Timebase Timer output as the 8-bit Counter start/stop trigger. After the counter is enabled, the counter starts counting when the first valid edge detection, and stops counting when the second valid edge detection, then store the count value to the Clock Monitoring Data Register.

2.4 Registers of Clock Supervisor Counter

This section explains how to set up registers of the Clock Supervisor Counter.

- Clock Monitoring Data Register (CMDR)

Figure 2. Clock Monitoring Data Register

Bit #	7	6	5	4	3	2	1	0
OFEAH	CMDR7	CMDR6	CMDR5	CMDR4	CMDR3	CMDR2	CMDR1	CMDR0
Read/Write	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX
Initial Value	0	0	0	0	0	0	0	0

- Functions of Bits in Clock Monitoring Data register (CMDR)

Table 1. Functions of Bits in Clock Monitoring Data Register

Bit name		Function
bit7-bit0	CMDR7-CMDR0	The CMDR register is a data register indicating the clock supervisor counter value after the counter stops. This register is cleared if one of the following events occurs: Reset The CMCEN bit is modified from "0" to "1" by the software. The CMCEN bit is modified from "1" to "0" by the software while the counter is running. After the external clock stops, the falling edge of the selected timebase timer clock is detected twice (See Figure 19.5-2 Clock Supervisor Counter Operation 2).

Note: This register is always "0" when counter is running (CMCEN="1").

- Clock Monitoring Control register (CMCR)

The Clock Monitoring Control register (CMCR) selects the counter source clock and Time Base Timer output as counter enable period, starts counter and checks whether counter is running or not.

Figure 3. Clock Monitoring Control Register

Bit #	7	6	5	4	3	2	1	0
OFE9H	-	-	Reserved	CMCSEL	TBTSEL2	TBTSEL1	TBTSEL0	CMCEN
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	-	-	0	0	0	0	0	0

R/W : Readable/writeable (Read value is the same as write value)

R/WX : Read only (Readable, writing has no effect on operation)

R0/WX : Undefined bit (Read value is “0”, writing has no effect on operation)

R1/WX : Undefined bit (Read value is “1”, writing has no effect on operation)

R0/W : Write only (Writable, “0” is read)

- Functions of Bits in Clock Monitoring Control register (CMCR)

Table 2. Functions of Bit in Clock Monitoring Control Register

<table>
<tr><th colspan="2">Bit name</th><th>Function</th></tr>
<tr><td>bit5</td><td>Reserved bit</td><td>This bit is reserved.
Write "0" to this bit. The read value is always "0".</td></tr>
<tr><td>bit4</td><td>CMCSEL</td><td>This bit selects the counter clock source.
Writing "0":selects the external the main oscillation clock as the source clock of the counter.
Writing "1":selects the external the sub-oscillation clock as the source clock of the counter.</td></tr>
<tr><td>bit3-1</td><td>TBTSEL2-0</td><td>These bits select the timebase timer interval.
The operation of the clock supervisor counter is enabled and disabled according to the timebase timer counter output selected by these bits.
The first rising edge of the interval selected enables the counter operation and the second rising edge of the same output disables the counter operation.
<table>
<tr><th>TCTSEL2</th><th>TBTSEL1</th><th>TBTSEL0</th><th>Interval Time</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>2^3 × 1/FCRH</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2^5 × 1/FCRH</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2^7 × 1/FCRH</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>2^9 × 1/FCRH</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>2^{11} × 1/FCRH</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>2^{13} × 1/FCRH</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>2^{15} × 1/FCRH</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2^{17} × 1/FCRH</td></tr>
</table>
</td></tr>
<tr><td>bit0</td><td>CMCEN</td><td>This bit enables and disables the clock supervisor counter.
Writing "0": stops the counter and clears the CMDR register.
Writing "1": enables the counter. The counter starts counting when detecting the rising edge of the timebase timer interval.
It stops counting when detecting the second rising edge of the same interval.
This bit is automatically set to "0" when the counter stops.</td></tr>
</table>

Notes:

- Do not modify the CMCSEL bit when CMCEN = 1.
- Do not modify the TBTSEL2-0 bit when CMCEN=1.

3 Operations of Clock Supervisor Counter

This chapter explains operations of the clock supervisor counter.

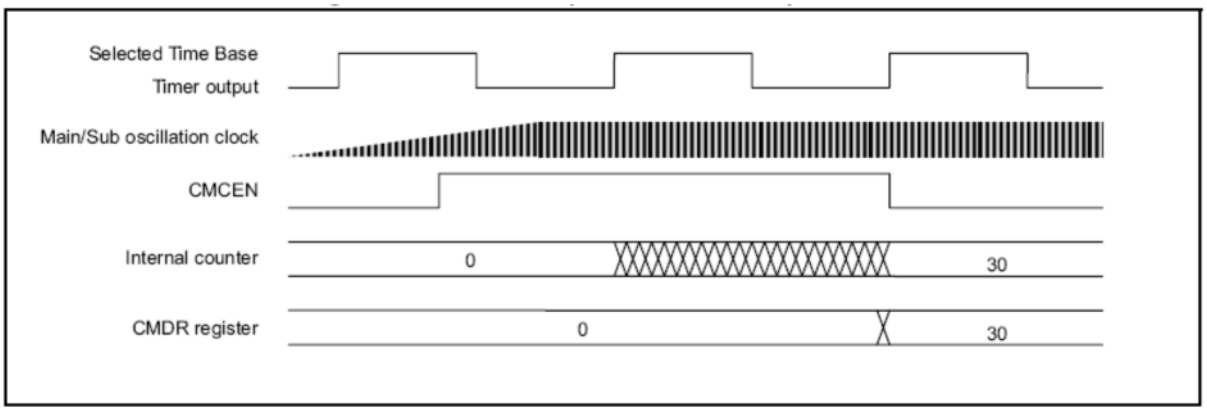
3.1 Clock Supervisor Counter Work Status in Different Condition

- Clock Supervisor Counter Operation 1

The clock supervisor counter is first enabled by the software (CMCEN = 1), and then the clock supervisor counter operates with the timebase timer interval selected from eight options by the TBTSEL [2:0] bits. Between two rising edges of the timebase timer interval selected, the internal counter is clocked by the external clock.

The count clock of this module can be selected from the main oscillation clock and the sub oscillation clock.

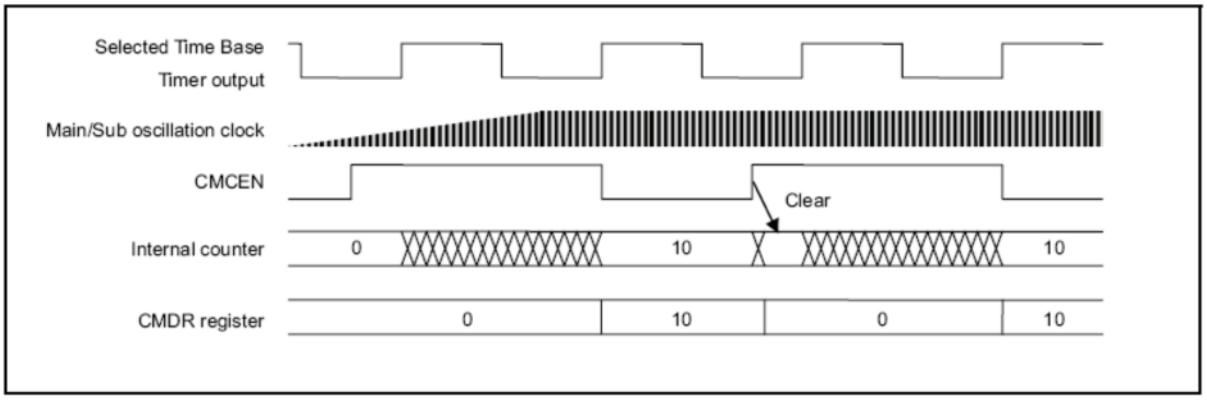
Figure 4. Clock Supervisor Counter Operation-1



- Clock Supervisor Counter Operation 2

The CMDR register is cleared when the CMCEN register changes from "0" to "1".

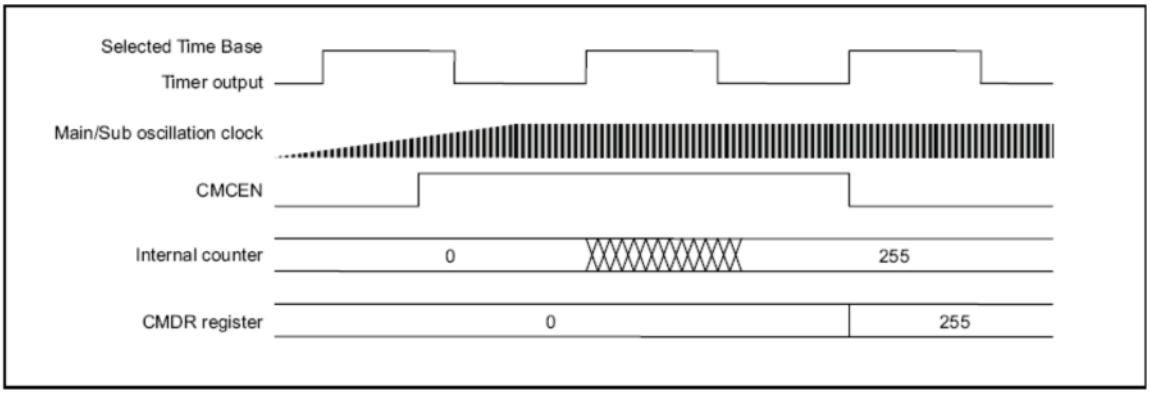
Figure 5. Clock Supervisor Counter Operation-2



- Clock Supervisor Counter Operation 3

The counter stops counting if it reaches "255". It cannot count further.

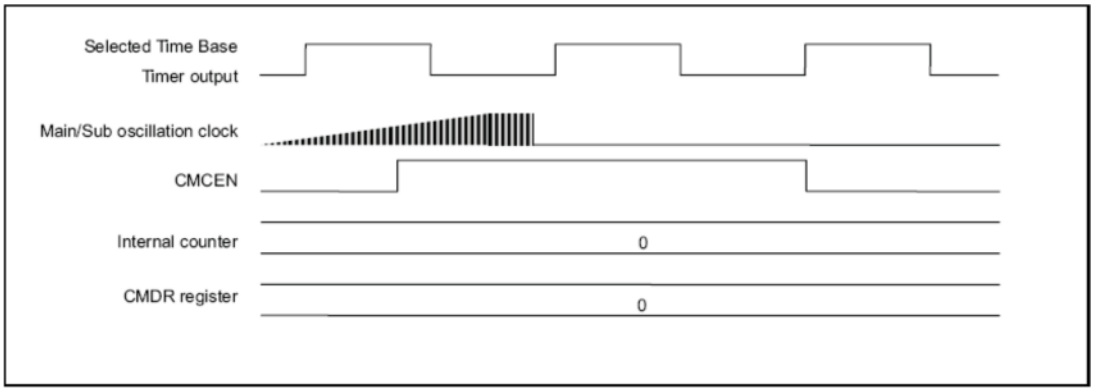
Figure 6. Clock Supervisor Counter Operation-3



- Clock Supervisor Counter Operation 4

If the external clock selected stops, the counter stops operating. The software can then identify that the external clock selected is in the abnormal state.

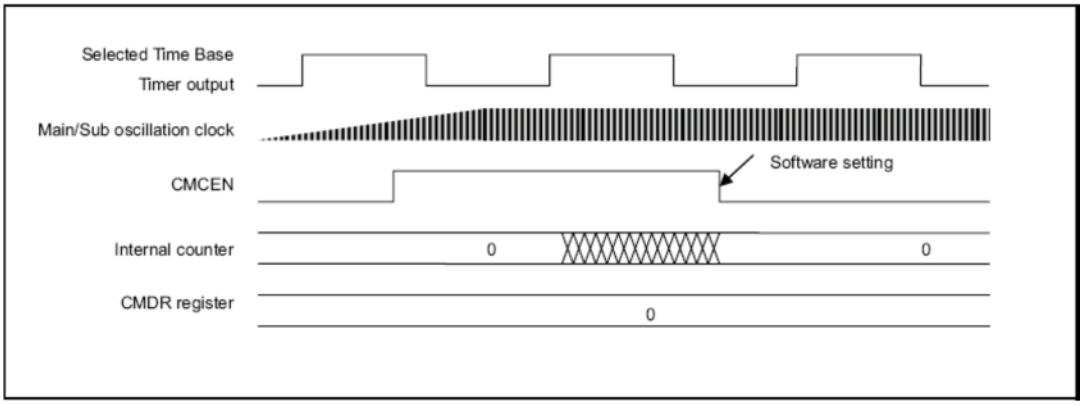
Figure 7. Clock Supervisor Counter Operation-4



- Clock Supervisor Counter Operation 5

The counter is cleared to "0" by the software if the CMCEN is set to "0" while the counter is operating.

Figure 8. Clock Supervisor Counter Operation-5



3.2 Table of Timebase Timer Intervals vs. Clock Supervisor Counter Values

The following table shows the Timebase Timer intervals suitable for respective main CRs and external clock frequencies.

Table 3. Count Value Table of Each TBTSEL Setting

Main CR (F_{CRH}) [MHz]	Main/Sub-oscillation [MHz]	Main CR error	Measure-ment error	TBTSEL2 - TBTSEL0							
				"000"	"001"	"010"	"011"	"100"	"101"	"110"	"111"
				($2^3\times1/F_{CRH}$)	($2^5\times1/F_{CRH}$)	($2^7\times1/F_{CRH}$)	($2^9\times1/F_{CRH}$)	($2^{11}\times1/F_{CRH}$)	($2^{13}\times1/F_{CRH}$)	($2^{15}\times1/F_{CRH}$)	($2^{17}\times1/F_{CRH}$)
1	0.03277	+5%	-1	0	0	0	6	30	126	510	2044
		-5%	+1	1	1	3	9	36	142	566	2261
	0.5	+5%	-1	0	6	29	120	486	1949	7800	31206
		-5%	+1	3	9	34	135	539	2156	8624	34493
	1	+5%	-1	2	14	59	242	974	3899	15602	62414
		-5%	+1	5	17	68	270	1078	4312	17247	68986
	4	+5%	-1	14	59	242	974	3899	15602	62414	249659
		-5%	+1	17	68	270	1078	4312	17247	68986	275942
	6	+5%	-1	21	90	364	1461	5850	23404	93621	374490
		-5%	+1	26	102	405	1617	6468	25870	103478	413912
	10	+5%	-1	37	151	608	2437	9751	39008	156037	624151
		-5%	+1	43	169	674	2695	10779	43116	172464	689853
	20	+5%	-1	75	303	1218	4875	19503	78018	312075	1248303
		-5%	+1	85	337	1348	5390	21558	86232	344927	1379706
	32.5	+5%	-1	122	494	1979	7922	31694	126779	507122	2028494
		-5%	+1	137	548	2190	8758	35032	140127	560506	2242022
8	0.03277	+5%	-1	0	0	0	0	2	14	62	254
		-5%	+1	1	1	1	2	5	18	71	283
	0.5	+5%	-1	0	0	2	14	59	242	974	3899
		-5%	+1	1	2	5	17	68	270	1078	4312
	1	+5%	-1	0	0	6	29	120	486	1949	7800
		-5%	+1	1	3	9	34	135	539	2156	8624
	4	+5%	-1	0	6	29	120	486	1949	7800	31206
		-5%	+1	3	9	34	135	539	2156	8624	34493
	6	+5%	-1	1	10	44	181	730	2924	11701	46810
		-5%	+1	4	13	51	203	809	3234	12935	51739
	10	+5%	-1	3	18	75	303	1218	4875	19503	78018
		-5%	+1	6	22	85	337	1348	5390	21558	86232
	20	+5%	-1	8	37	151	608	2437	9751	39008	156037
		-5%	+1	11	43	169	674	2695	10779	43116	172464
	32.5	+5%	-1	14	60	246	989	3960	15846	63389	253560
		-5%	+1	18	69	274	1095	4379	17516	70064	280253

Table 4. Count Value Table of Each TBTSEL Setting

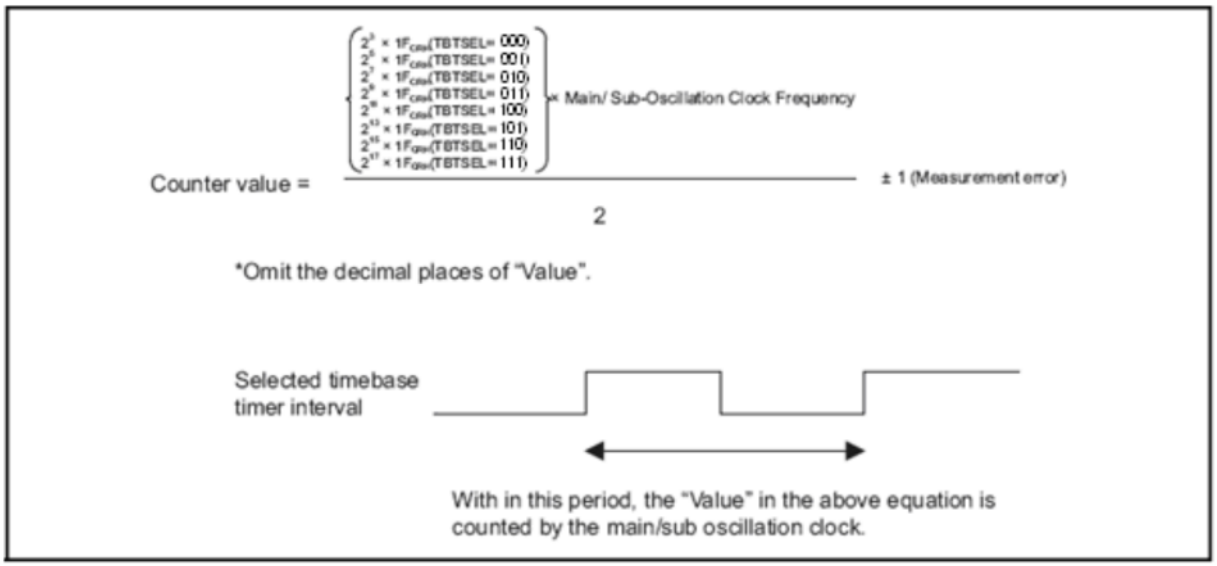
Main CR (F_{CRH}) [MHz]	Main/Sub-oscillation [MHz]	Main CR error	Measure-ment error	TBTSEL2 - TBTSEL0							
				"000"	"001"	"010"	"011"	"100"	"101"	"110"	"111"
				($2^3 \times 1/F_{CRH}$)	($2^5 \times 1/F_{CRH}$)	($2^7 \times 1/F_{CRH}$)	($2^9 \times 1/F_{CRH}$)	($2^{11} \times 1/F_{CRH}$)	($2^{13} \times 1/F_{CRH}$)	($2^{15} \times 1/F_{CRH}$)	($2^{17} \times 1/F_{CRH}$)
10	0.03277	+5%	-1	0	0	0	0	2	11	50	203
		-5%	+1	1	1	1	1	4	15	57	227
	0.5	+5%	-1	0	0	2	11	47	194	779	3119
		-5%	+1	1	1	4	14	54	216	863	3450
	1	+5%	-1	0	0	5	23	96	389	1559	6240
		-5%	+1	1	2	7	27	108	432	1725	6899
	4	+5%	-1	0	5	23	96	389	1559	6240	24965
		-5%	+1	2	7	27	108	432	1725	6899	27595
	6	+5%	-1	1	8	35	145	584	2339	9361	37448
		-5%	+1	3	11	41	162	647	2587	10348	41392
	10	+5%	-1	2	14	59	242	974	3899	15602	62414
		-5%	+1	5	17	68	270	1078	4312	17247	68986
	20	+5%	-1	6	29	120	486	1949	7800	31206	124829
		-5%	+1	9	34	135	539	2156	8624	34493	137971
	32.5	+5%	-1	11	48	197	791	3168	12677	50711	202848
		-5%	+1	14	55	219	876	3504	14013	56051	224203

: Recommended setting.

: The counter value becomes “0” or “255”.

The above Tables, Figure 9 and Figure 10 are calculated by the following equation:

Figure 9. Equation



Note: For the Timebase Timer operation and External Clock selection, refer to Chapter 6 and Chapter 10 of 8FX MCU Hardware Manual.

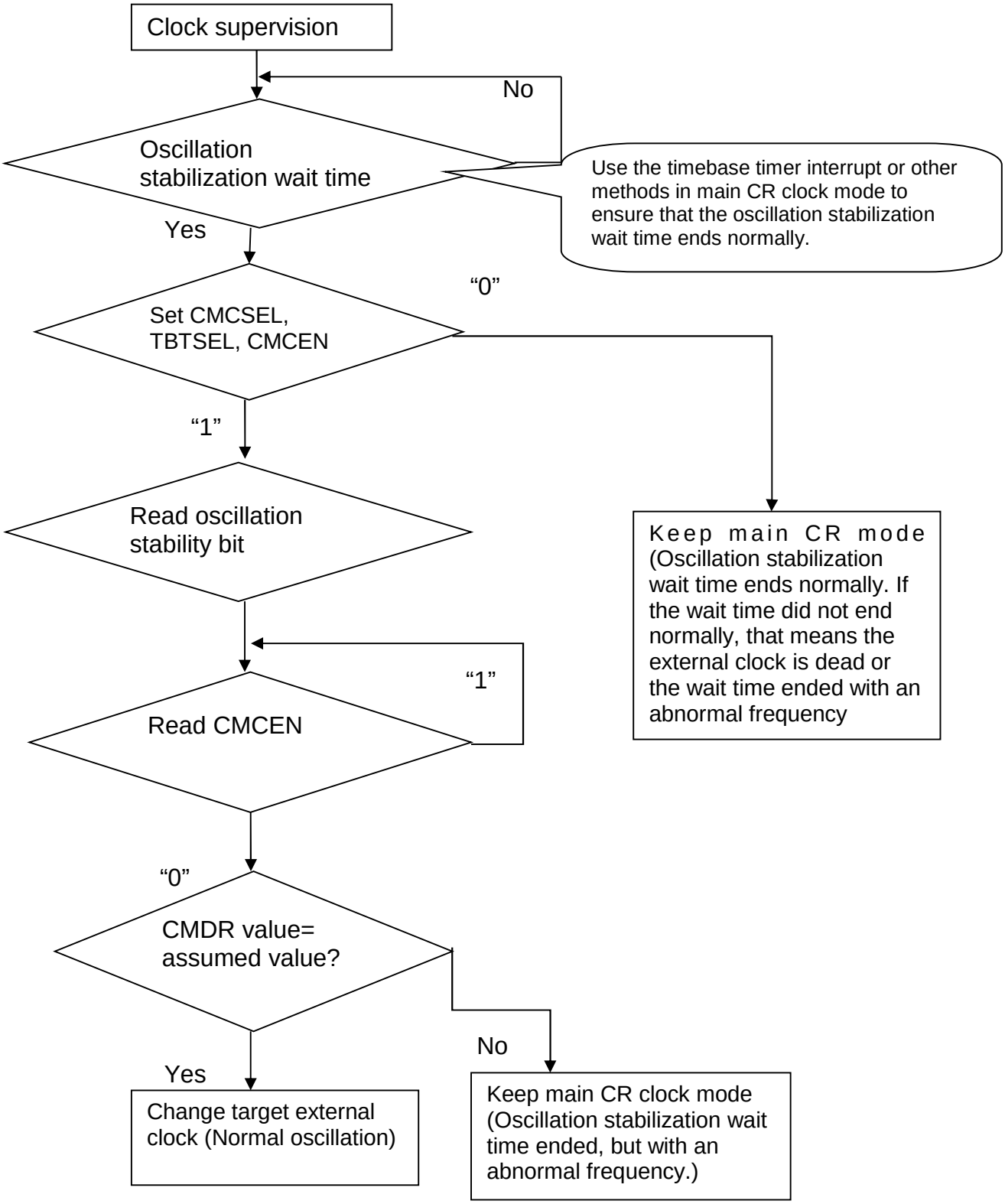
3.3 Usage for Clock Supervisor Counter

3.3.1 Operation Process

1. Enable the External Clock and wait after it's stabilization
2. Setup CMCR register to select the External Clock and the Timebase Timer output.
3. Enable Counter.
4. Watch result from the CMDR after the Counter stops.
5. Refer to Table of Timebase Timer Intervals vs. Clock Supervisor Counter Values for corresponding items.

3.3.2 Sample Operation Flowchart for the Clock Supervisor

Figure 10. Sample Operation Flowchart of the Clock Supervisor



3.3.3 Example Code

The following example shows how to use the Clock Supervisor Counter to check external main oscillator clock (4 MHz). Set Timebase Timer interval to $2^9 \times 1/F_{CRH}$; and then enable the clock supervisor counter operation.

```
SYCC2 = 0x25;           //main clock
SYSC = 0x03;            // enable/disable Sub OSC by SYCC2:SOSCE &
                           enable/disable Main OSC by SYCC2:MOSCE
CMCR_TBTSEL = 3;        //select Timer Base Timer output
CMCR_CMCSEL = 0;        // "0" select main clock “1" select subclock
CMCR_CMCEN = 1;         //enable CSV   '0' -->disable ‘1’-->enable
while (CMCR_CMCEN);     //wait the counter stop
ii = CMDR;              //read count value
```

Note: Refers to project CSV for Code.

When the counter stops, read the count value from the Clock Monitoring Data register (CMDR), and refer to Figure 12 and Figure 13 for corresponding items so as to check whether the external clock frequency is correct or not.

Figure 11. Example

		-5%	+1	1	3	9	34	135	539	2156	8624
8	4	+5%	-1	0	6	29	120	486	1949	7800	31206
		-5%	+1	3	9	34	135	539	2156	8624	34493
	6	+5%	-1	1	10	44	181	730	2924	11701	46810

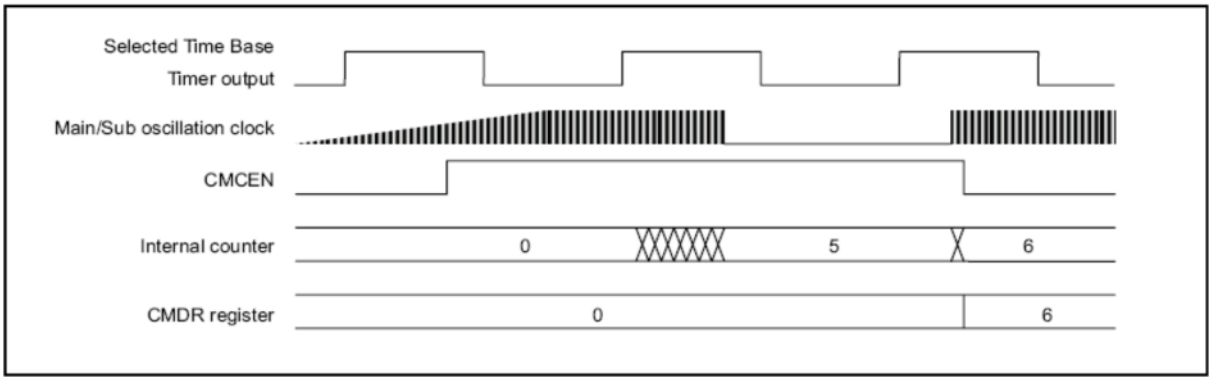
4 Notes on Using Clock Supervisor Counter

This chapter explains precautions when using Clock Supervisor Counter.

Notes on using the Clock Supervisor Counter:

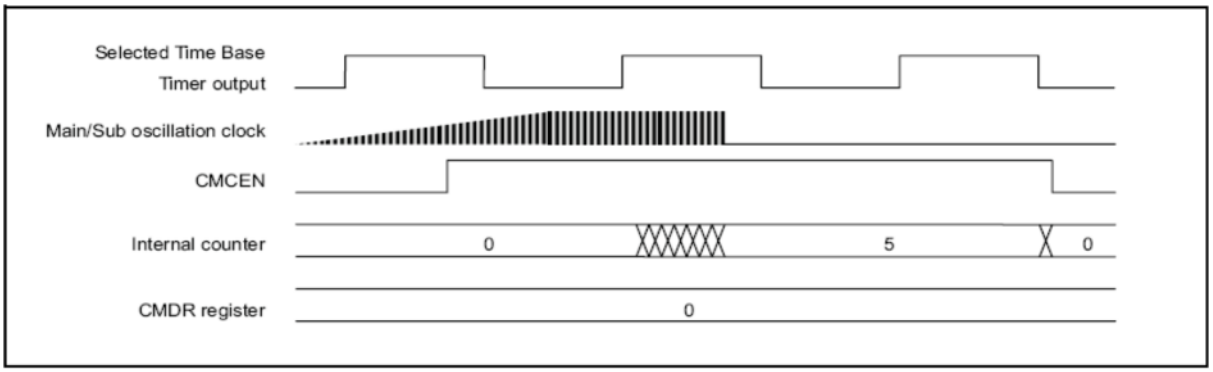
- Restrictions
  - Please use main CR clock mode only. DO NOT use other clock modes.
  - If Timebase Timer stops, internal counter does not work. And DO NOT clear Timebase Timer during this module is counting external clock.
  - Please select sufficient Timebase Timer output to count the clock supervisor counter. Refer to the Tables Figure 9 and Figure 10 for an example of Timebase Timer selection.
  - Please read CMDR register when CMCEN=0. (CMDR read value remains at "0" when counter is running (CMCEN="1").)
  - Please use this counter under the condition of machine clock is shorter than half period of selected Timebase Timer. If you use longer period of machine clock than half period of selected Timebase Timer, there is a possibility that CMCEN remaining at "1" after counter stops.
- If the external clock stops when counter is running and restarts external clock after the 2nd time rising edge detects selected Timebase Timer, CMCEN set to "0" after restarts external clock.

Figure 12. Clock Supervisor Counter Operation-1



- If the clock supervisor stops when counter is running. CMCEN is set to "0" by the falling edge detection of selected Timebase Timer after the 2nd time rising edge detection. The counter is cleared by this Timebase Timer falling edge.

Figure 13. Clock Supervisor Counter Operation-2



5 Additional Information

For more Information on MB95200 Products, visit the following website:

http://www.cypress.com/8fx-mb95200

5.1 Sample Code

Project Name: CSV

Function: check external clock

```
/*****************************************************************************************************
Name:       main.c
Function:   check external clock
*****************************************************************************************************/
#include "mb95200.h"
unsigned char ii;
/*****************************************************************************************************
Name:       vSysInit()
Function:   initial CMCR and I/O port 6
*****************************************************************************************************/
void vSysInit(void)
{
   SYCC2 = 0x25;                //main clock
   SYSC = 0x03;                 //enable/disable Sub OSC by SYCC2:SOSCE &
                                  enable/disable Main OSC by SYCC2:MOSCE
   CMCR_TBTSEL = 3;             //select Timer Base Timer output
   CMCR_CMCSEL = 0;             // "0" select main clock “1" select subclock
   CMCR_CMCEN = 1;              //enable CSV   '0' -->disable ‘1’-->enable
   PDR6 = 0x00;                 //port 6
   DDR6 = 0xFF;                 // unused - set all pins to output 'L'
}

/*****************************************************************************************************
Name:       main ()
Function:   loop main
*****************************************************************************************************/
void main(void)
{
   vSysInit ();                 //initial
   while (1)
   {
```

```
        while (CMCR_CMCEN);     //wait next edge detection and stop count
        ii = CMDR;              //read the count value from CMDR
        if (ii >= 120 && ii <= 135)    // compare count value and the item of table
        {
           PDR6 = 0x f7;              // if the external clock frequency is correct, the LED4 light
        }
        else
        {
           PDR6 = 0x ef;              //if the external clock frequency is not correct, the LED3 light
        }
        CMCR_CMCEN = 1;               //enable CSV   '0' -->disable '1'-->enable
    }
}
```

6 Document History

Document Title: AN205334 - F²MC-8FX Family, MB95200H/210H Series Clock Supervisor Counter

Document Number: 002-05334

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	HUAL	03/20/2008	Initial release
			03/20/2008	Modified Figure 3.1-3 and Figure 3.2-1; and updated this manual by new HWM.
*A	5264255	HUAL	05/11/2016	Migrated Spansion Application Note MCU-AN- 500012-E-11 to Cypress format

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