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AN205322

FR Family, MB91460 Microcontroller Alarm Comparator

This application note describes the functionality of the Alarm Comparator and gives some examples. The Alarm Comparator is used for detection of under-voltage or over-voltage conditions.

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1 Introduction

This application note describes the functionality of the Alarm Comparator and gives some examples. The Alarm Comparator is used for detection of under-voltage or over-voltage conditions.

1.1 Key Features

- Detection of Under-Voltage and Over-Voltage by comparison of external voltage input with AVDD/AVSS
- Generation of Interrupt on detection of Under-Voltage or Over-Voltage condition
- Controlled power consumption by choosing appropriate power mode
- Run Mode by default (after power-on)

2 The Alarm Comparator

THE BASIC FUNCTIONALITY OF THE ALARM COMPARATOR

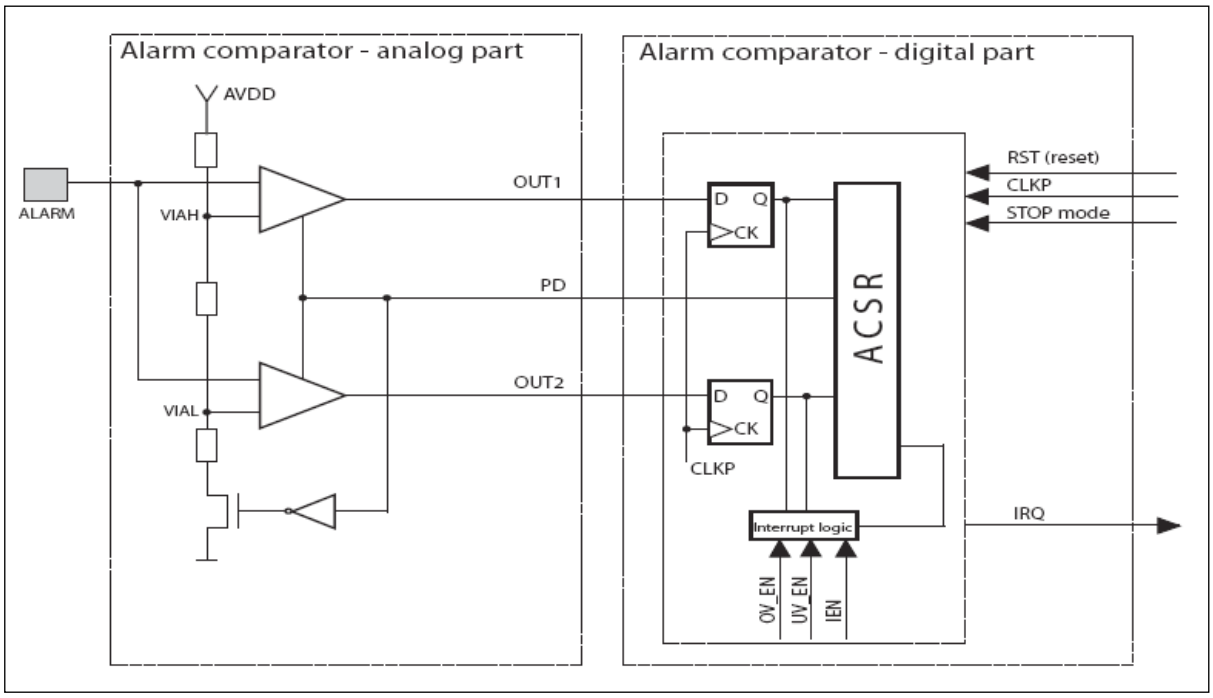
2.1 Introduction

The Alarm Comparator is used to detect under-voltage and over-voltage at an external analog input pin. It can be compared with AVDD/AVSS. It can be switched to fast or slow detection mode. The slow mode reduces the power consumption of this module. By default, the alarm comparator is in run mode.

2.2 Block Diagram

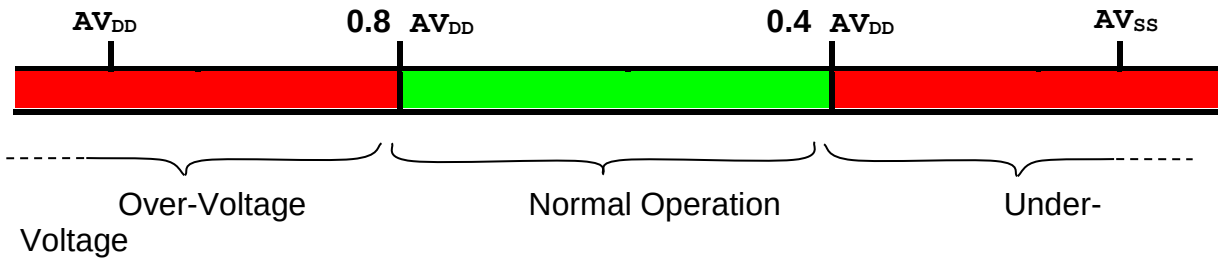
Figure 1 shows the internal block diagram of the Alarm Comparator.

Figure 1. Alarm Comparator block diagram



2.3 Voltage Detection Areas

Figure 2. Voltage Detection Areas



2.4 Standby Modes

It should be noted that the digital part of the alarm comparator is stopped in STOP or TIMER mode and it's operating in SLEEP mode. The analog part status is dependent on the `PD` bit of the `ACSRn` register. Hence it is possible to wake up only from the SLEEP mode (and not from STOP or TIMER mode) in the event of under / over voltage interrupts (if the analog comparator is in RUN mode and these interrupts are enabled).

Before switching to these modes it is advisable to put the alarm comparator in the power down mode, if the current consumption is critical for the application. For this purpose the interrupt should be disabled first and then alarm comparator should be put to power down mode.

2.5 Registers

2.5.1 Alarm Comparator Control/Status Register (ACSRn)

Table 1. ACSRn

Bit No.	Name	Explanation	Initial Value	Value	Operation
7	MD	Mode Select	0	0	Slow Mode (less power consumption)
				1	Fast Mode (high power consumption)
6	OV_EN	Over-Voltage Interrupt Enable	1	0	No Interrupt in case of Over-Voltage
				1	Interrupt in case of Over-Voltage
5	UV_EN	Under-Voltage Interrupt Enable	1	0	No Interrupt in case of Under-Voltage
				1	Interrupt in case of Under-Voltage
4	OUT2	Output of Alarm Comparator UV	X	0	ALARMn < 0.4 * AVDD
				1	ALARMn > 0.4 * AVDD
3	OUT1	Output of Alarm Comparator OV	X	0	ALARMn < 0.8 * AVDD
				1	ALARMn > 0.8 * AVDD
2	IRQ	Interrupt Request	X	0	No Under-Voltage or Over-Voltage Condition detected
				1	Under-Voltage or Over-Voltage Condition detected[1]
1	IEN	Interrupt Enable	0	0	Disable Interrupt
				1	Enable Interrupt
0	PD	Power Down Mode	0	0	Run Mode (Analog Part)
				1	Power Down Mode (Analog Part)

States of OUT0 and OUT1 and Voltage Condition

Table 2. Analog Comparator Outputs in Different Voltage Conditions

OUT0	OUT1	Condition
0	0	Under-Voltage
0	1	Not possible
1	0	Normal Operation
1	1	Over-Voltage

[1] It should be noted that the IRQ bit will be set with the next positive transition of CLKP after detecting an interrupt event and it will remain set unless and until the under-voltage or over-voltage condition persists. In such situation if the IEN is set to 1, the interrupt service routine will be executed even after clearing the IRQ bit in it. Hence to clear an interrupt caused by a persistent Under-Voltage or Over-Voltage condition the OVEN and/or UVEN bits should be cleared first and then the IRQ bit should be cleared separately.

3 Alarm Comparator Example

EXAMPLE FOR THE ALARM COMPARATOR

3.1 Under-Voltage and Over-Voltage with AVDD and AVSS as Reference Voltage

In this example AVDD and AVSS are used for Reference Voltage. Please note that in this example the root cause for the Alarm Comparator interrupt is not reset. If under-voltage or over-voltage persists after the ISR, the interrupt is generated again. To prevent this, the IEN bit or OVEN and/or UVEN bits of the ACSR0 may be set to “0” in the ISR before clearing the interrupt flag (IRQ).

Main.c

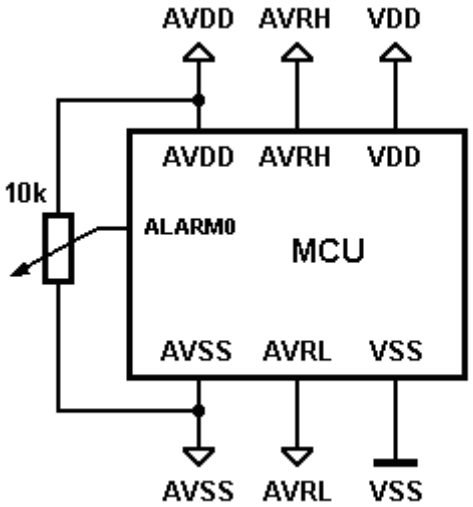
```
/* SAMPLE CODE
/*------------------------------------------------------------------------------*/

void InitAlarmComp (void)
{
  ACSR0 = 0x62;  // Slow Mode, Over and Undervoltage, Interrupt enable, Run Mode
}

/*------------------------------------------------------------------------------*/

void main(void)
{
  InitIrqLevels();
  __set_il(7);    // allow all levels
  __EI();         // globally enable interrupts

  InitAlarmComp();

  while(1);
}

/*------------------------------------------------------------------------------*/

__interrupt void AlarmISR (void)
{
  if (ACSR0_OUT1 && ACSR0_OUT2)
  {
    // Overvoltage (Vin > 0.8 * AVDD)
    //
    // Do something...
  }
  else
  {
    // Undervoltage (Vin < 0.4 * AVDD)
    //
    // Do something...
  }

  ACSR0 = 0x62;  // clear Interrupt
}
```

vectors.c

```
/*SAMPLE CODE
/*-------------------------------------------------------------------------
*/
void InitIrqLevels(void)
{
       . . .

ICR60 = 30;     /* Alarm Comperator 0           */
    . . .
}

/* ISR prototype */
__interrupt void AlarmISR (void);

    . . .

#pragma intvect AlarmISR 136 // Alarm Comparator of MB9634x Series

    . . .
```

With the following schematic, the code above can be tested easily.

Figure 3. Example Test Schematic



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The software example related to this application note is:

91460_alarmcomp

It can be found on the following Internet page:

http://www.cypress.com/cypress-mcu-product-softwareexamples

Document History

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**	—	NOFL	04/22/2008	V1.0, First draft, HPi
*A	5120074	NOFL	04/14/2016	Converted Spansion Application Note “MCU-AN-300071-E-V10” to Cypress format
*B	5836821	MALI	07/28/2017	Updated Logo and Copyright

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