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AN205321

FR Family, MB91460 A/D Converter

This application note describes the functionality of the Analog/Digital Converter (ADC) with examples.

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1 Introduction

This application note describes the functionality of the Analog/Digital Converter (ADC) and gives some examples.

1.1 Key Features

- Minimum conversion time per Channel: 3 µs
- RC type successive approximation conversion with sample & hold circuit
- 8-bit or 10-bit conversion resolution
- Sequential channel conversion, once (Single Mode), continuous (Continuous Mode) and converts one channel, stops and waits for the next activation (Stop Mode)
- Interrupt generation after conversion selectable
- Interrupt can trigger DMA to transfer conversion result to memory
- Triggered by software, external Pin (ATG) or Timer

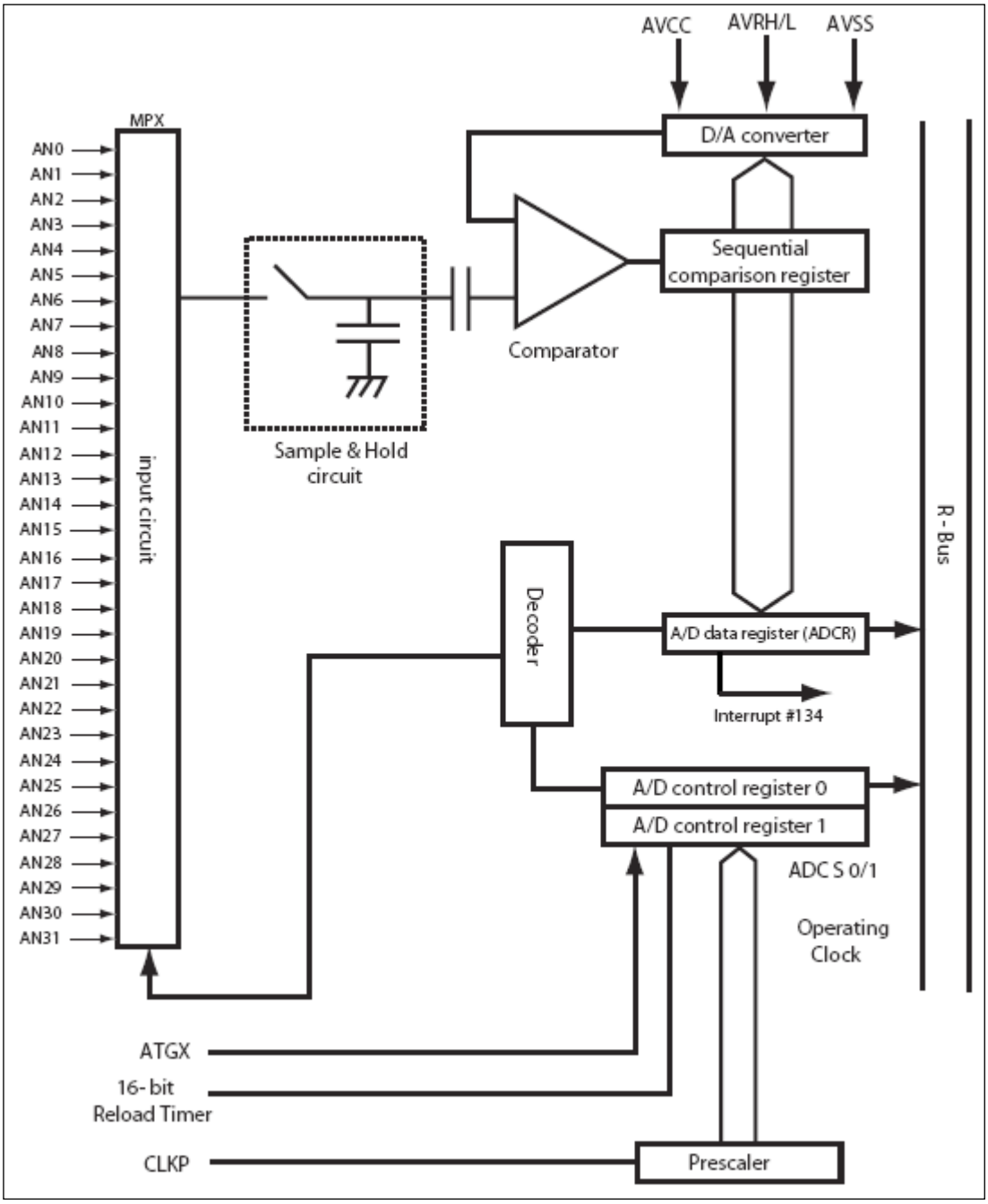
2 The Analogue/Digital Converter

The Basic Functionality of the Analogue/Digital Converter

2.1 Block Diagram

Figure 1 shows the internal block diagram of the ADC.

Figure 1. ADC Block Diagram



2.2 Registers

2.2.1 Control Status Register (ADCS1)

This register controls the A/D converter and indicates its status.

Table 1. ADCS1

Bit No.	Name	Explanation	Initial Value	Value	Operation
15	BUSY*	Busy Flag and Stop*	0	0	Read: No A/D Conversion Write: Force Conversion Stop
				1	Read: A/D Conversion ongoing Write: No effect
14	INT	Interrupt Flag	0	0	Read: No A/D Data Write: Clear Flag
				1	Read: A/D Data and Interrupt Write: No effect
13	INTE	Interrupt enable	0	0	Interrupt disabled
				1	Interrupt, if A/D Data
12	PAUS	A/D Converter Pause	0	0	Read: No A/D Conversion Pause Write: Clear Bit
				1	Read: Pause occurred Write: No effect
11, 10	STS1,0	Start Source Select	0, 0	0, 0	ADC Activation by Software
				0, 1	ADC Activation by Software and ADTG Pin
				1, 0	ADC Activation by Software and Timer
				1, 1	ADC Activation by Software, ADTG Pin, and Timer
9	STRT	Start Conversion	0	0	Always read; Write: no effect
				1	Start and Restart A/D Conversion
8	–	*Undefined*	X	0	*Reserved Bit , always write “0” to it*

2.2.2 Control Status Register (ADCS0)

This register controls the A/D converter and indicates its status.

Table 2. ADCS0

7, 6	MD1, 0	Operation Mode Select	0, 0	0, 0	Single Mode 1; Reactivation during Conversion allowed
				0, 1	Single Mode 2; Reactivation during Conversion not allowed
				1, 0	Continuous Mode; Reactivation during Conversion not allowed
				1, 1	Stop Mode; Reactivation during Conversion not allowed
5	S10	10-Bit Mode	0	0	10-Bit Conversion Mode
				1	8-Bit Conversion Mode
4 … 0	ACH4- ACH0	A/D converter mode set	00000	Read	Current converted channel is shown during A/D converting (BUSY="1"). If conversion is halt by forcibly stopping, they show the stopped channel.
				Write	No effect to these bits.

* These bits return “1” during Read-Modify-Write instruction.

2.2.3 Date Register (ADCR1, ADCR0)

These register stores digital value generated as a result of conversion. This register contains the last converted value and is rewritten every time the conversion ends.

Table 3. ADCR1 & 2

Bit No.	Name	Explanation	Value	Operation
15 … 10	-	-	0	These bits always return “0”
9 … 0	D9 … D0	Data Bits	-	These bits contain A/D data after successful conversion

2.2.4 Sampling timer and setting register (ADCT1, ADCT0)

These registers sets the sampling and conversion time

Table 4. ADCT1 & 2

Bit No.	Name	Explanation	Initial Value	Operation
15 … 10	CT5 … CT0	Comparison Time Setting	0,0,0,1,0,0	Setting "000001" means one division (=CLKP). It’s not allowed to set these bits "000000" Note : It’s not allowed to set the comparison time over 500 us
9 … 0	ST9 … ST0	Sampling time	0,0,0,0,1, 0,1,1,0,0	Sampling time = ST value * CLKP cycle Note: It’s not allowed to set the sampling time below 1.2 us when AVCC is below 4.5 V.

Sampling/Conversion Time

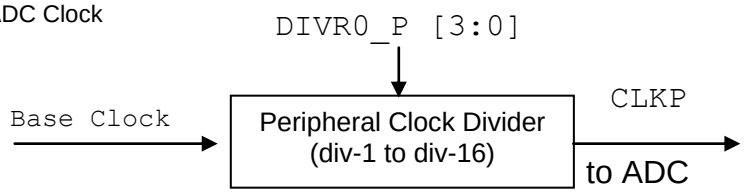
The sampling time must be equal to or greater than 0.4 µs. The Comparison time must be at least 0.6 µs. Therefore an overall A/D conversion time could be 1 µs, but this depends on the used peripheral clock.

Assume a peripheral clock of 16 MHz (62.5 ns cycle time). The sample cycle number then has at least to be 8 (0.5 µs) and the comparison time setting can be 1 (0.875 µs). Therefore the overall A/D conversion time is 1.375 µs.

All these settings are valid for **4.5 V ≤ AV_{CC} ≤ 5.5 V**. Please see the hardware manual for external impedance considerations.

Please consider that the source clock frequency of the Reload Timer (CLKP) depends on the settings of the Clock Division setting register (DIVR0).

Figure 2. ADC Clock



2.2.5 A/D Channel Setting Register (ADSCH, ADECH)

These registers specify the channels for the A/D converter to convert. Do not update these registers while the A/D converting is operating.

Table 5. ADSCH & ADECH

Bit No.	Name	Explanation	Initial Value	Value	Operation
15 … 13	-	*Undefined*	X	0	*Reserved Bit , always write "0" to it*
12 … 8	ANS4 … ANS0	Starting Channel Setting	0	00000	Start conversion from Channel 0
				…	
				11111	Start conversion from Channel 31
7 … 5	-	*Undefined*	X	0	*Reserved Bit , always write "0" to it*
4 … 0	ANE4 … ANE0	Ending Channel Setting	0	00000	End conversion at Channel 0
				…	
				11111	End conversion at Channel 31

Start/Stop Channels

- Use start channel = end channel for conversion of only one channel.
- If start channel is greater then end channel, conversion starts form start channel to the highest available channel, then from channel 0 to the end channel.

2.2.6 Analog Input Enable Register (ADER0 – ADERn)

While a pin is used as analog input, corresponding bit in ADER register have to be set to 1. If a channel between the configured scanning limits is not configured as ADC input (the corresponding bit in this register is “0”), this channel is skipped during the scanning process.

The following table shows ADERH.

Table 6. ADERH

Bit No.	Name	Explanation	Initial Value	Value	Operation
31 … 16	ADE31 … ADE16	ADC Input Selection	0	0	Digital I/O Port enabled
				1	Analog Input enabled

The following table shows ADERL.

Table 7. ADERL

Bit No.	Name	Explanation	Initial Value	Value	Operation
15 … 0	ADE15 … ADE0	ADC Input Selection	0	0	Digital I/O Port enabled
				1	Analog Input enabled

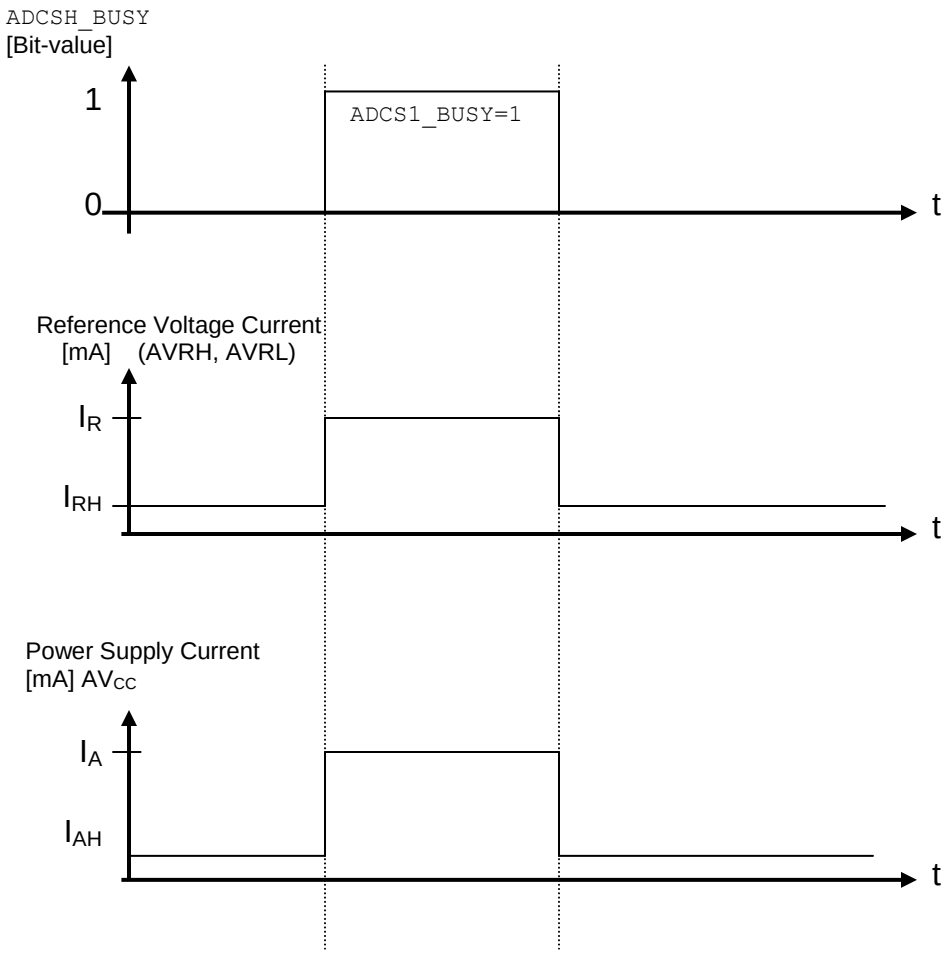
3 Power supply of A/D converter

Electrical Power Considerations

3.1 Power consumption

The power consumption (I_R, I_A) of the ADC increases in case a conversion is in progress (ADCS1_BUSY = 1). While the ADC is halted (ADCS1_BUSY = 0), only leakage current (I_{RH}, I_{AH}) flows. The following diagrams reflect this behaviour:

Figure 3. Power consumption and operating status of ADC



Note: Please refer to the datasheet in order to get the absolute values of I_R, I_{RH}, I_A and I_{AH}.

3.2 Noise consideration

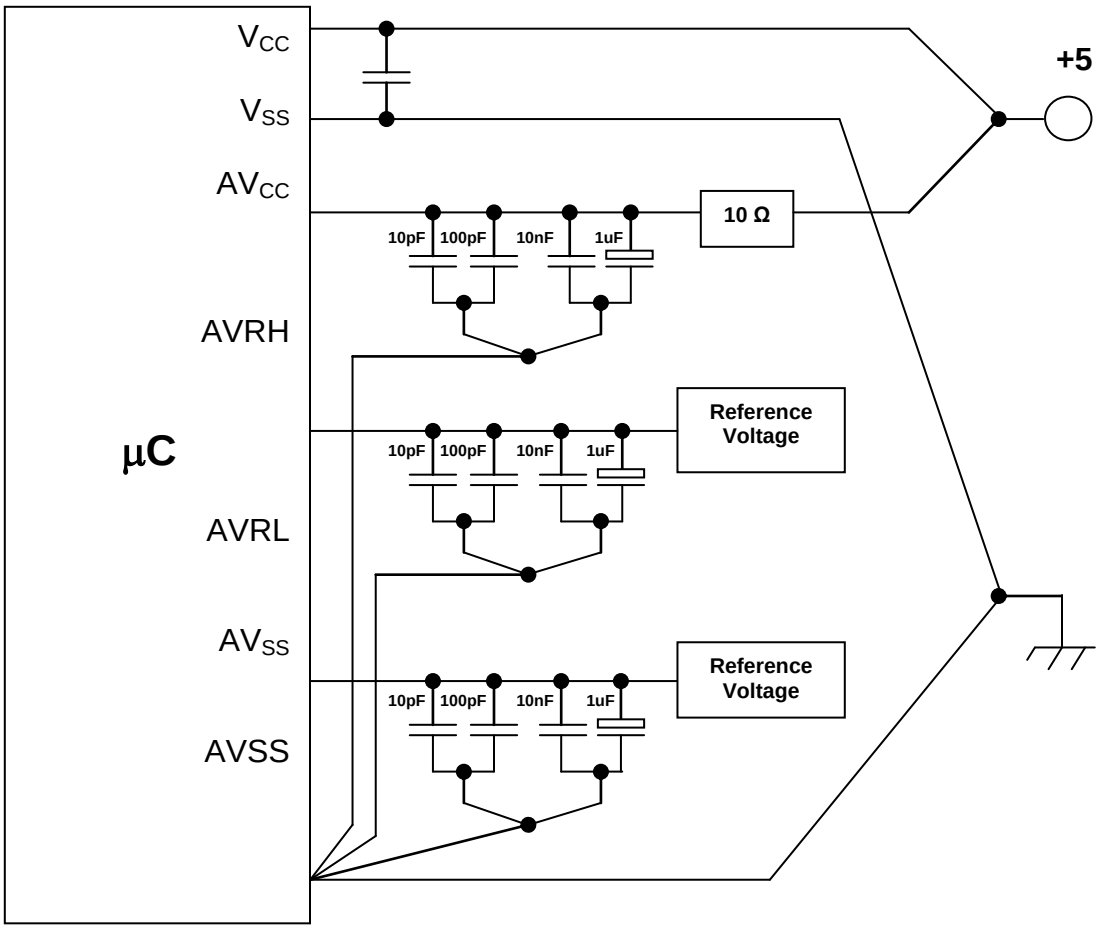
Cypress microcontroller has implemented an embedded 10-bit Successive Approximated Register (SAR) ADC. Due to the high resolution, the digital bit stream from the ADC output is sensitive to the environment noise. For example, 1LSB corresponds to only 4.9mV for U_{REF}=5V. Hence, the noise introduced from the external circuits must be considered and should be reduced to the minimum as possible.

The reference voltage U_{REF}, which is equal to AVRH-AVRL, is connected to the weighted capacitor array and the resistor array of the ADC. The noise coupled to AVR will not be rejected by ADC. This noise will be added to the U_{REF} directly, introducing an error with a ratio of U_{Noise}/U_{REF}. For example, to keep the error caused by this kind of noise below 0.1LSB, the noise level of U_{REF} must be kept within 0.49mV.

As a result, the pin AVRH and AVRL pins must be connected with low impedance. In practice often a simple low-pass RC-filter is used for noise reduction. In this case the reference voltage supply current (see datasheet) has to be taken into account when calculating the resistor of the filter, in order to minimize the voltage drop while converting. Normally two capacitors in parallel are recommended, one filtering low frequency noise, the other one filtering high frequency noise ((10nF–1μF)||(10pF-100pF)). In most cases, this configuration suppresses the noise efficiently. If very high frequency noise appears in the environment, an additional noise filter such as a dedicated π mode RC filter might be useful.

The analogue power path AV_{CC} supplies the internal voltage comparator and the analogue switches of the ADC, while the V_{CC} path supplies all the digital parts in the microcontroller. Internal parasitic capacitors may couple noise from AV_{CC} to the internal voltage comparator of the ADC. For this reason, also AV_{CC} should not be connected directly to V_{CC} but filter should be used, too. For more efficient noise filtering the same configuration as for AVRH is recommended.

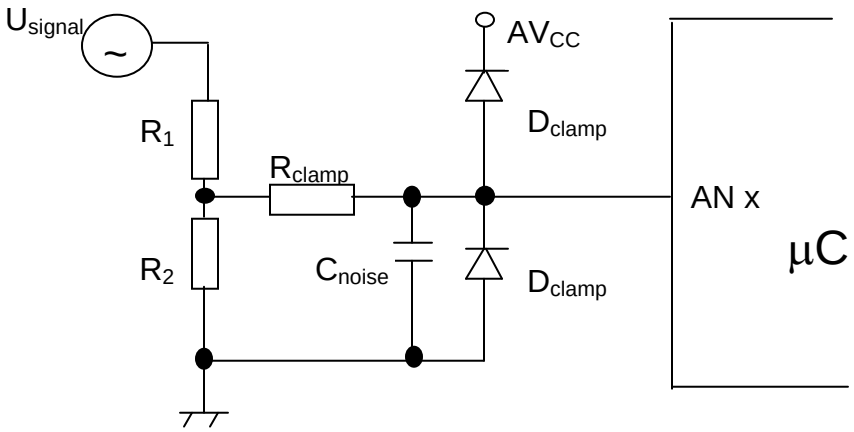
Figure 4. A suggested connection for the power supplies



4 Analogue input and related external circuits

4.1 External circuits for analogue input

Figure 5. A typical external circuit for analogue input



To protect the analogue pins to suffer from an over-voltage, the so-called “clamping resistor” is usually added to the input pins. The minimum value of the resistor can be chosen as

$R_{clamp} = U_{overvoltage}/I_{clamp}$,

Where, I_{clamp} is the specified maximum clamp current in the data sheet.

For some applications, a large clamp resistor is sometimes unacceptable. As a compromise, an external clamping diode with low leakage current could be added between the input pin and AV_{CC} pin.

In some cases, the sensor has been biased with a voltage supply higher than the maximum allowed voltage for the microcontroller. For example, in the automotive applications, the sensors could be biased directly with the car battery, which exhibits a voltage of 12V/24V. A resistor divider consisting of R_1/R_2 is commonly used to tail the sensor voltage signal “seen” on the pin down to the value which is equal or smaller than AV_{CC}/V_{CC} (see)

The ratio between R_1 and R_2 should satisfy the following constrain:

$$\frac{R_1}{R_2} \geq \frac{U_{Signal}}{AV_{CC}} - 1$$

Other factor which influences the size dimension of R_1, R_2 and R_{clamp}, is related to current consumption budget and the input signal noise suppressing. The second factor will be discussed here with more detail. The signal from the sensors could be also noisy. The noise, which has a time constant smaller than the sampling time $T_{sampling}$, is transparent to the ADC, resulting distorted output. In this case, an additional dedicated bypass capacitor together with the clamping resistor or resistor divider, works as a low pass filter. A larger capacitor will lower the AC impedance and will be more effective at shunt away the noise signal. Generally, the time constant of this low pass filter (R_{clamp} + R_1 || R_2) x C_{noise} should be chosen considerably larger than the sampling time (5 to 10 times larger with a rule of thumb).

However, at the same time this time constant should be also considerably smaller than the one of the sensor signal, depending on the applications. In this way, the analogue pin is able to follow the dynamic changes, which the ADC is being used to track. These, along with the dimension of R_1/R_2 or R_{clamp} must be considered when choosing the capacitor dimension to avoid rolling off any high frequency signal components of interest.

4.2 Input Leakage current consideration

The analogue input pins show a small leakage current, whose maximum value is about 3μA and ranged from 3μA down to 1μA depending on the temperature. The leakage current, which flows through the external resistor, introduces an undesired voltage drop. This error voltage is a function of the external resistor and the leakage current itself. The following example shows a dimension of the resistor with this factor taken into consideration. For the case of using a resistor divider to reduce the error due to leakage current, the size of $R_1 \parallel R_2 + R_{clamp}$ should not be chosen too large and should be according to the following equation:

$$R_1 \parallel R_2 + R_{clamp} \leq \frac{U_{LSB}}{I_{leakage}}$$

Note:
$U_{LSB} = U_{REF} / 1024$

To keep the error smaller than one LSB for a leakage of 3μA, the size of $R_1 \parallel R_2 + R_{clamp}$ should be smaller than 1.6kΩ. As the leakage current drops down to 1 μA, the value of R1 || R2 + R_{clamp} can be chosen as large as 5kΩ. This is considering U_{REF} of 5V.

It is found in the test that the leakage current consists of two parts: one is due to the leakage current of the input ESD structure. Another leakage current appears only as the multiplexer is switched on during the sampling time, whose contribution is usually considerably larger than the one created from ESD structure. The second leakage current can be regarded as a noise during the sampling time by the bypass capacitor, which is commonly used to filter the noise from the sensor input. If this capacitor is large enough, it can absorb most of the second leakage current during the sampling time, eliminating its contribution to the error voltage.

Figure 6. Leakage current flowing to the analogue input pin

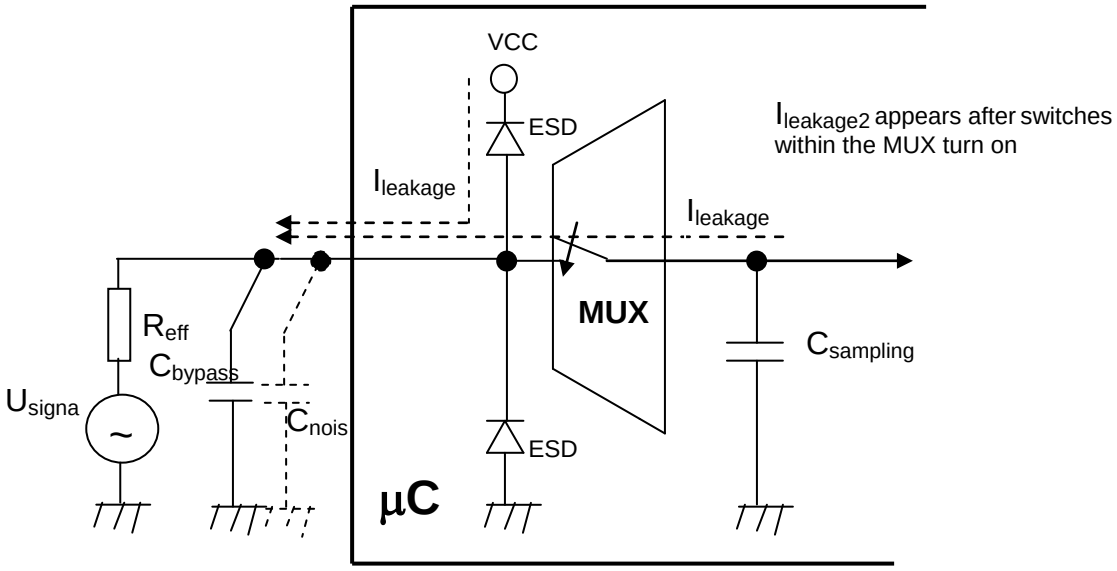
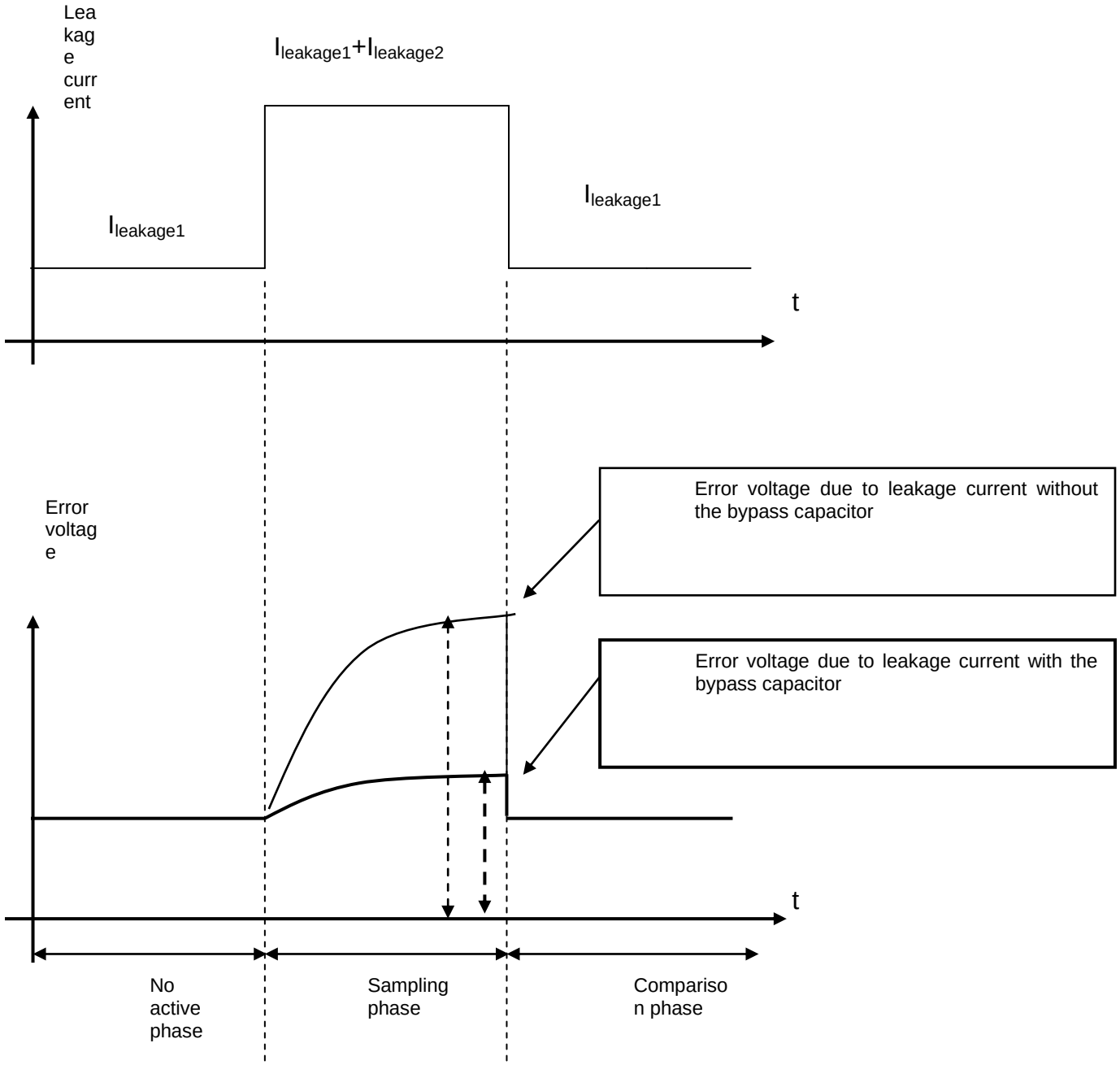


Figure 7. Reducing the leakage current with the bypass capacitor



To show the effect of the bypass capacitor on reducing the leakage current error, we take a sampling time of 5μs and a leakage current of 3μA as an example. If we want to keep the voltage drop due to the second leakage current small than 0.5 LSB, the minimum size of the bypass capacitor should be chosen as:

$$C = \frac{3\mu A \times 5\mu s}{4.9mV/2} \approx 6nF$$

5 Sampling time consideration

Cypress applies an embedded 10-bit successive approximation register ADC with an internal integrated sampling and hold stage. The signal will charge the sampling capacitor at first and then the voltage signal on the sampling capacitor will be evaluated by the 10-bit ADC successively. The time to charge the sampling capacitor to its final value equal to the signal level is a function of the sampling capacitor $C_{sampling}$, the external resistor and the internal switch on-resistor.

To reduce the error caused by the limited sampling time to an acceptable level, the sampling time should be chosen much larger than the time constant to charge the sampling capacitor. For example, if we choose a sampling time with a factor 7 of the RC constant, namely, $7 \times (R_{extern} + R_{switch}) \times C_{sampling}$. Then the error amounts to $e^{-7} \times U_{REF}$, corresponding $0.94 \times U_{LSB}$ only.

For MB91467D Series, the on-resistor of the transmission gate amounts to 2.6kΩ and the sampling capacitor $C_{sampling}$ equals to 11pF at AV_{CC} = 5V. For an external resistor of 2.25kΩ, the sampling time should be chosen larger than $7 \times (2.25k\Omega + 2.6k\Omega) \times 11pF = 0.37\mu s$ by using above thumb rule.

Figure 8. Block diagram for ADC in MB91F460D Series

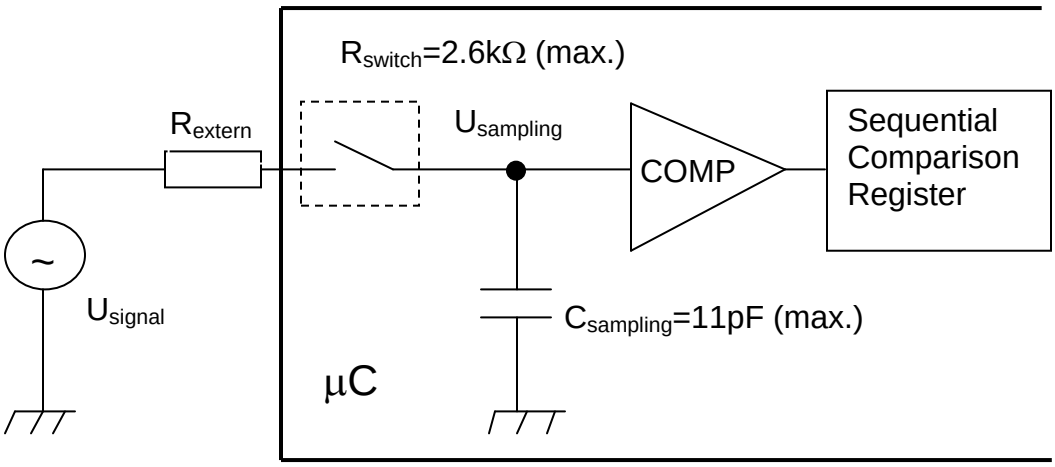
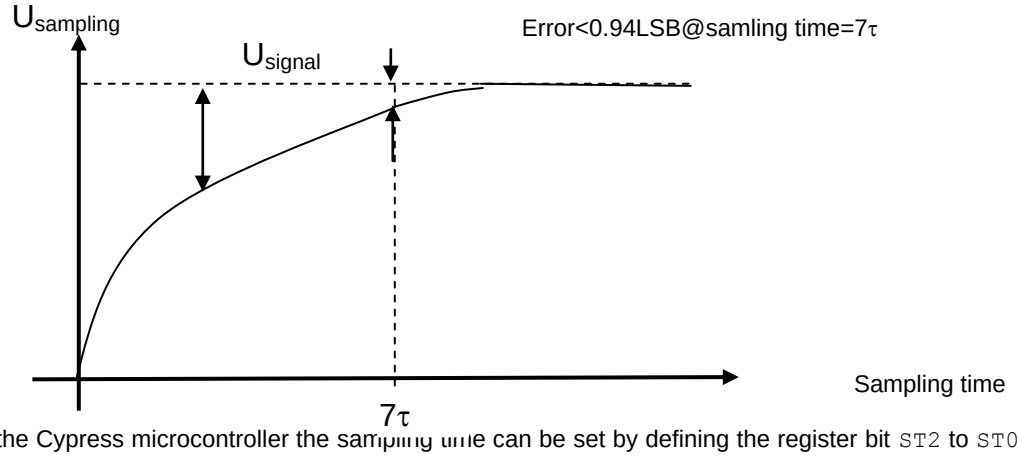


Figure 9. Error related to sampling time



For the Cypress microcontroller the sampling time can be set by defining the register bit ST2 to ST0 of the ADC data register (ADCT). Please refer to the hardware manual.

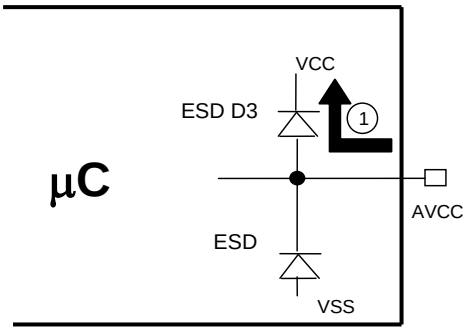
6 Latch-up related to AVCC/VCC and large input signal

RECOMMENDATIONS TO PREVENT LATCH-UP

Latch-up conditions can permanently damage the device and must be avoided. It is up to the application to assign any precautions in order to avoid any latch-up condition.

6.1 AVCC > VCC

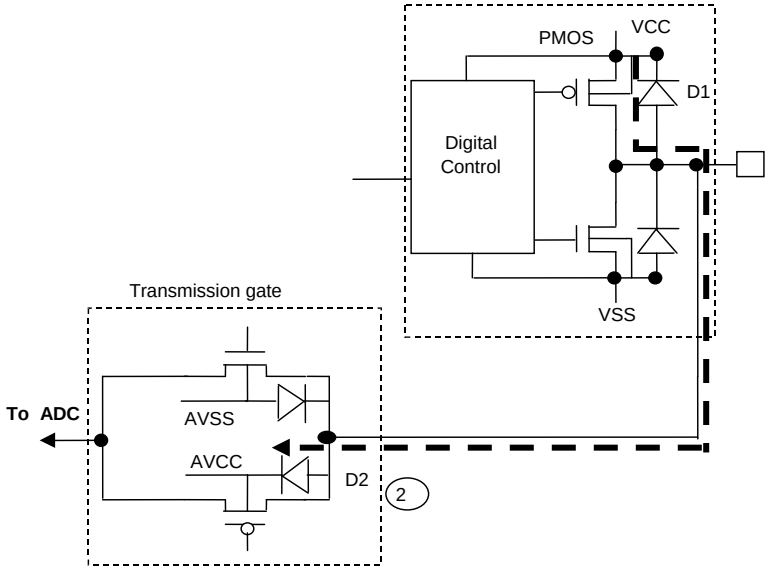
Figure 10. Latch-up in case AVCC > VCC



Latch-up can happen if AV_{CC} becomes larger than V_{CC}. This might be related to the application cases that V_{CC} is switched on later than AV_{CC} or V_{CC} is switched off earlier than AV_{CC}. The ESD diode D3 becomes forward biased, introducing a possible latch-up.

6.2 AVCC < VCC

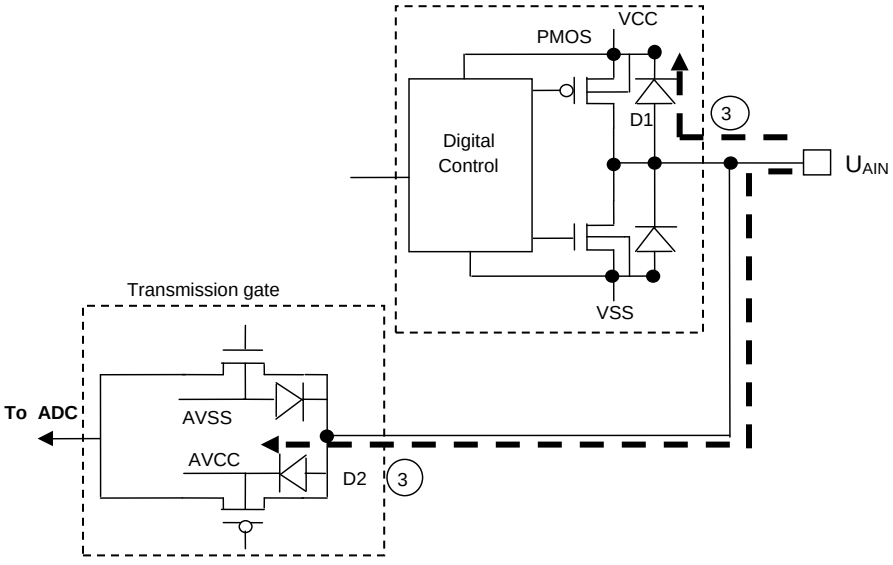
Figure 11. Latch-up in case AVCC < VCC



This case happens if the analogue pin is used as a digital output pin, the output level is “H”, and at the same time, AV_{CC} is switched off. In this case, the PMOS in the output is on and the parasitic diode D2 of the transmission gate within the analogue multiplex becomes forward biased. A quiescent current flows through PMOS and D2. In case that a latch-up does not happen, a reliable logic “1” should not be expected at the output, due to the load diode D2.

6.3 UAIN > AVCC or VCC

Figure 12. Problem in case UAIN > AVCC or VCC



If U_{AIN} becomes larger than V_{CC} or AV_{CC}, then the ESD diode D1 or D2 will be forward biased. A latch-up can happen. Even if a latch-up does not always happen in this case, the input signal, which exceeds V_{CC} or AV_{CC}, cannot be converted by the ADC properly.

6.4 Conclusion

It is strongly suggested that AV_{CC} and V_{CC} should be DC short circuit together to avoid any possible latch-up.

With the presence of AV_{CC} and V_{CC} voltage, an analogue input signal, which is smaller than AV_{CC} and V_{CC} can be always put on the analogue pins, independent on the MCU modes.

Latch-up conditions can permanently damage the device if the related specified currents are exceeded. So Latch-up conditions must be avoided under all circumstances. It is up to the application to assign any precautions in order to avoid any latch-up condition.

7 Input Impedance

ADC BEHAVIOR ON HIGH INPUT IMPEDANCES

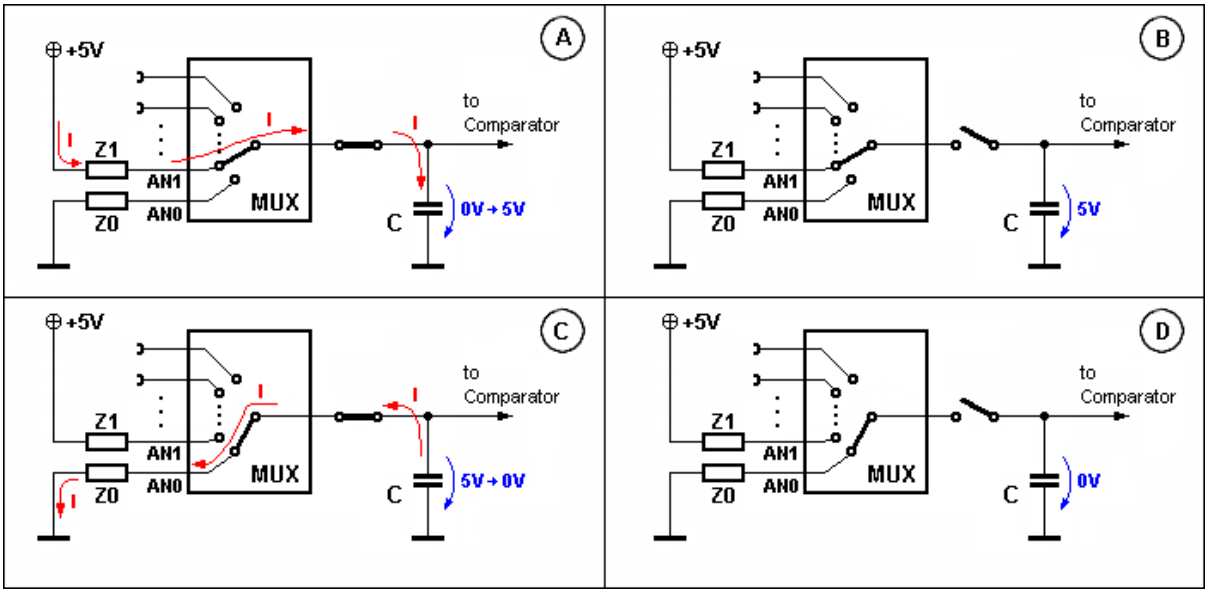
7.1 Recharging and discharging the Sampling capacitor

Because the ADC uses a sampling capacitor the input impedance must be set to a value below 15 kΩ to recharge or discharge this capacitor within the sampling time.

Example:

Assume an application uses two ADC inputs. At one pin there is a voltage of about Vcc and at the other pin Vss. The first conversion charges the internal capacitor to Vcc within the sample time (A). After this the conversion starts (B). At the second conversion the MUX switches to the other input and the capacitor is discharged to Vss (C). The second conversion starts (D). If the input impedance (Z_0) is too high, a rest of charge will remain and a wrong conversion will result.

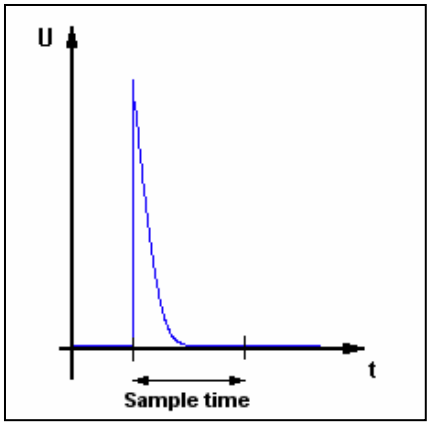
Figure 13. Current flow in the example



The left illustration shows the voltage glitch on AN0 if Z_0 is low.

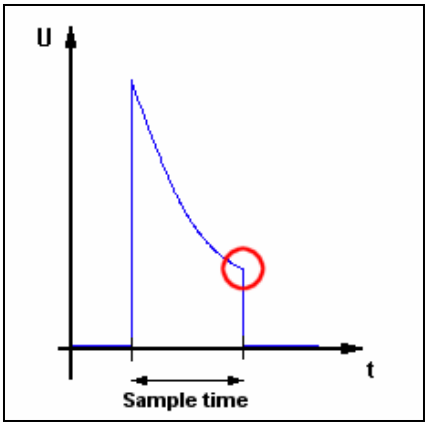
The glitch occurs, when the sampling switch is closed.

Figure 14. Voltage glitch at low input impedance



In this illustration the input impedance Z_0 is too high. The sampling capacitor is not discharged within the sampling time and thus a wrong voltage is converted (red circle).

Figure 15. Voltage glitch at high input impedance



Note: At high impedance input circuit, there will always be a glitch of about 0.5 Volts max even if the previous conversion was at 0 Volt. This results from the ADC internal architecture itself.

For the same reason discussed in this chapter an EMI capacitors for any analogue input pins should not exceed 1 nF.

8 ADC Example

Examples for the ADC

8.1 ADC with interrupts

Main C

```
SAMPLE CODE
------------------------------------------------------------------------
-*/
void InitADC (void)
{
       PFR29_D1 = 1;        /* resource function mode: analog input AN1 */
       ADERL = 0x0002;      /* channel 1 to analog input              */
       ADCS0 = 0xA0;        /* ADC set to 8 bit continuous mode       */
       ADCT1 = 0xFF;        /* Comparison time = 39.62uS @ 16MHz CLKP*/
       ADCT0 = 0xFF;        /* Sampling time = 63.94uS @ 16MHz CLKP */
       ADSCH = 0x01;        /* convert only AN1 */
       ADECH = 0x01;
       ADCS1 = 0xA2;        /* interrupt enabled, software trigger,
                            start conversion */
}

void main (void)
{
    DDR00 = 0xFF ;   /* Data direction Port 0 = Output        */
    InitIrqLevels();
    __set_il(7);            /* allow all levels                      */
    __EI();          /* globally enable interrupts            */

    PFR16 = 0x00;
    DDR16 = 0xFF;
    PDR16 = 0x00;

       InitADC();           /* init AD - converter                   */

    while(1)         /* waiting for interrupt (no operation)  */
       __asm("\tnop");
}

__interrupt void ISR_ADC (void)
{
    PDR16 = ADCR0;   /* shows voltage on Port 0 ( LEDs )      */
    ADCS1 = 0xA2;           /* clear interrupt flag                  */
}
```

The above example demonstrates to configure ADC in the continuous mode with 8 bit conversion resolution with interrupts enabled. The maximum possible sampling and comparison time is used here. After every ADC interrupt the converted data is output to the LEDs connected to Port 16.

vectors.c

```
        SAMPLE CODE
        ------------------------------------------------------------------------
        --*/

        void InitIrqLevels (void)
        {
            . . .
            ICR59 = 30;      /* Priority Level 30 for ADC */

            . . .
        }

        /* ISR prototype */
        __interrupt void ISR_ADC (void);

            . . .

        #pragma intvect ISR_ADC 134       /* ADC */
            . . .
```

9 Additional Information

Information about CYPRESS Microcontrollers can be found on the following Internet page:

http://www.cypress.com/cypress-microcontrollers

The software examples related to this application note is:

91460_adc8-v10

91460_adc_rlt-v10

91460_adc8_dma-v14

91460_ppg_rlt_adc_dma-v10

91460_adc8_uart_async-v13

91460_adc10_dma_irq-v12

It can be found on the following Internet page:

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Document History

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**	—	NOFL	04/23/2008	V1.0, First draft, HPi
			09/01/2009	Corrected calculation of comparison time in chapter 2.2.4.1, MHz
*A	5115322	NOFL	04/04/2016	Converted Spansion Application Note “MCU-AN-300070-E-V11” to Cypress format
*B	5842144	AESATP12	08/02/2017	Updated logo and copyright.

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