AN205319

FR, MB91460, Hardware Watchdog

This application note describes the functionality of the Hardware Watchdog Timer and Watchdog Reset and gives some examples. The Watchdog is an up-counting Timer which has to be cleared in a given time interval. Otherwise a reset is performed. It can be used for restarting an application, if the program gets stuck.

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1 Introduction

This application note describes the functionality of the Hardware Watchdog Timer and Watchdog Reset and gives some examples.

The Watchdog is an up-counting Timer which has to be cleared in a given time interval. Otherwise a reset is performed. It can be used for restarting an application, if the program gets stuck.

1.1 Key Features

- RC oscillator as a Clock Sources (100kHz)
- Timer clear by writing 0 to HWWD: CL bit
- Timer stopped in Stop Mode and in Sleep Mode
- Software disabling is not possible
- Timer Interval : ~328ms to ~10486ms

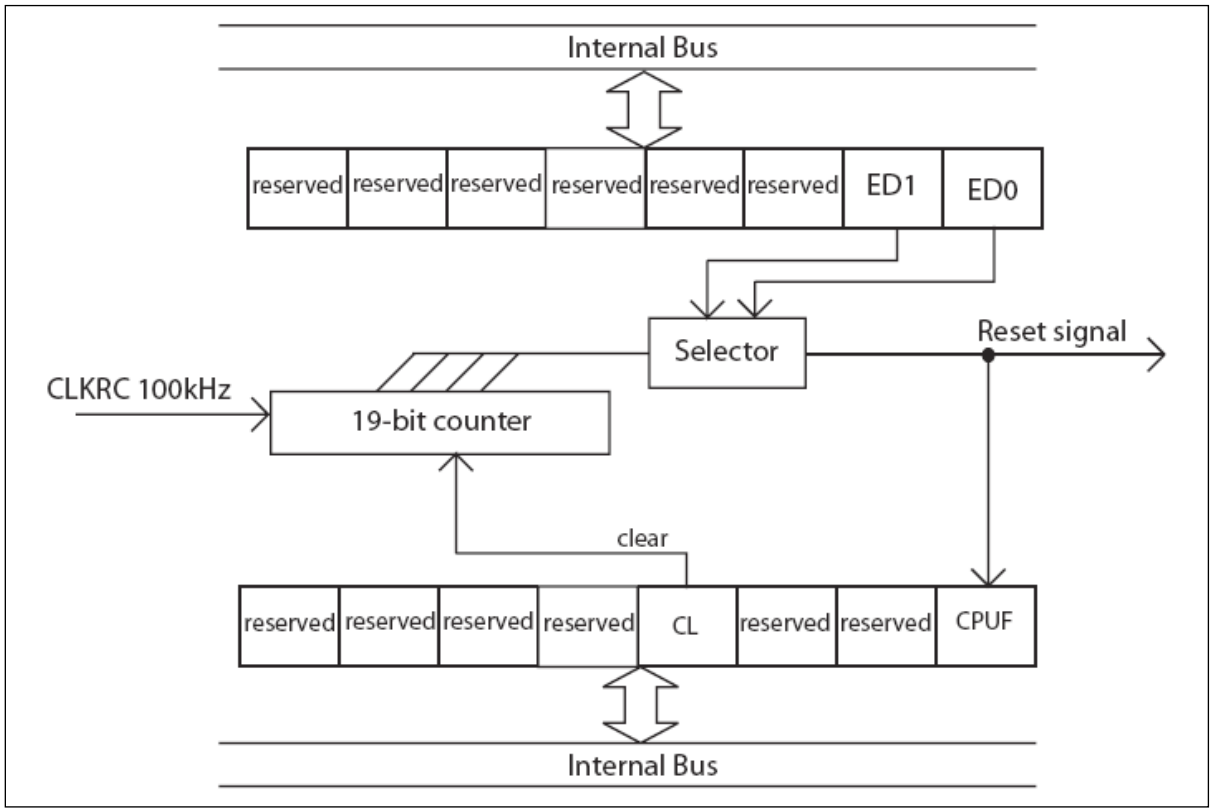
2 The Watchdog Timer

The basic functionality of the watchdog timer

2.1 Block Diagram

Figure 1 shows the internal block diagram of the Watchdog Timer.

Figure 1. Watchdog Timer block diagram



2.2 Registers

2.2.1 Hardware watchdog timer control and status register (HWWD)

Table 1. HWWD

Bit No.	Name	Explanation	Value	Operation
7,6,5	*RESV0*	*Reserved Bit*		Always write “0” to these bits
4	*RESV1*	*Reserved Bit*		Always write “1” to this bit
3	CL	counter clear	0	Watchdog timer is cleared
			1	No effect
2,1	*RESV0*	*Reserved Bit*		Always write “0” to these bits
0	CPUF*	CPU reset Flag	0	Watchdog reset not triggered
			1	Watchdog reset triggered (overflow of watchdog timer occurred)

*:- This bit is initialized by external reset input (INITX) or clock supervisor reset, but not by internal reset. Writing ‘0’ clears this bit, writing ‘1’ has no effect.

2.2.2 Hardware watchdog timer duration register (HWWDE)

Bit No.	Name	Explanation	Value	Operation
7 to 2	-	*Reserved Bit*		Always write “0” to these bits
1,0	ED1,ED0*	Elongate watchdog duration	00	The watchdog period is 2^{16} CLKRC cycles
			01	The watchdog period is 2^{17} CLKRC cycles
			10	The watchdog period is 2^{18} CLKRC cycles
			11	The watchdog period is 2^{19} CLKRC cycles

*:- The timer width is 19-bit. Since the RC oscillator is used as clock source of the hardware watchdog timer, the duration of the timer deviates with the RC oscillator accuracy

	ED1-0	Min	Typ	Max
RC Oscillator cycle (µS)		**5**	**10**	**20**
Watchdog Term (ms)	00	327.68	655.36	1310.72
	01	655.36	1310.72	2621.44
	10	1310.72	2621.44	5242.88
	11	2621.44	5242.88	10485.76

3 Watchdog Timer Examples

Examples for the watchdog

3.1 Timer Clear by writing CL bit

```
 /*                                  SAMPLE CODE                                  */
 /*-------------------------------------------------------------------------------*/

void main(void)
{
    . . .

    . . .

    while (1)
    {
       HWWD_CL = 0;  // Clear Watchdog Timer
       . . .
    }

    . . .
       }
```

3.2 Determining Watchdog Reset

```
  /*                               SAMPLE CODE                                   */
  /*-------------------------------------------------------------------------------*/
  void DetermineWtReset(void)
  {
  unsigned char reset_cause;

  reset_cause = HWWD;       // Read reset cause, also clear it

    if (reset_cause & 0x1)  // Is reset caused by watchdog overflow?
    {
           // Reset caused by watchdog overflow,
       // Take appropriate action
  }
  }
```

4 Important Notes

- Software disabling is not possible
- Hardware disabling is only possible on the evaluation device MB91V460
- In modes where the CPU does not work (SLEEP state, STOP state or STOP with RTC active state), the timer is cleared first then the counting is stopped.
- During DMA transfer between D-bus modules, the writing ‘0’ to CL bit is not possible. Thus, if the transfer time is more than 328ms (calculated from the fastest frequency of the RC oscillator as minimum period), a reset occurs.
- Unlike on MB91V460 Rev.A it is possible on flash devices to elongate the duration of the watchdog reset.
- Unlike on MB91V460 Rev.A it is possible on flash devices to change the CLKRC frequency to 2MHz. Even though the watchdog timer is always operated with a frequency of 100 kHz (10us) typical.
- After releasing INITX the hardware watchdog timer starts immediately without stabilization time. If the timer is not cleared periodically, setting initialization (INIT) reset occurs.
- If one of the below condition occurs, the watchdog counter is cleared
  - Writing “0” to CL bit in the HWWD register
  - Initialization Reset (INIT)
  - Operational Reset (RST)
  - Oscillation stops
  - Transition to the SLEEP state, STOP state or “STOP with RTC running” state

5 Additional Information

Information about Cypress Microcontrollers can be found on the following Internet page:

http://www.cypress.com/cypress-microcontrollers

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NOFL	05/06/2008	V1.0, First draft, HPi
*A	5090817	NOFL	04/12/2016	Converted Spansion Application Note “MCU-AN-300068-E-V10” to Cypress format
*B	5862837	AESATP12	08/24/2017	Updated logo and copyright.

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