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AN205318

FR, MB91460, Clock Monitor

The Clock Monitor is a module that outputs internal clock signals to a terminal to externally monitor them. The Clock Monitor provides a function to divide the frequency of a clock signal before it outputs to the terminal, thus allowing the clock signal to be used as an event at which external circuits act in synchronization with a MCU function.

Contents

1 Introduction....1
1.1 Key Features....1
2 Clock Monitor....2
2.1 Block Diagrams....2
2.2 Operation....2
2.3 Registers....3
3 Software Example....5
3.1 Basic Functionality of the Clock Monitor....5
4 Additional Information....5
Document History....6

1 Introduction

The Clock Monitor is a module that outputs internal clock signals to a terminal to externally monitor them. The Clock Monitor provides a function to divide the frequency of a clock signal before it outputs to the terminal, thus allowing the clock signal to be used as an event at which external circuits act in synchronization with a MCU function.

Not all devices are having this feature. Please refer datasheet of corresponding device to check availability of this function.

1.1 Key Features

- Divide an internal clock signal to output it to a terminal (MONCLK)
- Maximum frequency that can be monitored on a terminal (MONCLK) is 50MHz
- A dedicated MONCLK pin is available and no port function registers are required to set for enabling it.
- Division ratios: CLK/1, CLK/2, CLK/3, ..., CLK/16
- Programmable mark level (output “L” or “H” before enabling the clock output)
- Glitch free output enable

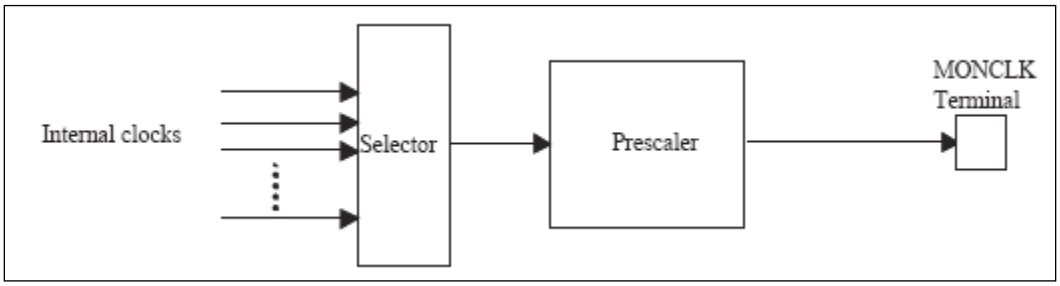
2 Clock Monitor

The basic functionality of the clock monitor is explained

2.1 Block Diagrams

Figure 1 shows the internal block diagram of a Clock Monitor.

Figure 1. Clock Monitor



2.2 Operation

Due to the glitch free switching mechanism it is necessary to follow these rules when switching the clock source (CMCFG3:0) or the pre-scalar ratio (CMPRE3:0):

- The CMPRE3:0 registers can only be written if the CMSEL3:0 registers are currently 0x00.
- The CMPRE3:0 registers can only be written if the CMSEL3:0 registers are written to 0x00 within the same write access.
- Between 2 write accesses to CMPRE/CMCFG there must be at least 2 cycles of the divided monitor clock.
- For changing the selector value, the MONCLK must be disabled.

2.3 Registers

2.3.1 Monitor Configuration Register (CMCFG)

This register selects output settings of an Internal Clock Signal

Table 1. CMCFG

Bit No.	Name	Explanation	Value	Operation
7,6,5,4	CMPRE3-CMPRE0	Select an output frequency prescaler	0000	Source clock (selected by CMSEL) divided by 1 (Initial)
			0001	Source clock (selected by CMSEL) divided by 2
			…	…
			…	…
			1110	Source clock (selected by CMSEL) divided by 15
			1111	Source clock (selected by CMSEL) divided by 16
3,2,1,0	CMSEL3-CMSEL0	Select a clock source	0000	MONCLK output disabled (high impedance) (Initial)
			0001	OSCMAIN
			0010	OSCSUB
			0011	CLKRC
			0100	CLKSUBRC
			0101	CLKMAIN
			0110	CLKSUB
			0111	CLKMOD
			1000	Clock modulator observer output*
			1001	PLL output after 1/g divider (Auto Gear)
			1010	PLL output after 1/m divider
			1011	CLKCAN
			1100	CLKPLLFB
			1101	CLKB
			1110	CLKP
			1111	CLKT

*Silicon evaluation purposes only, not available for customer applications.

2.3.2 Clock Source Configuration Register (CSCFG)

Table 2. CSCFG

Bit No.	Name	Explanation	Value	Operation for Channel *(2n+0)* or *(2n+1)*
7	EDSUEN	EDSU/MPU Enable	0	EDSU/MPU is (clock) disabled [Initial value]
			1	EDSU/MPU is (clock) enabled
6	PLLLOCK	PLL Lock	0	PLL is in the un-locked state
			1	PLL is in the locked state
5	RCSEL	CLKRC Selector	0	CLKRC is set to 100kHz [Initial value]
			1	CLKRC is set to 2MHz
4	MONCKI	Clock Monitor MONCLK inverter	0	MONCLK mark level is low [Initial value]
			1	MONCLK mark level is high
3	CSC3	Clock Source Selection for LCD Controller	0	LCD Controller is sourced by Sub Oscillator
			1	LCD Controller is sourced by RC Oscillator (100kHz)
2	CSC2	Clock Source Selection for Sub clock calibration	0	Sub clock Calibration is sourced by Sub Oscillator
			1	Sub clock Calibration is sourced by RC Oscillator(100kHz)
1,0	CSC1, CSC0	Clock Source Selection for RTC	00	Real Time Clock is sourced by Main Oscillator
			01	Real Time Clock is sourced by Sub Oscillator
			10	Real Time Clock is sourced by RC Oscillator(100kHz)
			11	Setting prohibited

3 Software Example

Example for Clock Monitor

3.1 Basic Functionality of the Clock Monitor

The following example sets clock source and clock divider.

```
/*                          SAMPLE CODE                                       */
/*----------------------------------------------------------------------------*/

void InitClockMonitor(unsigned char divider, unsigned char clk_source)
{
/* disable MonClk output */
       CMCFG = (CMCFG & 0xF0);
       while (CMCFG & 0x0F) {
 HWWD_CL = 0;
  }
/* Set Pre scalar value */
       CMCFG = (CMCFG & 0x0F) | (divider << 4);

 /* Enable MonClk output */
  CMCFG = CMCFG | (clk_source & 0x0F);
 }
```

Note: Maximum frequency that can be monitored on a terminal (MONCLK) is 50MHz

4 Additional Information

Information about Cypress Microcontrollers can be found on the following Internet page:

http://www.cypress.com/cypress-microcontrollers

The software examples related to this application note is:

91460_monclk

It can be found on the following Internet page:

http://www.cypress.com/cypress-mcu-product-softwareexamples

Document History

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**	-	NOFL	06/02/2008	V1.0, First draft, HPi
			06/03/2008	V1.1, Updated introduction and Key feature section, HPi
*A	5090796	NOFL	04/12/2016	Converted Spansion Application Note “MCU-AN-300067-E-V11” to Cypress format
*B	5842136	AESATP12	08/02/2017	Updated logo and copyright.

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