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AN205311

FR, MB91460, Reload Timer

This application note describes the functionality of the Reload Timer and gives some examples. The Reload Timer is a down counter which reloads its 16-bit timer value again on counter underflow (if the reload functionality is enabled).

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1 Introduction

This application note describes the functionality of the Reload Timer and gives some examples.

The Reload Timer is a down counter which reloads its 16-bit timer value again on counter underflow (if the reload functionality is enabled).

1.1 Key Features

- 16-bit Counter Value
- Output Frequency Range from 1.9 Hz to 4 MHz at 16 MHz Peripheral Clock
- Timer Interval Time from 125 ns to 263 ms at 16 MHz Peripheral Clock
- Prescaler Settings for Clock Divisions
- External clock and trigger selectable
- One-shot or Reload Counter Mode
- Interrupt Generation on Counter Underflow
- Timer Output
- Reload timer TOT0-TOT7 outputs are connected to the PPG0-PPG15 internal trigger inputs
- Reload timer TOT7 output is connected to the A/D converter 0 trigger input.

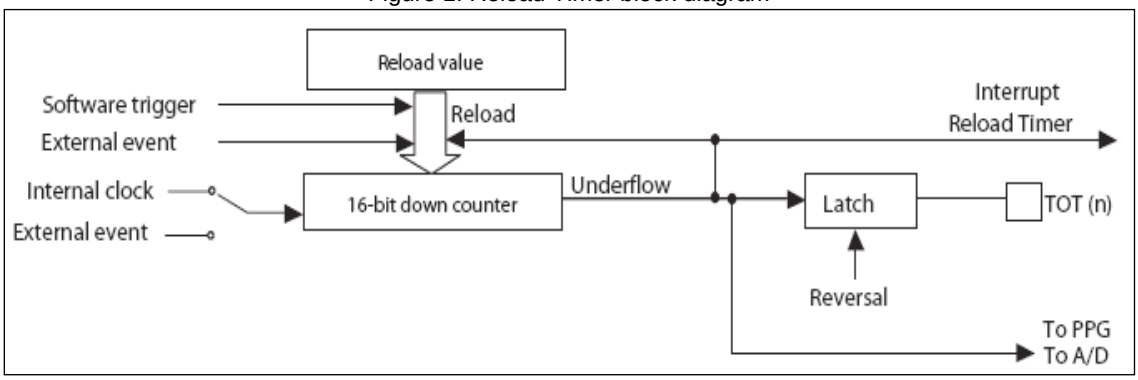
2 The Reload Timer

The basic functionality of the Reload Timer

2.1 Block Diagram

Figure 1 shows the internal block diagram of a Reload Timer channel.

Figure 1. Reload Timer block diagram



2.2 Registers

2.2.1 Timer Control Status Register (TMCSR)

This 16-Bit register controls the operation mode and interrupts for the reload timer.

Table 1. TMCSR

Bit No.	Name	Explanation	Value	Operation
15	-	*Undefined*	-	-
14	-	*Undefined*	-	-
13	-	*Undefined*	-	-
12, 11, 10	FSEL, CSL1, CSL0	Clock Division Control and Select	0, 0, 0	Clock = CLKP / 2^1
			0, 0, 1	Clock = CLKP / 2^3
			0, 1, 0	Clock = CLKP / 2^5
			0, 1, 1	External Event Count
			1, 0, 1	Clock = CLKP / 2^6
			1, 1, 0	Clock = CLKP / 2^7
9, 8, 7	MOD2, MOD1, MOD0	Mode Setting	*See tables below*	*See tables below*
6	-	*Undefined*		
5	OUTL	Output Level	0	Normal Output
			1	Inverted Output
4	RELD	Reload	0	One-shot Mode
			1	Reload Mode
3	INTE	Interrupt Enable	0	Interrupt Disabled
			1	Interrupt Enabled
2	UF	Underflow	0	Read: No underflow Write: Clear Underflow
			1	Underflow occurred
1	CNTE	Count Enable	0	Counter Disabled
			1	Counter Enabled
0	TRG	Trigger	0	No Effect
			1	Write: Trigger Counter

Mode Settings:

CSL0/1 = “00”, “01”, “10”

Table 2. TMCSR – Mode Settings

MOD2	MOD1	MOD0	Reload Trigger
0	0	0	Software trigger
0	0	1	External trigger (rising edge)
0	1	0	External trigger (falling edge)
0	1	1	External trigger (both edges)

CSL0/1 = “11”

Table 3. TMCSR – Mode Settings, CSL0/1 = “11”

MOD2	MOD1	MOD0	Count Trigger
0	0	0	-
0	0	1	External trigger (rising edge)
0	1	0	External trigger (falling edge)
0	1	1	External trigger (both edges)

2.2.2 16-Bit Reload Register (write) (TMRLR)

This 16-Bit register contains the reload value, which is set after counting underflow and reload function.

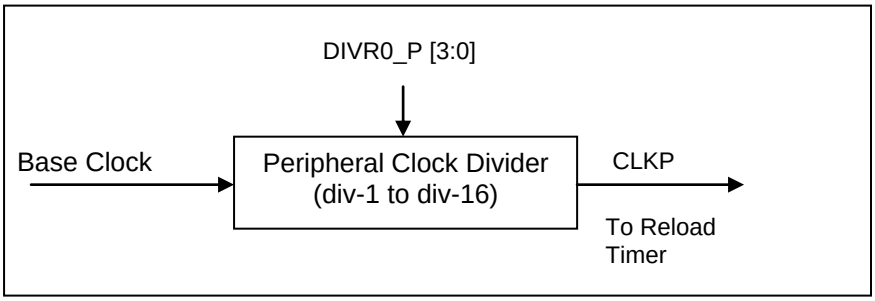
2.2.3 16-Bit Reload Register (read) (TMR)

This 16-Bit register contains the actual reload count.

2.3 Reload Timer Peripheral Clock

Please consider that the source clock frequency of the Reload Timer (CLKP) depends on the settings of the Clock Division setting register (DIVR0)

Figure 2. Reload Timer Clock



2.4 Operation Modes and Usage

This section describes various modes in which the 16-Bit Reload Timer (RLT) can operate.

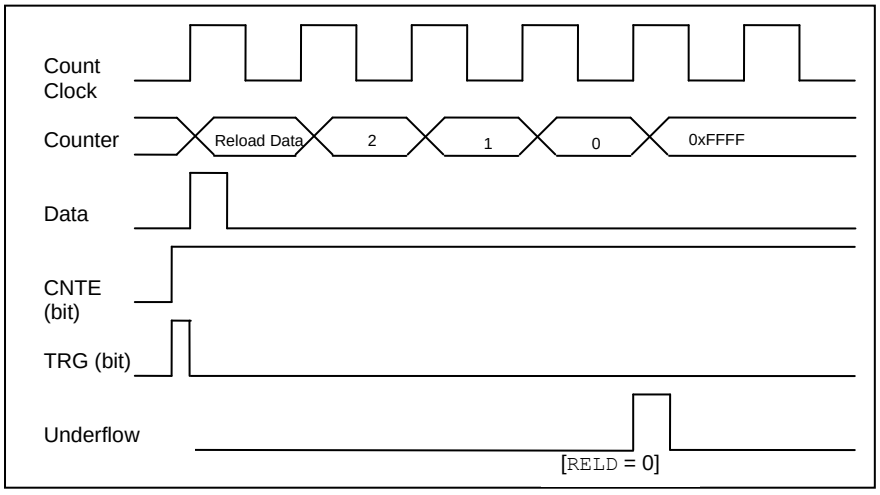
2.4.1 Interval Timer

The RLT can be used as an interval timer in one-shot mode or reload mode depending upon the setting of RELD bit of TMCSRn register. After the counter is enabled (TMCSRn:CNTE = 1) and triggered (TMCSRn:TRG = 1), the reload value is loaded from reload register to the counter and it starts counting. The counter decrements after every clock cycle of counter clock.

The counter decrements from 0 to 0xFFFF, if RELD bit of TMCSRn register is cleared to “0” or it decrements from 0 to the reload value, if RELD bit of TMCSRn register is set to “1”. In both the cases the underflow flag (TMCSRn:UF) gets set. If the INTE bit is "1" at this time, an interrupt request is generated.

The following figure describes the behavior of RLT in one-shot mode:

Figure 3. RLT as Interval Timer with RELD = 0

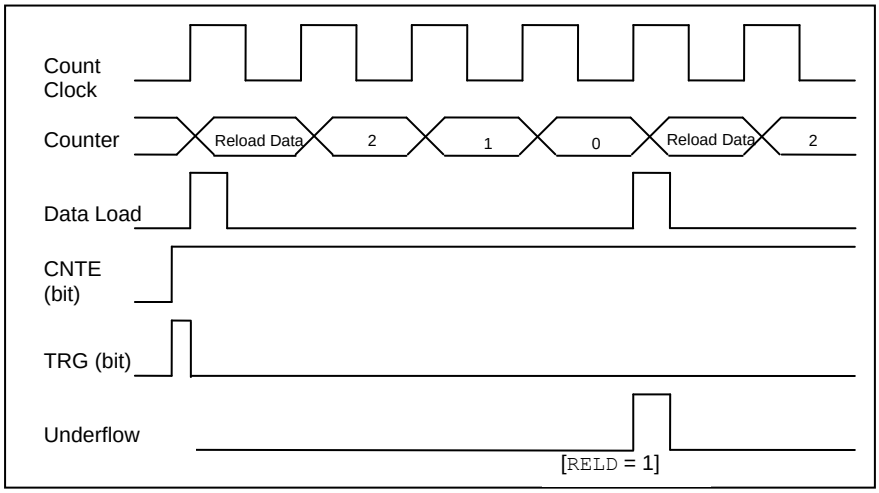


This mode can be used if an interrupt after specific interval is required.

The corresponding software examples are discussed in sections 3.1 and 3.2.

The following figure describes the behavior of RLT in reload mode:

Figure 4. RLT as Interval Timer with RELD = 1

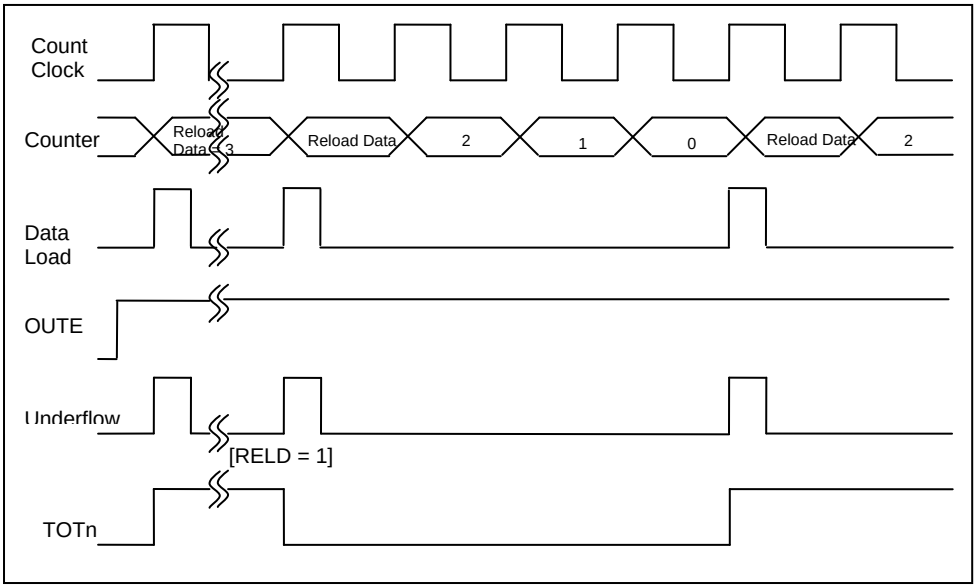


This mode can be used if periodic interrupts after specific interval is required.

2.4.2 Interval Timer with Output Function

The interval timer described in section 2.4.1 can also be used with TOTn output. TOTn output toggles after every underflow. Hence the frequency of this output equals half the frequency of the underflow interrupt.

Figure 5. RLT with TOTn Output in Reload Mode



The polarity of the TOTn output depends on OUTL bit of TMCSRn register. The following table describes the behavior:

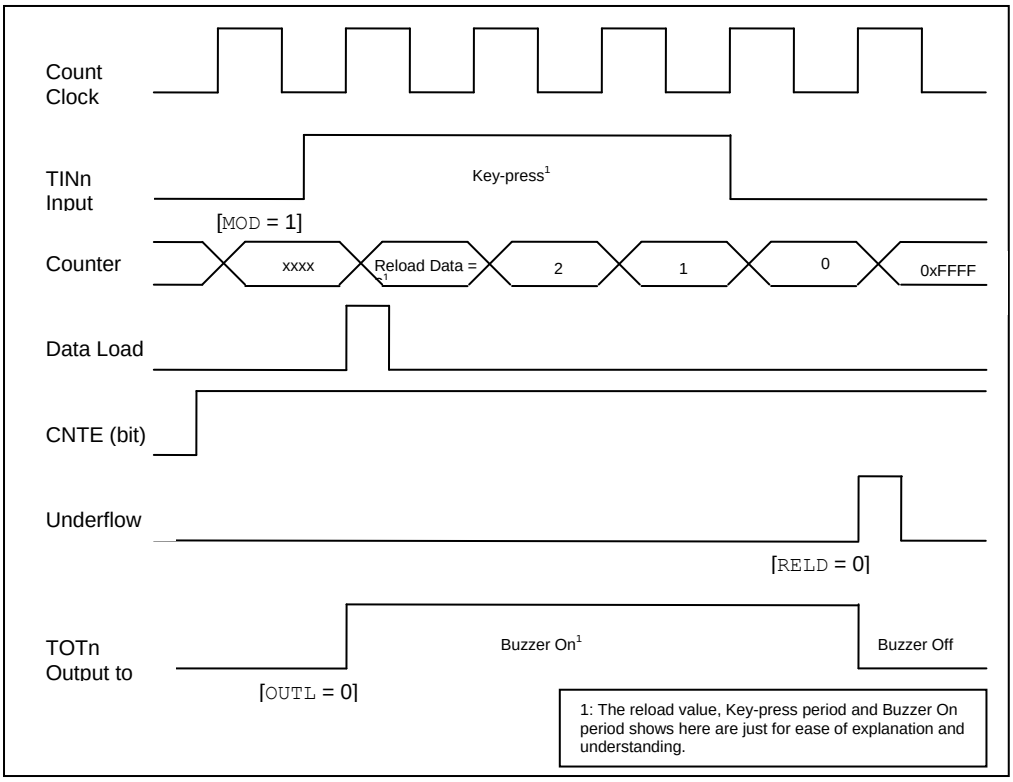
Sr. No.	OUTL	Condition	TOTn Output Status	
			One-shot Mode [RELD = 0]	Reload Mode [RELD = 1]
	0	Counter Enabled and triggered	1	0
		After First Underflow	0	1
		After Second Underflow	Not Applicable	0
	1	Counter Enabled and triggered	0	1
		After First Underflow	1	0
		After Second Underflow	Not Applicable	1

2.4.3 Timer with Trigger Input and Output Function

This mode operates exactly same as modes described in sections 2.4.1 and 2.4.2 except for the fact that the RLT is triggered by the signal on TINn input pin. In this case it is considered that trigger input edge is “Rising”. After the rising edge on TINn pin the reload value (3) is loaded in the counter and the counter starts counting.

This mode may be used for generating “Key-stroke Beeps”. If an application requires that each key-stroke / key-press on a key matrix is required to be acknowledged by a beep of the buzzer, then the key input can be fed to the TINn input (debounce of the key needs to be taken care separately) and the TOTn output can be fed to buzzer (amplifier circuitry may be required to drive the buzzer).

Figure 6. RLT with TINn as Trigger Input



Here the RLT is configured in trigger input mode with rising edge (TMCSRn: MOD[2:0] = 1). Hence if the key is pressed, positive edge would appear at the TINn input of the reload timer. This would load the reload value into the counter and the TOTn output is set to high (since the OUTL bit of TMCSRn register is configured as “0”) and in turn the buzzer would be turned on.

The reload value is dependent on the time of the beep. Once the required delay is expired the underflow flag would be set and the TOTn output would be cleared and hence the buzzer would stop beeping.

The corresponding software example is discussed in section 3.3.

Note: In order to use the TINn pin as an input, the corresponding port input must be enabled by setting the appropriate bit in the required PFRx and DDRx register.

2.4.4 Event Counter

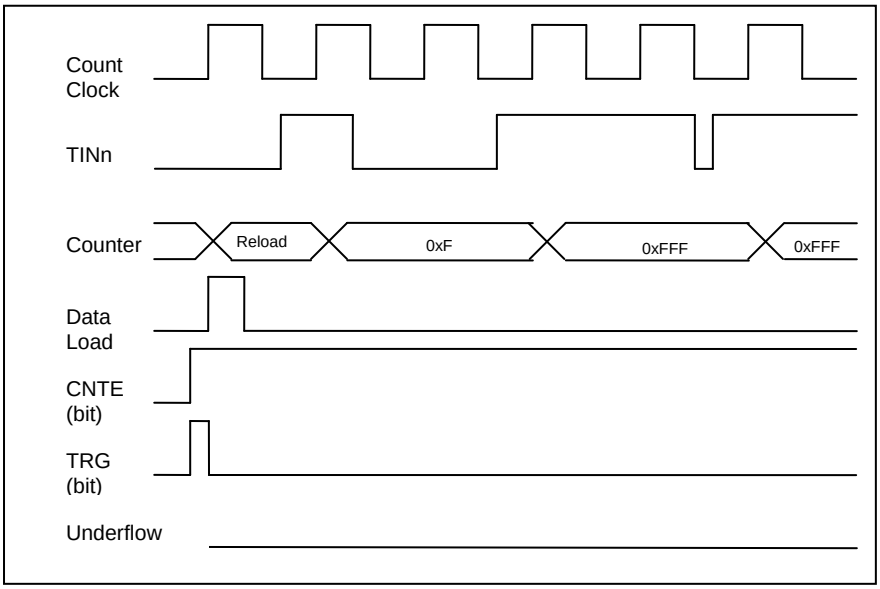
In this mode, TINn input is used as an external event input. The reload value is loaded in to the counter after the counter is enabled (TMCSRn:CNTE = 1) and triggered (TMCSRn:TRG = 1). However, the counter starts decrementing only when the active edge appears at input pin. This edge is configured by MOD[1:0] bits of TMCSRn register.

The pulse width of the input signal should be at least 2T (T: 1 cycle of peripheral clock CLKP) to the TINn pin.

This mode may be used for “Frequency Measurement”. The frequency of the signal is essentially number of cycles of the signal in the period of 1 second. Here two reload timers are used: one for generating 1 second delay (RLT0) and the other for counting the number of edges in this 1 second delay (RLT1).

The below diagram shows the operation of RLT1 only, which essentially counts the number of edges in the period of 1 second.

Figure 7. RLT with TINn as External Event Input



The RLT0 and RLT1 are triggered simultaneously. RLT0 is configured to generate a delay of 1 second. It is used as an interval timer in one-shot mode with interrupt. RLT1 is configured as event counter counting rising edges. RLT0 starts counting as soon as it is enabled and triggered. However RLT1 counter would decrement only after a rising edge appears at TINn input pin. The number of edges would be equal to the number of decrements of RLT1 counter.

After 1 second delay RLT0 underflow flag is set and interrupt is generated. In the RLT0 interrupt service routine, the both RLT0 and RLT1 are disabled. The frequency of the signal would be calculated as 0xFFFF – value of TMR1. It should be noted that the maximum measurable frequency here is 65535 Hz.

The corresponding software example is discussed in section 3.4.

Note: In order to use the TINn pin as an input, the corresponding port input must be enabled by setting the appropriate bit in the required PFRx and DDRx register.

2.5 Frequency Examples for TOTn Pin

The following table shows some frequency settings for the Reload Timer clocked by CLKP.

CLKP	CSL2, 0 Division	Reload Value TMRLR	Period Time	Period Frequency
16 MHz	2	0xFFFF	16.38 ms	61.03 Hz
		0x0000	250 ns	4 MHz
	8	0xFFFF	65.54 ms	15.26 Hz
		0x0000	1 µs	1 MHz
	32	0xFFFF	262.14 ms	3.81 Hz
		0x0000	4 µs	250 kHz
	64	0xFFFF	524.29 ms	1.91 Hz
		0x0000	8 µs	125 kHz
	128	0xFFFF	1.05 s	0.95 Hz
		0x0000	16 µs	62.5 kHz

The formula for the Reload Timer frequency f_{RLT} using f_{CLKP} (CLKP) as clock source is:

$$f_{RLT} = \frac{f_{CLKP}}{2 \cdot div_{FSEL} \cdot (R+1)}$$, where div_{FSEL} is the CSL2-0 division factor and R the Period Value

Important Note:

The frequencies and period times above are related to the Reload Timer output pins. If you use interrupts, the period time is as half as long and the frequency doubles.

3 Reload Timer Examples

Examples for Reload Timer Operation

3.1 Interval Timer with Output Function and without Interrupts

The following example shows how to set up the Reload Timer 0 for operation without interrupts.

```
/*                        SAMPLE CODE                                          */
/*-------------------------------------------------------------------------------*/

void InitReloadTimer0(void)
{
    TMRLR0 = 0x1F3F;            // set reload value
    TMCSR0 = 0x0013;            // pre-scalar 1:2
}
```

The example outputs a frequency of about 500 Hz at the TOT0 pin using 16 MHz Peripheral Clock (CLKP).

3.2 Interval Timer with Output Function and Interrupts

Setting the INTE-Bit enables interrupts for the Reload Timer. An interrupt occurs, if an underflow of the timer is detected. The interrupt is cleared by setting the UF-Bit to “0”.

```
/*                             SAMPLE CODE                                     */
/*-------------------------------------------------------------------------------*/

void InitReloadTimer0(void)
{
    TMRLR0 = 0x1F3F;       // set reload value
    TMCSR0 = 0x001B;       // prescaler 1:2, interrupt enable
}

 __interrupt void ReloadTimer0 (void)
 {
     TMCSR0_UF = 0;        // reset underflow interrupt request flag
 }
```

The example outputs a frequency of about 500 Hz at the TOT0 pin using 16 MHz Peripheral Clock (CLKP). Therefore interrupts are generated in periodic interval of 1 ms.

Please note, that the corresponding interrupt vector and level has to be defined in the *vectors.c* module of our standard template project.

```
/*                             SAMPLE CODE                                     */
/*-------------------------------------------------------------------------------*/

void InitIrqLevels(void)
{
  ICR08 = 20;     /* Reload Timer 0               */
                  /* Reload Timer 1               */
}
   . . .

__interrupt void ReloadTimer0(void);    // Prototype

   . . .

#pragma intvect ReloadTimer0       32     // RLT0 of MB91467D Series
```

3.3 Timer with Trigger Input and Output Function

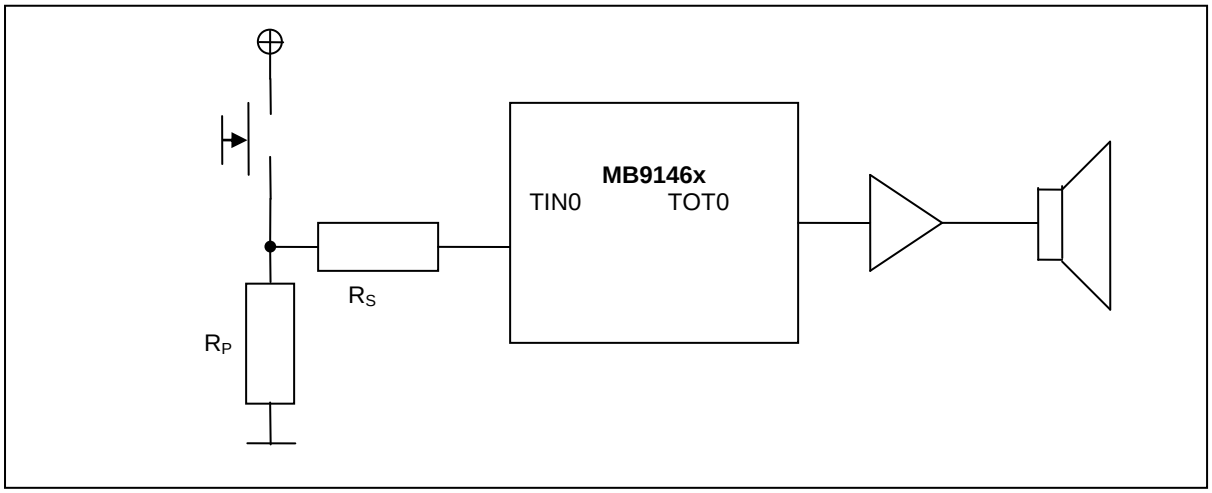
The following software example demonstrates to configure the RLT0 on MB91467D Series with Trigger Input and Output Function in order to generate the “Key-stroke Beeps” as explained in the section 2.4.3. After every key press the buzzer would beep for 100 ms.

The CLKP is considered as 4 MHz after the divider of 64 the RLT0 clock would become 62.5 kHz. The reload counter of RLT0 is set to a value equal to 0x1869. Hence the period for the TOT0 output would stay high after the rising edge at TIN0 for 100 ms (1/62.5 kHz * (0x1869 + 1)). Here RLT0 is configured in one-shot mode and TOT0 output would stay high while the count is in progress (i.e. till underflow). After the underflow the output would be cleared and the buzzer stops beeping.

```
/*                                  SAMPLE CODE                                  */
/*-------------------------------------------------------------------------------*/

void InitReloadTimer0(void)
{
    TMRLR0 = 0x1869;    // set reload value = 6249
    PFR14_D0 = 1;       // enable TIN0 input pin
    PFR15_D0 = 1;       // enable TOT0 output pin
    EPFR15_D0 = 1;
    TMCSR0 = 0x1483;    // pre-scalar 1:64, trigger input-rising edge, output
                        // enable, count enable, trigger
}

void main(void)
{
   InitReloadTimer0();

         while(1);
      }
```

The below figure depicts the connection diagram corresponding to the above code:

Figure 8. Connection Diagram for Keystroke Beeps



In the above figure R_P is the pull-down resistor to limit the current once the key is pressed where as R_S is the series resistor to limit the input current and also to filter the noise. The TOT0 output can be fed to the buzzer via an amplifier as shown above.

3.4 Event Counter

The following software example demonstrates to configure the RLT1 as an event counter and RLT0 as an interval timer on MB91467D Series in order to “measure frequency” as explained in the section 2.4.4.

TIN1 is used as external event input. The counter decrements at every edge of the signal appearing on TIN1 input (of which the frequency is to be measured).

The CLKP is considered as 4 MHz after the divider of 64, the RLT0 clock would become 62.5 kHz. The reload counter of RLT0 is set to a value equal to 0xF423. Hence the underflow interrupt of RLT0 would occur after 1 second (1/62.5 kHz * (0xF423 + 1)). By that time the counter of RLT1 would have decremented by the number of edges at TIN1 input. In the RLT0 interrupt service routine the frequency of the signal is calculated as 0xFFFF – TMR1.

```
/*                                  SAMPLE CODE                                 */
/*------------------------------------------------------------------------------*/

void InitReloadTimer0_1(void)
{
    TMRLR0 = 0xF423;    // set reload value = 62499
    TMRLR1 = 0xFFFF;    // set event counter value

    PFR14_D1 = 1;       // enable TIN1 input pin

    TMCSR0 = 0x140B;    // pre-scalar 1:64, count enable, interrupt enable,
                        // trigger
    TMCSR1 = 0x0C83;    // External count mode, event input, rising edge,
                        // count enable, trigger
}

unsigned int Frequency;

void main(void)
{
   InitReloadTimer0_1();

   while (1);
}

__interrupt void ReloadTimer0 (void)
{
    TMCSR0_UF = 0;              // reset underflow interrupt request flag
    Frequency = 0xFFFF - TMR1;  // calculate frequency
    TMCSR0_INTE = 0;            // disable interrupts
}
```

Also note that the pulse width of signal appearing on TIN1 should be at least 2 times the CLKP (i.e. 0.5 µs at 4 MHz CLKP).

Please note, that the corresponding interrupt vector and level has to be defined in the *vectors.c* module of our standard template project.

```
/*                                SAMPLE CODE                                   */
/*------------------------------------------------------------------------------*/

void InitIrqLevels(void)
{
  ICR08 = 20;     /* Reload Timer 0               */
                  /* Reload Timer 1               */
   // Reload Timer 0 of MB9634x Series
}
   . . .

__interrupt void ReloadTimer0(void);    // Prototype

   . . .

 #pragma intvect ReloadTimer0      32  // RLT0 of MB91467D Series
```

4 Additional Information

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The software examples related to this application note is:

91460_rlt-v12

91460_rlt_irq-v12

91460_rlt_event_counter

91460_adc_rlt

91460_ppg_rlt_adc_dma

It can be found on the following Internet page:

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Document Number:002-05311

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**	-	NOFL	03/26/2008	V1.0, First draft, HPi
			04/24/2008	V1.1, Typo in title page corrected, MSt
*A	5088846	NOFL	04/06/2016	Converted Spansion Application Note “MCU-AN-300060-E-V11” to Cypress format
*B	5842098	AESATP12	08/02/2017	Updated logo and copyright.

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