AN205217

Declaration to handle the Clock Modulator

This application note describes about handling clock modulator by changing PLL settings.

1 Introduction

This application note describes about handling clock modulator by changing PLL settings.

2 Declaration regarding handling clock modulator by changing PLL settings

The delay line of the clock modulator is specified for frequencies between
16 MHz and 48 MHz.
Is the input frequency of the delay line outside these limits then glitches
could appear at the output clock of the delay line.
These glitches are caused by the wrong calibrated delay line.
The delay line is calibrated always after the clock modulator is switched
On even if the automatic calibration is enabled.
The automatic calibration will be active configurable time intervals. Is
the clock modulator not changed and the input frequency changed then the
clock modulator runs with a non-calibrated delay line till the next
automatic calibration is activated.
This would lead quite sure to a crash of the application.
Because always switch off clock modulator first and then change PLLsettings.

3 Document History

Document Title: AN205217 - Declaration to handle the clock modulator

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NOFL	05/31/2001	Initial release
*A	5226377	NOFL	04/18/2016	Migrated Spansion Application Note MCU-AN-391020-E-V10 to Cypress format
*B	5843053	AESATP12	08/03/2017	Updated logo and copyright.

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