AN205209

FR Family 460 Series Hardware Set Up

This application note describes how to set up a hardware environment for Cypress FR 460 series MCUs.

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1 Introduction

This application note describes how to set up a hardware environment for Cypress FR MCUs. As an example the MB91F467DA is used.

1.1 Abbreviations

MCU Microcontroller

DECAP Decoupling Capacitor

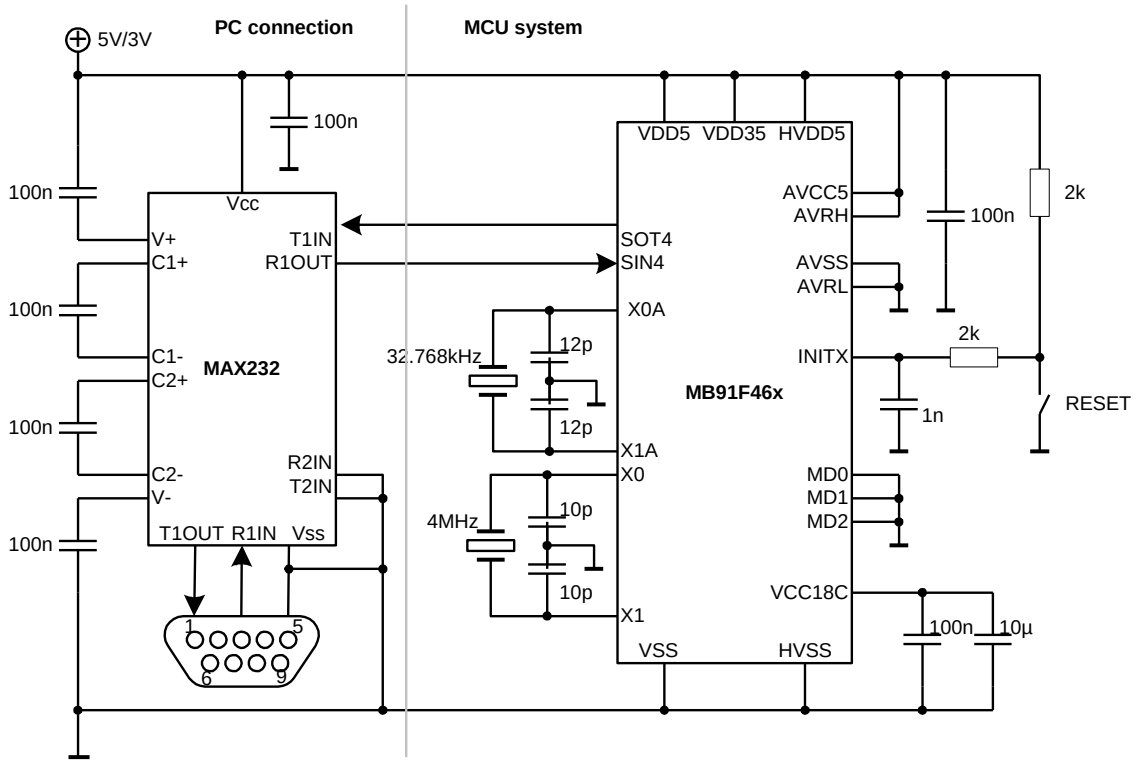
2 Minimal System

This Chapter gives an Example of a Minimum Hardware System

2.1 Schematic

The following graphic shows a schematic of a minimum hardware system. Note that for other MCU families a different pinning is needed.

Below is an example of an asynchronous serial programming interface for single chip mode:



2.2 Serial Interface

The “PC connection” section is only needed, if no 5V external serial data lines for programming are existing. The MAX232 is a standard level shifter, which converts the 5V levels of the MCU to ±12V RS232V24 levels and vice versa.

If you use a 3.3V MCU a MAX3232 is recommended.

Please consider, that the internal charge pumps of the level shifter can produce noise on the +5 Volts line, which can influence the ADC, if AVCC and AVRH are directly (unfiltered) connected to it.

Note: It may be in case of external noise at SCK4 pin that the synchronous programming interface will be initialized instead of asynchronous interface. Make sure that the level at SCK4 pin is stable during the initialization of Flash loader.

Power supply

The power supply should be 5 Volts ±10% for normal usage. If a different supply voltage is used please refer to the MB91460 data sheet.

2.3 Analog Digital Converter Supply Pins

The analog converter supply pins (AVCC, AVSS, AVRH, AVRL) should be connected even if the ADC of the MCU is not used.

2.4 Analog Input Pins

Because the ADC works with an internal sample capacitor the input impedance and external capacity must be low. Cypress recommends an input impedance of not more than 15k Ohm. Choose the external capacity as low as possible (about 1 nF for EMI protection).

2.5 Reset Pin (INITX)

To reset the MCU a switch connects this pin to VSS (Ground). Additionally a capacitor has to be connected between VSS and the reset pin for debouncing the switch and for EMI protection. From experience Cypress recommend a capacity of not more than 1 nF (COG). This capacity covers the most common frequency protection in a wide range. Higher capacities and high impedance may cause latch-up effects together with an INITX-switch and low EMI protection.

If the device has no internal pull-up resistor, an external pull-up resistor should be connected.

2.6 VCC18C Pin

A 4.7µF...10µF (ceramics X7R) capacitor *must* be connected to the C pin of the MCU. This smooth capacitor is needed to stabilize the internal 1.8V core supply. Otherwise the MCU may not operate correct or will be damaged in worst case. Please refer to the DS regarding the specified capacitance value. Also see chapter 3.

2.7 Clock Source

A clock source must be provided to the MCU. Therefore crystals or external clock signals can be used. For external source pin X0 (X0A) is used whereby pin X1 (X1A) is not connected.

Note: If the sub clock oscillator is not used, connect the X0A pin to ground and leave the X1A pin open.

Please also refer to the chapter *Introduction/Precautions for Device Handling* in the corresponding hardware manual for details.

2.8 Mode Pins

The mode pins signalize the MCU the current operation mode. For a single chip system the mode pins MD2-0 should be connected directly to GND. To avoid entering test mode due to noise, use a short trace length between each mode pin on printed board and VDD or VSS to connect pins at low impedance.

Table 1. Mode pin settings for available operation modes

MD0	MD1	MD2	Operation mode	Behavior of IO ports after Reset
0	0	0	Single chip Internal vector mode	All IO port as HIZ excepted SIN4,SOT4,SCLK4 and external bus interface
1	0	0	External vector mode *1)	External bus interface is activated
1	1	1	Parallel programming mode	Flash programming interface is activated

Note: *1) The Bootloader is only available for the Internal vector mode MD[210]=000. Hence, the programming of external Flash via Bootloader will be not supported by external vector mode. For this reason the MD0 pin should be connected to a test point with pull-up resistor to jump into the Bootloader.

2.9 Unused IO Pins

Please read Chapter 4 for how to proceed with unused (not connected) pins.

An unused pin must be terminated by a pull-up / pull-down resistor externally, or by switching on the internal pull-up or pull-down resistor before enabling the port inputs (PORTEN bit) to avoid transverse current.

3 Layout and Electromagnetic Compatibility

This Chapter Gives Some Tips For Layout Design

3.1 General

To avoid ESD problems and noise emission of the system some rules for the layout design has to be observed.

The most critical point is the C pin because this is the connection to the internal 3.3V supply for the MCU core. Thus a decoupling capacitor has to be placed very near to this pin.

Also the ground and VDD routing has to be done carefully. VDD lines should be routed in star shape. We recommend a VSS ground plane *on the mounting side* just under the MCU. For both VDD and VSS only *one* connection to the rest of the circuit should be done, otherwise noise is carried-over from and to the MCU. Decoupling capacitors (DeCaps) has to be placed as nearest as possible to the related pins. If they are placed too far away their function becomes useless.

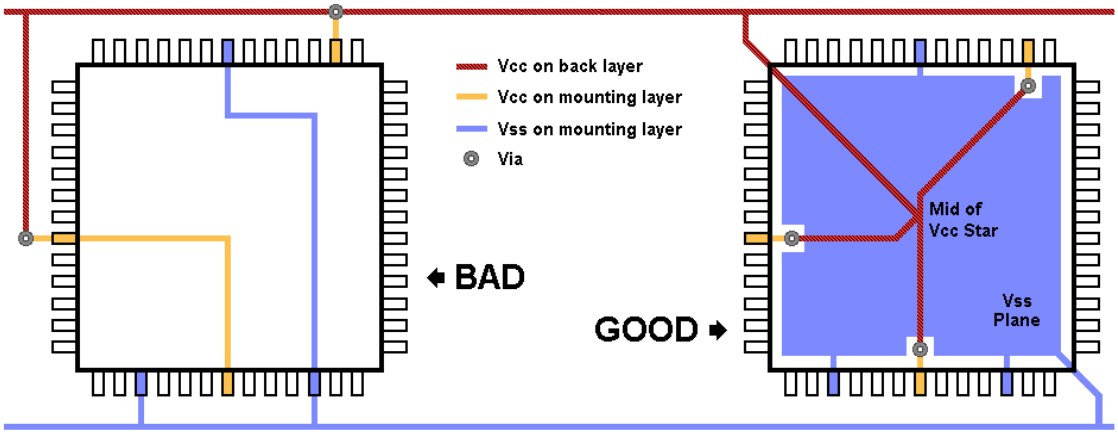
If crystals are used, they have to be placed as nearest as possible to the X1(A) pins.

If possible all decoupling capacitors should be placed on the same mounting side as the MCU.

3.2 Power Line Routing

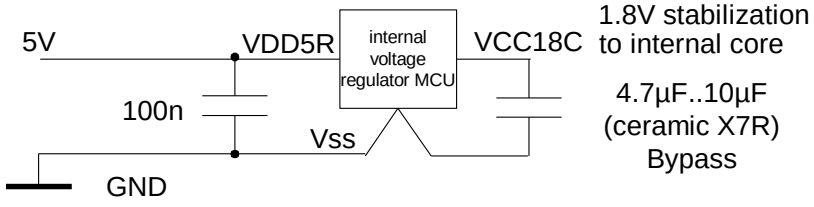
In general the VDD and VSS lines should not be routed in “chains”, but in “star shape”. For VSS a ground plane is recommended which covers the chip package, and is connected in *one* point to VSS of the whole circuit.

Below is a example of a bad and a good power line routing:



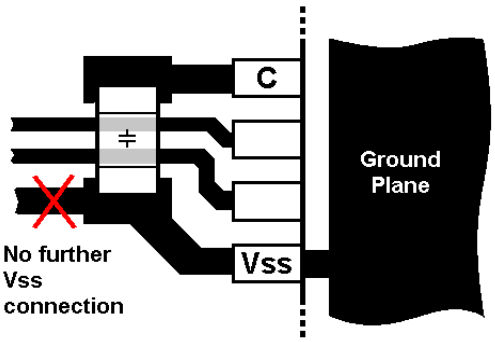
3.3 C Pin bypass capacitor

The following example shows the recommended connection for VDD5R/VSS and VCC18C.



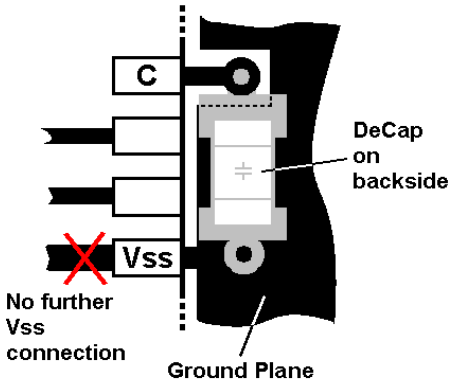
Note: To reduction of EMI noise, the Bypass capacitor should be connected at first to VSS5 and then with the GND plane. Anyway the feedback line of Bypass capacitor should be routed through VSS pin.

The following routing and placement for single sided metal layer is recommended (Note, that in all following illustrations the mounting metal layer is drawn in black and the back side metal layer in gray):



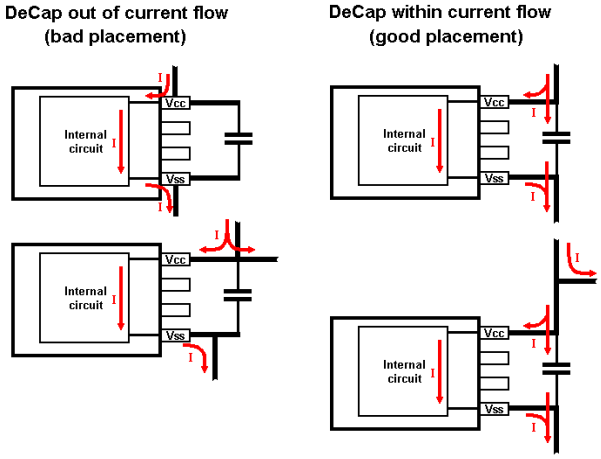
Please use 4.7µF …10µF capacitor (ceramic X7R), the capacitance value depends on the used max. PLL speed.
Please refer to the DS

The following routing and placement for double-sided metal layer is recommended. Note, that despite the capacitor is placed on the opposite side as the MCU, this solution is the best.

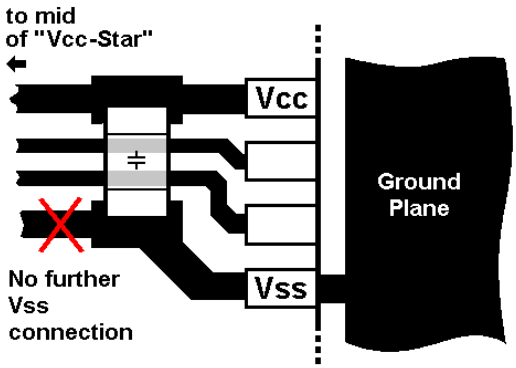


3.4 Power Supply Decoupling

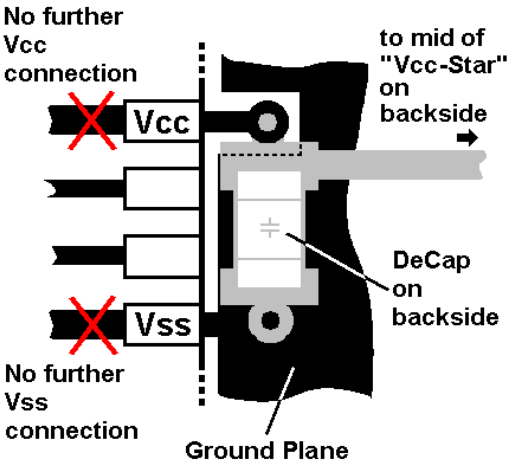
DeCaps for power supply have to be placed within the “current flow”. Otherwise they are senseless, because then their function become inoperable. The following graphic illustrates this:



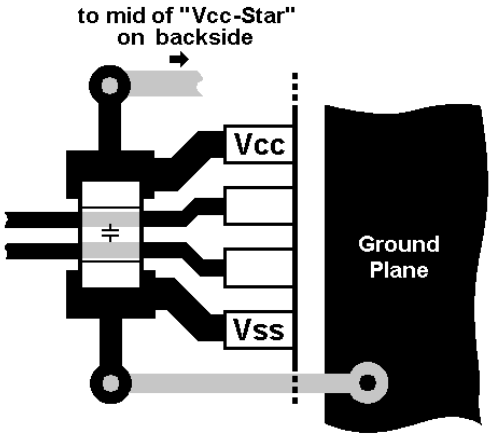
The following routing and placement for single sided metal layer is recommended:



The following routing and placement for double-sided metal layer is recommended. Note, that despite the capacitor is placed on the opposite side as the MCU, this solution is the best like for the VCC18C pin.



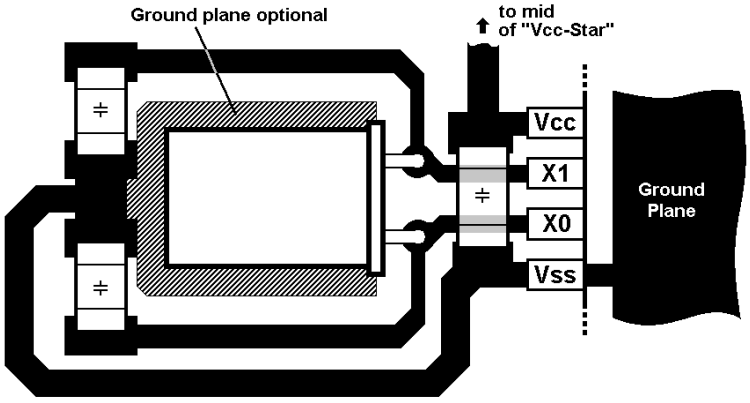
If mounting on both sides is not possible the following placement and routing is recommended:



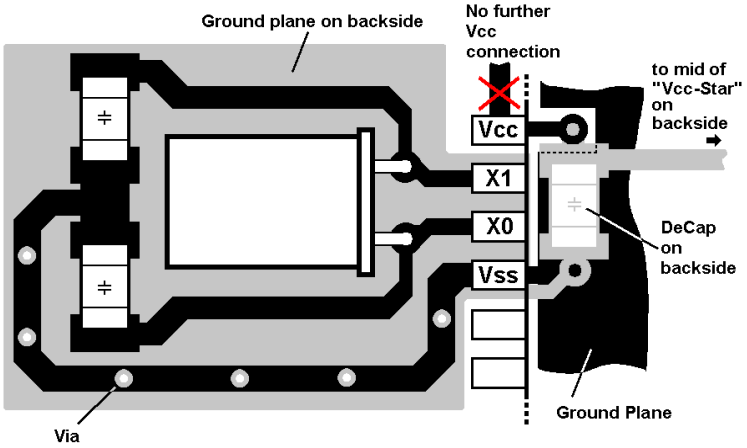
3.5 Quartz Crystal Placement and Signal Routing

The crystal has to be placed as nearest as possible to the MCU. Therefore the oscillator capacitors have to be placed “behind” the crystal.

For single metal layer circuit board the following placement and signal routing is recommended:



For double sided metal layer layout the following is recommended:



3.6 Other documents

For further detailed information please refer to the application note 32*bit-EMC-Guideline* or MCU device specific EMI Report.

3.7 MCU Pin Summary

The following table shows the EMC critical pins and gives short information about how to connect them.

Pin name	Function
VDD5	Main supply for IO buffer, crystal oscillator
VDD35	Main supply for external Bus buffer at 5V or 3.3V level
VDD5R	Main supply for the internal 1.8V regulator. Note, this pin shows the noise of the internal core supply.
VSS5	Main supply for IO buffer and MCU core, close to the internal 1.8V regulator, close to crystal oscillator
VCC18C	External smooth capacitor for internal 1.8V regulator output, it is used for supply of the MCU core. Note, this pin leads the most of noise
AVCC*	Power supply for the A/D converter
AVSS*	Power supply for the A/D converter
AVRH* AVRL*	Reference voltage input for the A/D converter
HVDD5*, HVSS5*	Power supply for the SMC (high current) outputs, it is not connected to VDD, should be connected to extra power supply
X0, X0A*	Oscillator input, if not used so shall be connected to ground (see please DS of related MCU series)
X1, X1A*	Oscillator output, the crystal and bypass capacitor must be connected via shortest distance with X1 pin, if not used so shall be open

*only if supported by device

4 Port Input / Unused Pins / Latch-up

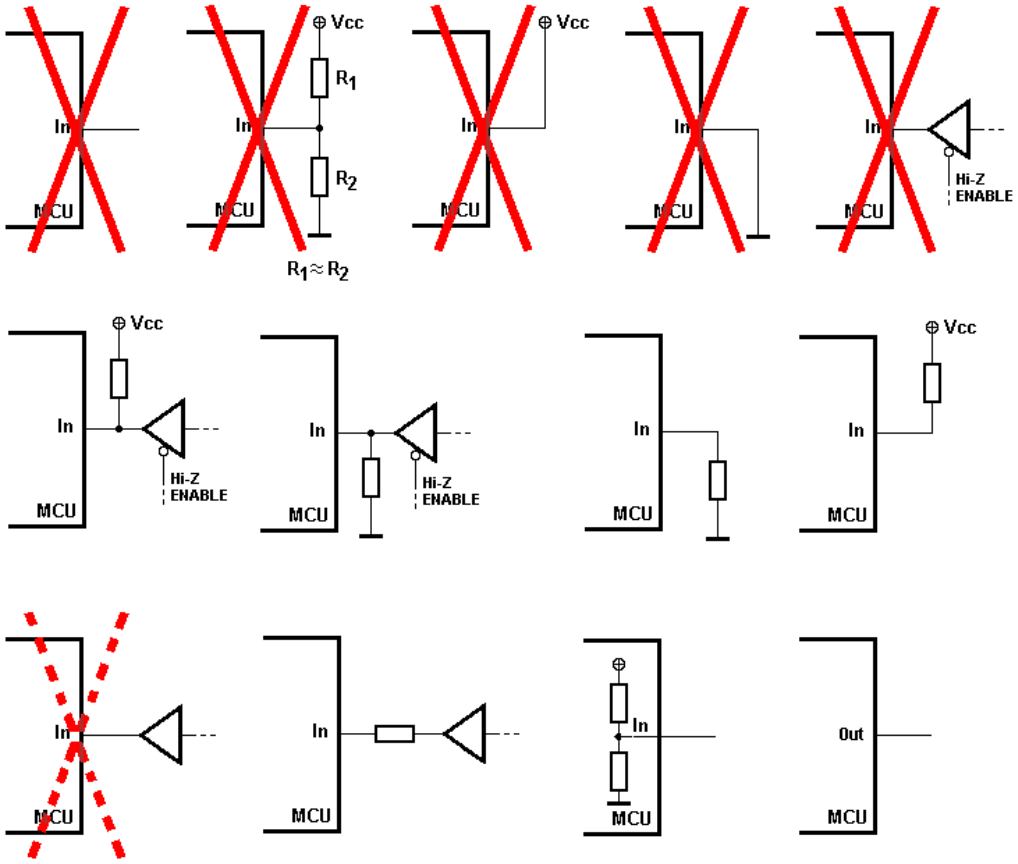
How to Connect Input Port Pins and How to Proceed With Unused Pins

4.1 Port Input / Unused Pins

It is strongly recommended to do not leave Input Pins unconnected. In this case those pins can enter a so-called *floating state*. This can cause a high I_{CC} current, which is adverse to low power modes. Also damage of the MCU can happen.

Use the internal pull-up/down resistors, if the port provides such function. If not, use external pull-up or pull-down resistors to define the input-level. If both solutions are not possible, set the Port Pin to Output.

Never connect a potential divider with almost same resistor values.



Be careful with connection of input pins to other devices, which can go into High-Z states. Always use pull-up or pull-down resistors in this case.

Outputs from external circuits should always be connected via a serial resistor to a MCU input pin.

Debouncing and decoupling capacitors should always be chosen as smallest as possible. Please refer to chapter 4.2.

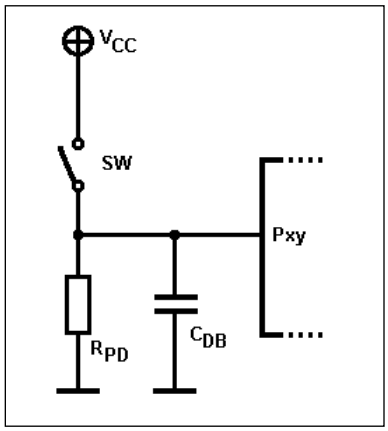
All pins are set to input HiZ after its power-on default. Therefore set unused pins to input with internal pull-up/down resistor, or provide them with pull-up or pull-down resistors.

Do not connect any input ports directly to VDD or VSS (GND)! Always use pull up or down resistors (2k … 4k Ohms). If available it is possible to use the internal pull up or pull down resistors as well. Please note the value internal resistors can be 20k … 100k depends on the device and temperature.

4.2 Latch-up consideration (switch)

Be careful with external switches to VDD or ground together with debouncing capacitors connected to port pins.

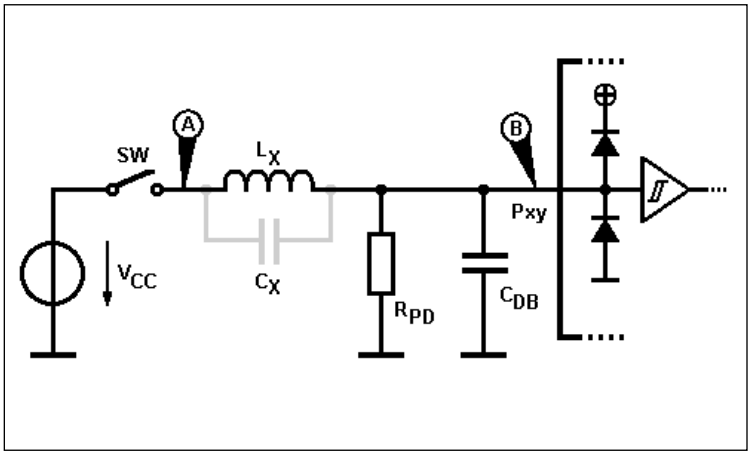
A usual configuration is shown in the following schematic:



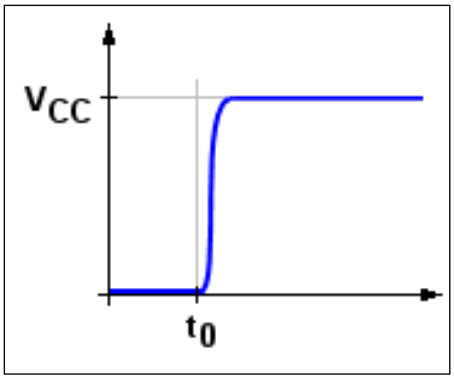
R_{PD} is a pull-down resistor and C_{BD} a debouncing capacitor. If the switch SW is open, a “0” is read from the port pin Pxy. If the switch is closed the input changes to “1”.

From the physical aspect, it has to be considered, that the switch is often placed in distance to the MCU by cable, wire, or circuit path. The longer the circuit path is the higher will be its inductivity L_X (and capacity C_X).

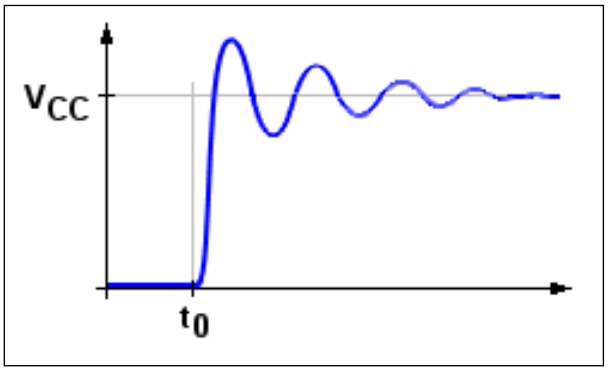
An equivalent circuit diagram looks like the following illustration:



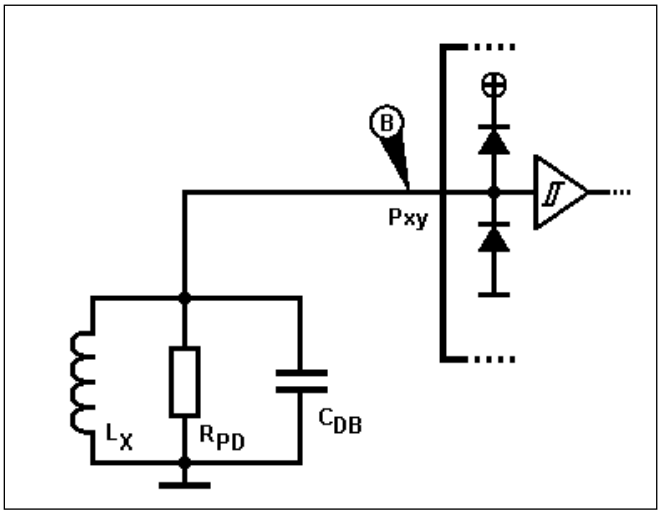
By closing the switch SW at time t_0 the following voltage can be measured at point (A):



But at the port pin Pxy on point (B) the following voltage can be measured:

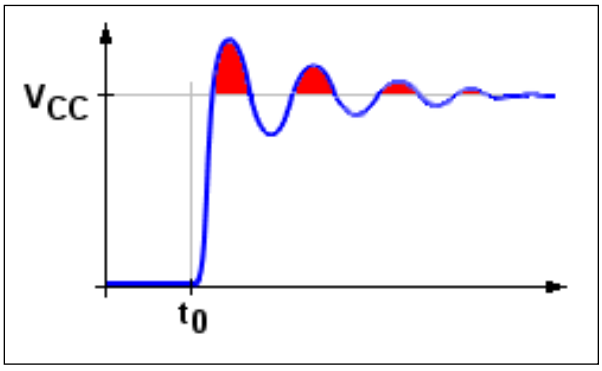


By closing the switch SW the circuit becomes a parallel oscillator with the wire-inductivity L_X, the debouncing capacity C_X and the damping R_{PD} of the pull-down resistor (Assume the power supply to be ideal, i. e. it has no internal resistance):



Because R_{PD} is often chosen high (> 50 K Ohms), its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin, drawn in red in the illustration below:



These overshoots may cause an internal latch-up on the port pin, because the internal clamping diode connected to VDD becomes conductive. Similar is the effect, if the switch SW is opened. In this case there are under shoots on the port pin.

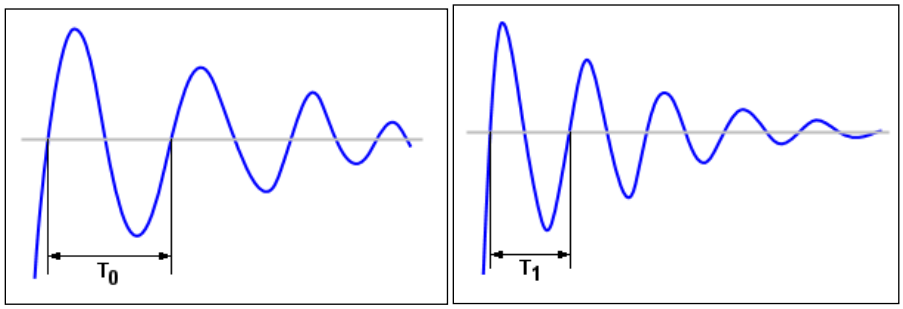
The frequency of the oscillation can be calculated by

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}} .$$

The inductivity L_X is the unknown value and depends on the PCB, its routing, and the wire lengths.

There are two counter measurements to prevent from latch-up.

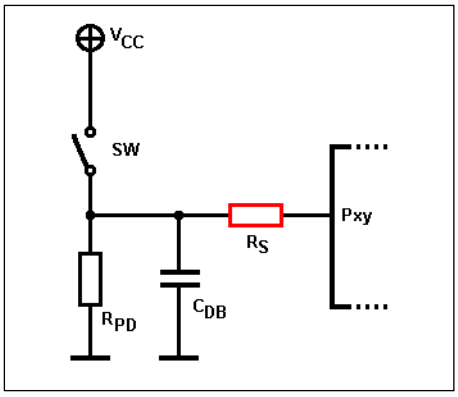
One solution is to decrease the capacity of the debouncing capacitor. This increases the oscillation frequency, and the over-all energy of the overshoots is smaller.



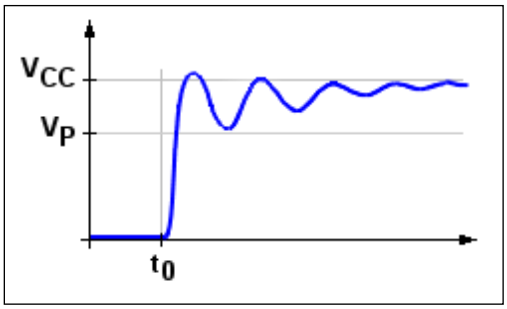
"big" capacity "small" capacity

This solution has two disadvantages: First the debouncing effect decreases and second, there is no guarantee, that the latch-up condition is eliminated.

A better solution is to use a series resistor at the port pin like in the following schematic:



The series resistor R_S reduces the amplitude of the oscillation and decreases the voltage offset at first. The resistor must not be chosen too high, so that the port pin input voltage V_P is within the positive CMOS/TTL/Automotive level.



5 Minimum Flash Programming Connection

This Chapter Shows Which Connections Are Needed For Programming

5.1 Internal vector mode and Programming via BootROM

When using a target board, which normally operates in single vector mode, the mode pins of the MCU has to be set to MD2-0 = 0. It is possible to jump to serial programming mode via the BootROM.

When the device does not start from an INITX (external power-on reset) or the bootloader is disabled (boot security vector), the boot loader cannot be started.

If the boot security vector is not valid the Boot-ROM enters a short check loop in order to verify the actual boot-conditions. This is the reception of character 'V' from the internal UART4 at 9600 Baud (serial trigger). But at first the boot loader is scanning for a falling edge at SCK4. If falling edge is detected at SCK4, the serial interface will be initialized for synchronous communication.

5.2 Programming Pins

For serial programming the following pins are affected:

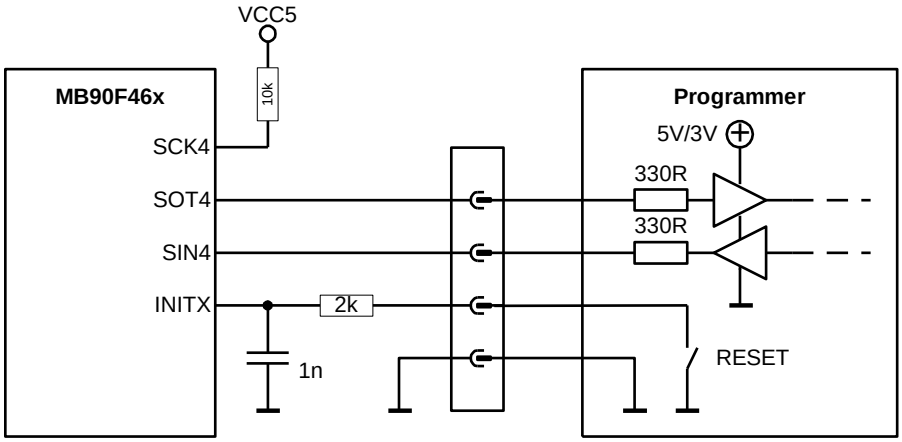
1. SIN4 serial input
2. SOT4 serial output
3. SCK4 clock input
4. INITX reset input

After the MCU Reset the UART4 pins will be initialized for serial communication for the debug or Flash loader. UART4. The other pins are GPIO or external bus.

5.3 Asynchronous Programming

The following schematic shows a possible configuration:

Figure 1. Serial asynchronous programming interface

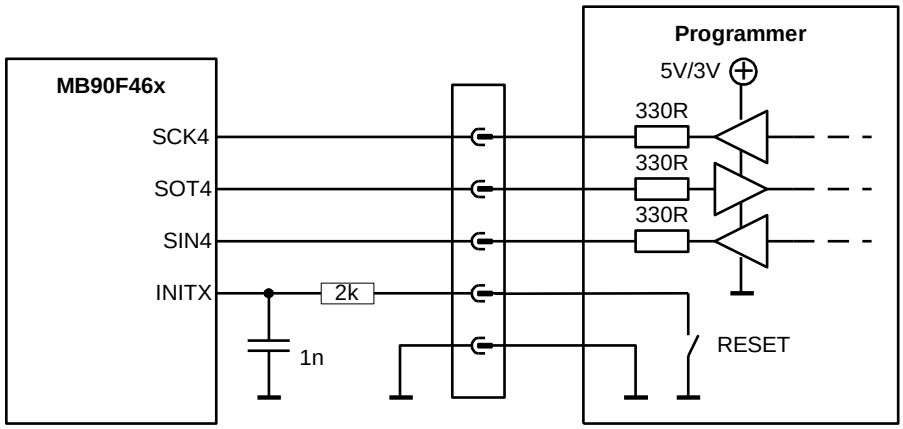


Important note: In run mode the ports corresponding to SIN4 and SOT4 have to be set to output or input with internal pull-up, if not connected to other circuitries! Otherwise this port pins will be floating. Another way is to use an external pull up or down resistors. Make sure the SCK4 pin is connected to stable level because a falling edge could be detected as synchronous interface in use. Hence, an unused SCK4 pin should be connected to external pull up or pull down resistor (2k …10k).

5.4 Synchronous Programming

The following schematic shows a possible configuration:

Figure 2. Serial synchronous programming interface



For pin connection and pull up/down resistors please refer to asynchronous programming. Please note the SCK4 has to be threatened electrically equal to SIN4.

6 Reset Behaviour of GPIO ports and external bus

This Chapter Shows the Behaviour of Io-Port During and After Reset

During the power-on or INITX reset state the GPIO port pins are going to HiZ and the inputs are disabled to prevent the leakage by any floating pin. After release of reset the IO-ports will be set to initial value (see related DS of MB91460 series)

Note: For some MCU derivates (e.g. MB91F467D or MB91F469G) with external bus interface the external bus function will be set by reset, independents on internal or external mode vector fetch. In case of single chip mode the external bus function is active until any user program overwrites the related PFR's from external bus to GPIO function. The initial values of external bus are configured as following:

GPIO	XBUS	Initial function	Initial state
P00-P03	D0-D31	XBUS	Input HiZ
P04-P07	A0-A31	XBUS	Output high
P08-P10	Bus control	XBUS	Output high
P10_4	MCLKO	XBUS	Output CLKT
P10_5	MCLKI	XBUS	Input
MONCLK	MONCLK	XBUS	Output HiZ
P11-P35	-	GPIO	Input HiZ

Note: If the external bus pins should be used as GPIO function the address and bus control lines are driven as output at high level directly after the reset initialization.

7 Document History

Document Title: AN205209 - FR Family 460 Series Hardware Set Up

Document Number: 002-05209

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NOFL	07/12/2006	Initial release
			08/10/2006	Flash programming UART4 added
			10/06/2006	Reset behaviour of GPIO ports and external bus interface added
			03/07/2007	Ceramic smooth capacitor changed to single capacitor
			04/19/2007	Mode pin setting corrected
			09/10/2007	Unused XA0 pin, startup external bus interface, unused SCK4 pin
*A	5123755	NOFL	02/03/2016	Migrated Spansion Application Note from MCU-AN-300033-E-V15 to Cypress format
*B	5870434	AESATMP9	09/01/2017	Updated logo and copyright.
*C	6054520	NOFL	02/05/2018	Updated links. Updated Sales page.

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