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AN205202

Fr Family, Mb91f467s Emulation

This application note describes the emulation system for MB91460S (MB91F467S) series and the current emulation system is based on EVA device MB91V460A, which does not include an APIX® interface.

1 Introduction

This application note describes the emulation system for MB91460S (MB91F467S) series.

The current emulation system is based on EVA device MB91V460A, which does not include an APIX® interface. For that reason the APIX® interface is emulated by an FPGA. The FPGA is connected to the bus interface of MB91V460A.

Note: APIX® is a registered mark of INOVA Semiconductors GmbH

The following chapters describe any discrepancies between FPGA emulation system and MB91F467S standalone Flash microcontroller.

2 Hardware Setup

The chapter describes the setup of the Emulation system

2.1 Required parts

To Emulate the MB91F467S series following parts are required:

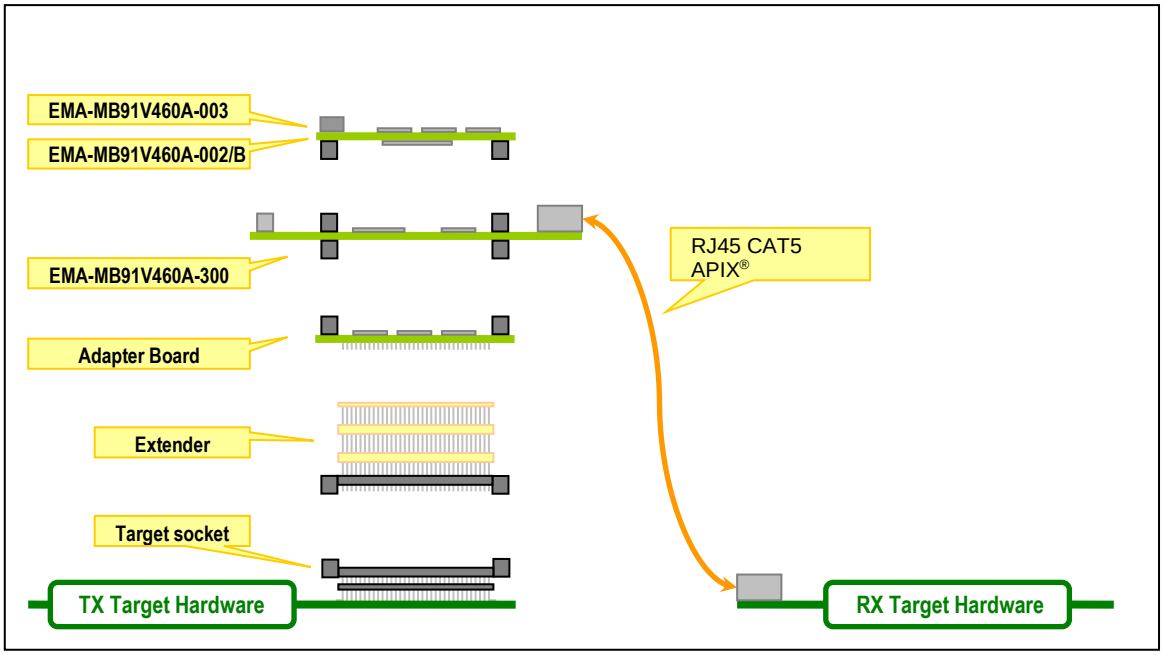
1. MB2198-01 Emulator Main Unit
2. MB2198-10: DSU4 cable
3. EMA-MB91V460A-002B/-80: Adapter board, including MB91V460A
4. EMA-MB91V460A-300: APIX® FPGA extension board
5. EMA-MB91F467S-LS-176M07: Socket adapter board (level shifter)
6. EMA-MB91F467S-NLS-176M07: Socket adapter board (No level shifter)
7. NQ-PACK176SD-ND: Socket for package FPT-176P-M07 (Tokyo Eletech Corp http://www.tetc.co.jp/e)

On the target system a NQ-PACK176SD-ND socket is required enabling connection to the EMA-MB91F467S-LS-176M07 board.

2.2 Installation

The figure below shows the default system setup for APIX® receiver and transmitter connection during emulation.

Figure 1. APIX® Emulation System Setup



For detailed installation instruction see the user guides of the emulation tools.

- UG-910055-xx-EMA-MB91V460A-002.doc
- UG-910065-xx-EMA-MB91V460A-003.doc
- UG-910069-xx-EMA-MB91V460A-300.pdf

It is recommended to read the user guide for the EMA-MB91V460A-300 APIX® FPGA board to ensure correct settings for operation.

In addition there are several application notes for MB2198-01 emulator available, describing features and software installation (e.g. USB drivers).

3 Differences between MB91F467S and Emulation System

The chapter describes the differences between the emulation system and MB91F467S series.

3.1 Overview about differences

Table 1. Overview of the Differences between MB91F467S and Emulation System

Feature	Emulation system (MB91V460A + FPGA)	MB91F467S series
Maximum CPU Operating Frequency	MB91V460A: 80 MHz	100MHz
Must setting for ext. Bus Frequency	20MHz	user defined
Bus Interface pins	Bus interface function required	Bus Interface or GPIO function selectable
Ext. Bus Chip select for FPGA board	One chip select is required for EMA-MB91V460A-300 board User defined: CS [0…7]	Not required
APIX® Register start address	0x0030.7200	0x00.7200
APIX® IP version Register address	0x0030.7320	0x00.7320
APIX® Interrupts	APIX® interrupts connected to external Interrupt 13 and 15 TRANSACTION BUFFER → INT13 EVENT BUFFER → INT15	APIX® interrupts set in APIX® register
Interrupt vector table (Intvect)	External Interrupt	Internal APIX® Interrupts
DMA	Setup via external bus DMA transfer request	Setup via internal register
Number of Transaction buffers	8 buffers	16 buffers
Available ASHELL	ASHELL 0	ASHELL 0 & 1
APIX® Link speed	500Mbit/s	125Mbit/s
AIC pin selection	Selectable via jumper on emulation board	Selectable via PFR/EPFR register

3.2 Details of differences

3.2.1 Maximum CPU Operating Frequency

The maximum operating frequency of the emulation device MB91V460A is 80MHz. Do not set higher PLL frequencies! The MB91F467S series has a maximum operating frequency of 100MHz.

Using the Emulator ensure that the PLL frequency do not exceed 80MHz. The PLL options can be set in the file start91460.asm (See Chapter 4.7.1 Clock Selection in start91460.asm file).

For further details refer to MB91460A series Hardware Manual and MB91F467S series Datasheet.

3.2.2 Must setting for ext. Bus Frequency

The frequency for external bus of the MB91V460A in emulation must be set to 20MHz!

Other settings may cause malfunction of FPGA and APIX® communication.

3.2.3 Bus Interface Usage

Using Emulation system all available Bus interface pins are also used for APIX FPGA board. This ports shall not be set to GPIO functionality otherwise connection to APIX FPGA gets lost.

Using MB91F467S the pins can be assigned to Bus interface functionality or GPIO functionality.

FPGA Reset

Address line A23 is used in some FPGA bit streams. In case of using this bit stream do not use A23 in your Application. Otherwise APIX FPGA might be reset

Latest FPGA bit stream is using Port13_7 as Reset line. A23 can be used as Bus Interface pin.

Table 2. FPGA Reset Pin Usage

Reset pin	FPGA Moduleid Register Value
P05_7 (A23)	0x80270101, 0x80040201, 0x80070201, 0x80250201, 0x80110301, 0x80260301
P13_7	0x80180801

The FPGA bit stream version can be read out via the moduleid register.

See chapter 3.2.6 for register address.

3.2.4 Ext. Bus Chip select for FPGA board

The APIX® FPGA extension board (EMA-MB91V460A-300) is connected to the external bus interface of the MB91V460A emulation chip. Thus it is required to enable one chip select line to access the FPGA via the external bus! The chip select can be freely selected by the user. The FPGA board has to be configured via DIP-SW on EMA-MB91V460A-300 board.

Note:

- The chip select which is enabled for FPGA usage,
  - Cannot be used for any RAM/ROM on target hardware anymore!
  - Has to be configured on adapter board (EMA-MB91F467S-LS-176M07) as masked chip select additionally. Please read the user guide for the adapter board for details on how to configure masked chip select!

3.2.5 APIX® Register start address

The start address of the APIX® Register is different in Emulation tool and MB91F467S.

In MB91F467S the start address is 0x00007200

Using the Emulation system the register start address is in external Bus interface address range. The Offset address value is: 0x0030.7200

There exist two header files for the remote handler (remote_flash.h and remote_emu.h) which overcome the address offset. Select in remote.h file which system is used.

When using the Emulation system the used Chip select must be setup in start91460.asm to ensure access to the Remote Handler / APIX® Register.

3.2.6 APIX® IP Register address (MODULEID)

Within the Register set of the APIX interface there is one 32-bit register including the IP version.

For the MB91F467S this Register is at address: 0x00.7320

For the FPGA system it is at address: 0x30.7320

The MODULEID Register description is as following:

Bit 31: FPGA

0	NONFPGA version
1	FPGA version

- Bit 30 – 24: reserved: read value is ‘0’
- Bit 23 – 16: Date code: Day

- Bit 15 – 08: Date code: Month
- Bit 07 – 00: Revision

3.2.7 APIX® Interrupts

On MB91F467S two internal interrupts are available for the APIX® interface.

On Emulation system these interrupts are available at external interrupts.

Table 3. Interrupt assignment

Interrupt	APIX® Event/ Fatal Error	APIX® Transaction Buffer
MB91F467S	No. 76 / ICR30	No. 80 / ICR32
Emulation system	No. 31 / ICR07	No. 29 / ICR06

3.2.8 DMA usage

At MB91F467S internal DMA transfer from APIX register can be used.

Using the emulation system, the DMA transfer must setup using DMA via external Bus.

3.2.9 Number of Transaction buffer

The number of available transaction buffer is different in Emulation system and MB91460S.

For the Emulation system (FPGA) 8 buffers (0 -7) are available. They are assigned to Link 0.

For the MB91460S series 16 Transaction buffers are available.

3.2.10 Available APIX® Link

In Emulation system ASHELL 0 is available.

In MB91460S series ASHELL 0 and 1 are available. ASHELL 0 can be assigned to internal Physical layer (APIX® link) or Automotive Interconnection Link output. ASHELL 1 is assigned to Automotive Interconnection Link only.

3.2.11 APIX® Link speed

Emulation system APIX® Link speed is 500Mbit/s as external INAP APIX® Transceiver are used.

The MB91F467S APIX® Link speed is 125MBit/s.

Payload data

MB91F467S: max. 2.79 MByte/s

Condition: Use Case: Downlink over Pixelchannel

CLKB = 100MHz, CKLP = 50 MHz,

Data transfer from internal Flash to transaction buffer using DMA

Emulation system: max. 150 kByte/s

Condition: Use Case: Communication over Automotive Interconnect to external AShell (1Bit Datawidth)

CLKB = 60MHz, CLKP=10MHz, CLKB = 20MHz

Data transfer from internal Flash to transaction buffer using DMA

3.2.12 AIC pin selection

In case of AIC link (Automotive InterConnection) usage the dedicated pins needs to be configured.

For Emulation system the selection if using GPIO or AIC function is done via jumper on emulation board. See corresponding documentation.

Note: Emulation system supports only ASHELL 0!

Using MB91F467S selection is possible via PFR and EPFR register setting.

4 MB91F467S template Project

The chapter describes the template project of MB91F467S series.

Cypress is offering a template project for MB91F467S series. It includes some basic settings for e.g. APIX®, Linker, C-Compiler which must be checked and modified in detail, corresponding to the user application.

4.1 Template file structure

The template project comes with following files:

- Start91460.asm
- Vectors.c / .h
- Mb91467s.h / .asm
- Remote.h / .asm
- Remote_flash.h
- Remote_mcu.h
- Main.c
- Fpga.c / .h

4.1.1 Start91460.asm

The Start91460.asm file is sued to initialise the MCU. Settings like stack size, Clock speed and Bus interface can be set in this file.

When using the Emulation system ensure that the Chip select for the APIX® FPGA board (DIP switch on EMA-MB91V460A-300) is set to “ON” and all configuration register are set accordingly.

4.1.2 Vectors.c / .h

This file contains the Interrupt vector table. In addition the Interrupt level can be set via the ICRxx register.

Be aware of the different interrupt vectors of MB91F467S and Emulation system for the Remote handler / APIX®.

4.1.3 Mb91467s.h / .asm

This file defines the I/O register of MB91F467S series. The Remote Handler / APIX® register are defined in a separate file.

4.1.4 Remote.h / .asm

The Emulation system and MB91F467S have different addresses for Remote Handler / APIX® register. Select in this file which target system (STANDALONE or EMULATION) is used. Depending on this selection a header file is included with offset address for that target system.

Figure 2. remote.h file

```
/* THIS SAMPLE CODE IS PROVIDED AS IS AND IS SUBJECT TO ALTERATIONS.        */
/* MICROELECTRONICS ACCEPTS NO RESPONSIBILITY OR LIABILITY FOR ANY ERRORS OR  */
/* ELIGIBILITY FOR ANY PURPOSES.                                             */
/* ------------------------------------------------------------------------- */

#define STANDALONE 1
#define EMULATION  2

#define TARGET_SYSTEM STANDALONE // <<< please choose target system

#if (TARGET_SYSTEM == STANDALONE)
       #include "remote_flash.h"
#elif (TAGET_SYSTEM == EMUALTION)
       #include "remote_emu.h"
#else
       #error Target system not supported!
#endif
```

4.1.5 Remote_flash.h

This file contains the register definition and addresses of Remote Handler / APIX® register for Mb91F467S. (start address: 0x00007200)

4.1.6 Remote_emu.h

This file contains the register definition and addresses of Remote Handler / APIX® register for Emulation system. (start address 0x00307200)

4.1.7 Fpga.c / .h

The Emulation system has to set some respective reset settings during startup.
This files hold the required rest and initialization routines for the fpga.

The following function call has to be inserted into the project main and has to be called after initialization of the external bus interface:

Fpga_Init();

A Appendix

A.1 Related Documentation

A.1.1 Application Notes:

- FR Family MB2198-01 Emulator System Getting Started Guide
- AN205146 - FR Family, MB91460 Emulation System
- AN204828 - F2MC-16FX Family, Emulating and Debugging with Softune and MB2198-01
- AN205200 - FR Family MB91460 Series, Start91460.asm

A.1.2 Documentation:

- MB91460A series Hardware Manual
- MB91F467S series Datasheet
- EMA-MB91V460A-00x User Guide
- EMA-MB91V460A-300 (APIX® extension board) User Guide
- EMA-MB91F467S-LS-176M07 (socket adapter board) User Guide

5 Document History

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Document Number: 002-05202

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NOFL	02/06/2008	Initial release
			03/05/2008	Chapter 3.2.5 APIX® IP Register address (MODULEID) Bit0.7 description corrected
			03/28/2008	Chapter 2.2: add. information's added
			08/21/2008	Chapters Bus Interface usage, AIC pin selection added
			10/02/2008	Chapter 3.2.11 payload data added
*A	5084096	NOFL	01/14/2016	Migrated Spansion Application Note from MCU-AN-300023-E-V14 to Cypress format
*B	5844304	AESATP12	08/04/2017	Updated logo and copyright.
*C	6052824	NOFL	02/02/2018	Updated links. Updated Sales page.

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