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AN205118

F²MC-8FX Family MB95260 and MB95560 Comparison

This application note compares the MB95260 and MB95560 series and also with different series with different peripheral types that are available, the port-pin function share is the same between MB95260 and MB95560.

1 Introduction

This application note compares the MB95260 and MB95560 series.

The MB95260 series consists of several different series with different peripheral types. The MB95260 is the current production. In contrast, the MB95560 is a newly generation production using new technology with high performance. Though different series with different peripheral types are available, the port-pin function share is the same between MB95260 and MB95560. The MB95560 instruction set is compatible with MB95260 series.

2 Peripherals

This chapter describes the differences of the peripherals

There are some differences of peripheral resource between MB95260 and MB95560.

2.1 Clock Distribution

MB95560 uses a new main CR macro with different frequencies and higher accuracy.

	MB95260	MB95560
Main CR frequency	1/8/10MHz +/- 3%	4MHz +/- 2%
Sub CR frequency	50~200KHz	50~150KHz
PLL multipliers	N/A	x2, x2.5, x3, x4

2.2 Clock Control Registers

The clock control registers is different between MB95260 and MB95560.

MB95260
MB95560
Different Point

	Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	PLLC	0006H	-	-	-	-	-	-	-	-
			MPEN	MPMC1	MPMC0	MPRDY	-	-	-	-
	SYCC	0007H	-	-	-	-	SRDY	-	DIV1	DIV0
			SCM2	SCM1	SCM0	SCS2	SCS1	SCS0	DIV1	DIV0
	STBC	0008H	STP	SLP	SPL	SRST	TMD	SCRDY	MCRDY	MRDY
			STP	SLP	SPL	SRST	TMD	-	-	-
	SYCC2	000DH	RMC1	RMC0	RCS1	RCS0	SOSCE	MOSCE	SCRE	MCRE
			SRDY	MRDY	SCRDY	MCRDY	SOSCE	MOSCE	SCRE	MCRE
	STBC2	000EH	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	DSTBYX

For detail register setting, please refer to the MB95560 Hardware Manual.

2.3 Deep Standby Mode

The deep standby mode of MB95560 series is a completely new feature. While MCU will enter standby mode, MB95560 can enter deep standby mode if bit0 of Standby Control Register 2 (STBC2) is set to 0. After that, flash memory will be disabled. STBC2 is a new register.

	MB95260	MB95560
Deep standby mode	N/A	Before enter standby mode, set STBC2_DSTBYX to 0

2.4 Time Base Timer

Main PLL can be performed the source clock for time base time of the MB95560 MCU.

	MB95260	MB95560
Clock Source	Main CR Main Clock	Main CR Main CR PLL Main Clock

2.5 Watch Dog Timer

Due to Sub CR range is 50~150 KHz of MB95560 series, the minimum interval time of Sub CR is increased.

	MB95260	MB95560
Sub CR frequency	50~200KHz	50~150KHz
WDT interval time of Sub CR (Min)	328ms	437ms

2.6 Clock Supervisor Counter

The CR frequency is fixed to 4MHz, new counter values in relation to TBTSEL settings are used in CSV module. Please refer to MB95560 Hardware Manual for details.

2.7 8/16 Bit Composite Timer

The 8/16 bit composite timer of MB95560 series is a little different from MB95260 series.

	MB95260	MB95560
Input capture mode (Both edge detection)	The first falling edge cannot be detected	The first falling edge can be detected

2.8 NVR Register

MB95560 series adds a new NVR byte for CR trimming. It is called Main CR Temperature Dependent Adjustment Register (CRTDA). The lower 5 bits of this register are loaded from flash address 0xFFBB bit 4- bit 0 to IO area 0x0FE7 bit 4- bit 0 during reset. The initial value is determined by the pre-loaded values in flash.

MB95260
MB95560
Different Point

	Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	CRTH	0FE4H	-	CRSEL1	CRSEL0	CRTH4	CRTH3	CRTH2	CRTH1	CRTH0
			-	-	-	CRTH4	CRTH3	CRTH2	CRTH1	CRTH0
	CRTDA	0FE7H	-	-	-	-	-	-	-	-
			-	-	-	CRTDA4	CRTDA3	CRTDA2	CRTDA1	CRTDA0

2.9 Flash Operation

The flash memory automatic algorithm of MB95560 has been modified. For each flash operation, the bus address is changed from AAAH to AA8H every write cycle. For detailed information, please refer to the MB95560 Hardware Manual.

	MB95260	MB95560
Write	$UAAA_H$ ← AA_H $U554_H$ ← 55_H $UAAA_H$ ← $A0_H$ PA ← PD	$UAA8_H$ ← AA_H $U554_H$ ← 55_H $UAA8_H$ ← $A0_H$ PA ← PD
Erase	$UAAA_H$ ← AA_H $U554_H$ ← 55_H $UAAA_H$ ← 80_H $UAAA_H$ ← AA_H $U554_H$ ← 55_H $UAAA_H$ ← $10_H/30_H$	$UAA8_H$ ← AA_H $U554_H$ ← 55_H $UAA8_H$ ← 80_H $UAA8_H$ ← AA_H $U554_H$ ← 55_H $UAA8_H$ ← $10_H/30_H$

2.10 I/O Ports

Several I/O port functions have been changed.

	MB95260	MB95560
Input level select register	Input level of P04 can be selected by ILSR bit 2 [ILSR] 0: Hysteresis input level selected 1: CMOS input level selected	ILSR has been deleted Input level of P04 is fixed to hysteresis
Pull-up register of P62~P64	P62/P63/P64 do not have pull-up	P62/P63/P64 can be pulled up by setting PUL6[4:2] to 1
Hysteresis input High = 0.8VDD Low = 0.2VDD	P00 to P07 P12 P62 to P64 PF0, PF1 PG1, PG2	P00 to P03, P05 to P07 P12 P62 to P64 PF0, PF1, PF2 PG1, PG2
Hysteresis input High = 0.7VDD Low = 0.3VDD	P04 PF2	P04
High current pin	P05, P06 P62, P63	P00 to P03, P05 to P07 P62, P63

2.11 I/O Map

Some new registers are added in MB95560 series.

Register Abbreviation	MB95260	MB95560
PLLC	N/A	PLL Control Status Register
STBC2	N/A	Standby Control Register 2
PUL6	N/A	Port 6 Pull-up Register
LVDR	N/A	LVD Reset Voltage Selection ID Register
CRTDA	N/A	Main CR Temperature Dependent Adjustment Register
ILSR	Input Level Select Register	N/A

3 Additional Information

For more information on Cypress MB95560 products, please visit following website:

www.cypress.com/documentation/application-notes/mb95560-compare-differ-between-mb95260-mb95560

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	RLIU	08/26/2010	Initial release.
			05/20/2011	Update bit name of STBC2 register.
*A	5258867	RLIU	05/09/2016	Migrated Spansion Application note from MCU-AN-500097-E-11 to Cypress format.
*B	5843406	MALI	08/04/2017	Updated logo and copyright.

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