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AN205011

F²MC-8FX Family, MB95430 Series Voltage Comparator

This application note describes the fundamental of voltage comparator and the register configuration. The related sample codes were given as well.

1 Introduction

This application note describes the fundamental of voltage comparator and the register configuration. The related sample codes were given as well.

2 Feature of Voltage Comparator

This chapter introduces the features of the voltage comparator.

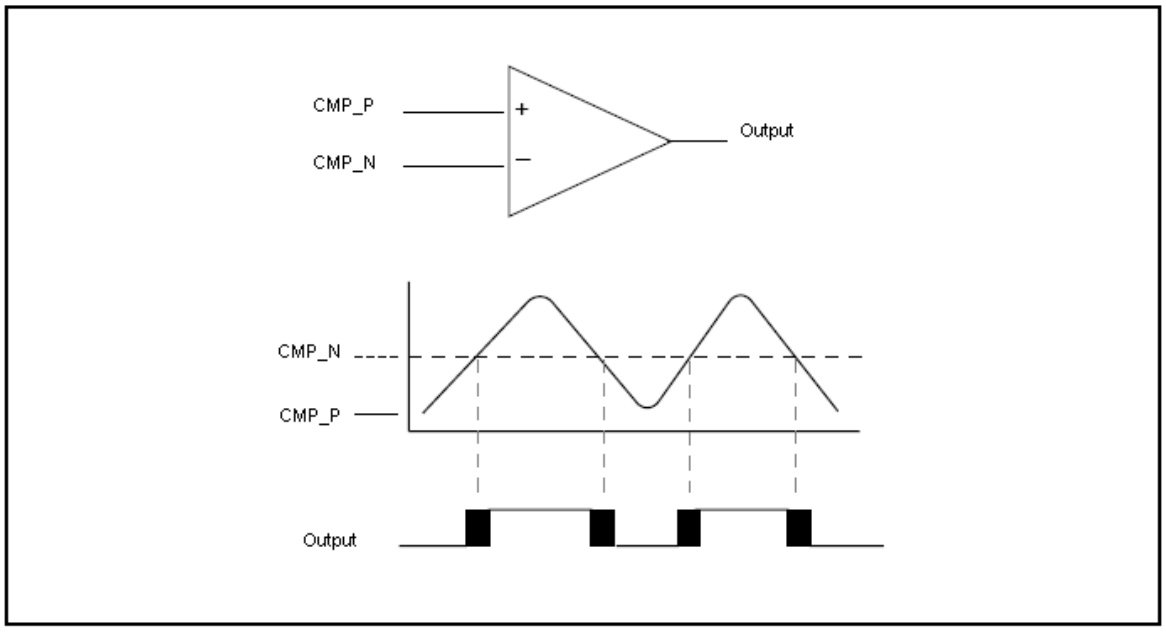
2.1 Comparator Fundamental

A single comparator is shown in

Figure 1 along with the relationship between the analog input levels and the digital output. When the analog input at CMP_P is less than the analog input CMP_N, the output of the comparator is at digital “L” level. When the analog input at CMP_P is greater than the analog input CMP_N, the output of the comparator is at digital “H” level.

The shaded areas of the output in Figure 1 represent uncertainty due to input offsets and response time.

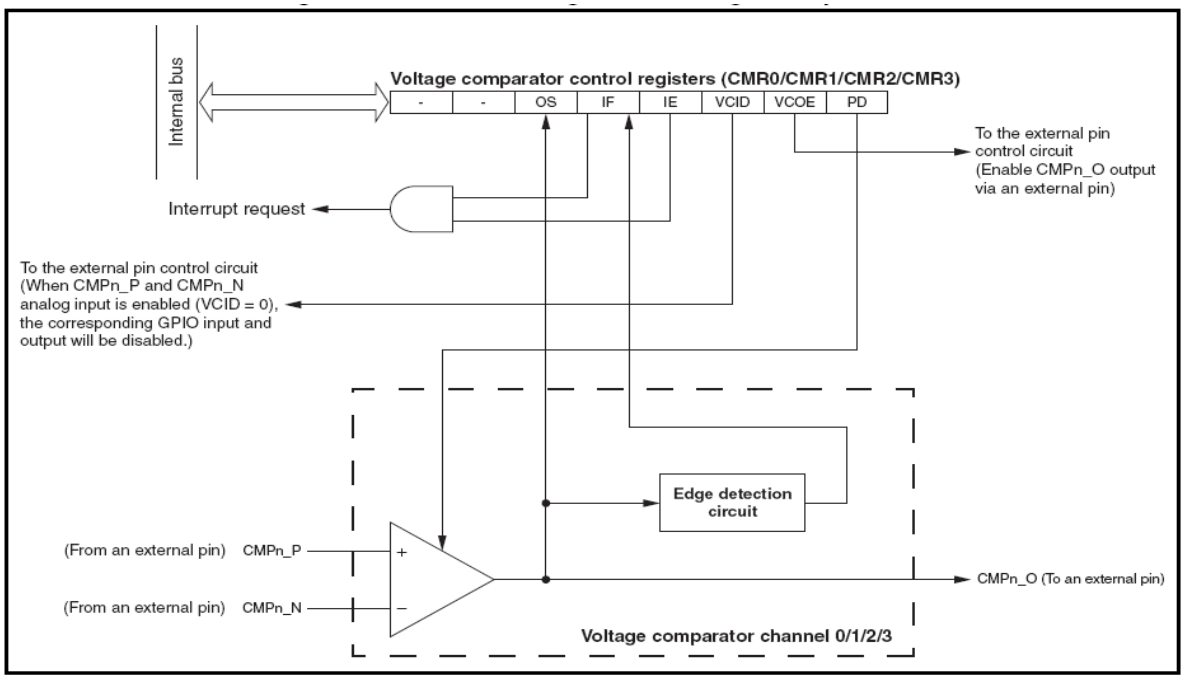
Figure 1. Comparator Operation



2.2 Block Diagram of Voltage Comparator

Figure 2 shows the block diagram of voltage comparator.

Figure 2. Block Diagram of Voltage Comparator



2.3 Pins Associated with the Voltage Comparator

2.3.1 Input Pins

For each voltage comparator, there are two analog input pins which are named as CMPn_P and CMPn_N, and either of them can be connected to the external reference voltage which depends on the output level desired. Before enabling the voltage comparator, the user has to enable the analog input by clearing the bit CMRn_VCID. A reset will clear the CMRn_VCID to default.

Since the input pins are shared by GPIO/VC and internal ADC channel, the right configuration should be done to select the right function of pins, just shown as Table 1.

Table 1. Input Pin Configuration

CMRn_VCID	AIDRH	Pin Status
0(Enable)	0(ADC)	VC and ADC
0(Enable)	1(GPIO)	VC
1(Disable)	0(ADC)	ADC
1(Disable)	1(GPIO)	GPIO

2.3.2 Output Pins

The output pins of voltage comparators are shared by several peripherals or GPIOs. The output pins are disabled as default. They can be enabled by set the CMRn_VCOE to 1.

2.4 Edge Detection Circuit

The edge detection circuit detects the level conversion of the comparator output. Except in stop mode, watch time mode or time base mode, a raising edge or a falling edge of voltage comparator output will set the interrupt flag of the related register automatically.

2.5 Control Registers (CMR0~CMR3)

These registers are used to turn on and off the voltage comparator (CMR0~CMR3: PD), to enable and disable voltage comparator output (CMR0~CMR3: VCOE), and to enable and disable voltage comparator analog inputs (CMR0~CMR3: VCID).

Except in stop mode, watch mode or time-base timer mode, if CMR0~CMR3: IE has been set to "1", upon detection of a rising edge or falling edge of voltage comparator output, the voltage comparator generates an interrupt request and the interrupt flag bit (CMR0~CMR3: IF) is automatically set to "1" at the same time.

The output status of a voltage comparator channel (ch. 0/1/2/3) can be read through the OS bit in its corresponding voltage comparator control register (CMR0~CMR3).

Figure 3 shows the detailed content of the registers.

Figure 3. Register of Voltage Comparators

	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
CMR0	003AH	-	-	OS	IF	IE	VCID	VCOE	PD	00000001B
CMR1	003BH	R0/WX	R0/WX	R/WX	R(RM1),W	R/W	R/W	R/W	R/W	
CMR2	003CH									
CMR3	003DH									

PD	Voltage comparator power down control bit
0	Turns on the voltage comparator.
1	Turns off the voltage comparator.

VCOE	Voltage comparator output enable bit
0	Disables voltage comparator output.
1	Enables voltage comparator output.

VCID	Voltage comparator analog input disable bit
0	Enables voltage comparator analog input.
1	Disables voltage comparator analog input.

IE	Interrupt request enable bit
0	Disables interrupt requests.
1	Enables interrupt requests.

IF	Output edge detection interrupt flag bit	
	Read	Write
0	No interrupt requests.	Clears this bit.
1	An interrupt has been generated.	No effect on operation.

OS	Output status bit
0	The voltage comparator outputs "L".
1	The voltage comparator outputs "H".

R/W : Readable/writable (The read value is the same as the write value.)
R(RM1),W : Readable/writable (The read value is different from the write value. "1" is read by the read-modify-write (RMW) type of instruction.)
R/WX : Read only (Readable. Writing a value to it has no effect on operation.)
R0/WX : The read value is "0". Writing a value to it has no effect on operation.
- : Undefined bit
: Initial value

2.6 Interrupt Vector of Voltage Comparator

If the CMRn_IE is enabled, the user needs to configure the interrupt vector of voltage comparator first.

Table 2 below shows the interrupt vector.

Table 2. Interrupt Vector

Interrupt source	Interrupt request no.	Interrupt level setting registers		Vector table addresses	
		Register	Setting bit	Upper	Lower
Voltage Comparator channel 0	IRQ10	ILR2	L10	$FFE6_H$	$FFE7_H$
Voltage Comparator channel 1	IRQ11	ILR2	L11	$FFE4_H$	$FFE5_H$
Voltage Comparator channel 2	IRQ12	ILR3	L12	$FFE2_H$	$FFE3_H$
Voltage Comparator channel 3	IRQ13	ILR3	L13	$FFE0_H$	$FFE1_H$

Note: In stop mode, watch mode or time-base timer mode, the edge detection circuit stops work, and the interrupt flag bit (IF) of voltage comparator control registers (CMR0~CMR3) will not be updated even if the voltage comparator is turned on.

3 Software Operation

3.1 Setting Procedure

- Disable interrupt first.
- Enable analog input and disable output.
- Active comparator.
- Wait until comparator becomes stable.
- Clear interrupt flag bit.
- Enable interrupt if necessary.
- Enable output pin if necessary.

3.2 Initialization

This routine is the initialization of voltage comparator.

Figure 4. Initialization of Voltage Comparator

```
/*Initialize the voltage comparator*/
CMR0 = 0x00;            // disable the interrupt first
                        // enable analog input
                        // disable analog output
                        // turn off comparator
CMR0_PD = 1;            // turn on comparator

__wait_nop();           // several us for comparator
__wait_nop();           // becoming stable
__wait_nop();

CMR0_IF = 0;            // clear flag
CMR0_IE = 1;            // enable interrupt

CMR0_VCOE = 1;          // enable output if necessary
```

To voltage comparator, there is a stable time when it was turned on or the reference voltage changed. Before activating voltage comparator, please preset CMR0~CMR3: IE to 0, in order to avoid any unexpected interrupt request caused by voltage comparator's unstable status during its startup.

3.3 Interrupt

The voltage compare interrupt occurs at raising edge or fall edge which depends on the input. So, It is better to confirm the output level first in the ISR.

Figure 5. Interrupt Service Routine

```
__interrupt void VC0_ISR(void)
{
    if(CMR0_IF&CMR0_IE)     // interrupt flag was set
    {
        CMR0_IF = 0;        // clear interrupt flag
        if(CMR0_OS)         // is the "H" level which is expected?
        {;}                 // yes
        else
        {;}                 // no

    }
}
```

The user should set the interrupt priority and vector in the file vector.c supplied by Cypress, just like this:

Figure 6. Interrupt Priority Setting

```
/*-------------------------------------------
 name: InitIrqLevels()
 function: Initialize the interrupt priority
-------------------------------------------*/
void InitIrqLevels(void)
{
    //...
     ILR2 = 0xCF;           //  IRQ8:  Output compare ch1 match
                            //  IRQ9:  reserved
                            //  IRQ10: Voltage comparator ch0
                            //  IRQ11: Voltage comparator ch1
    //...
}
/*-------------------------------------------
 Prototype
-------------------------------------------*/
__interrupt void VC0_ISR(void);

/*-------------------------------------------
 Vector definition
-------------------------------------------*/
#pragma invect VC0_ISR  10  // IRQ10: Voltage comparator ch0
```

All above just take the comparator0 for example. The configuration for comparator 1~3 is almost the same.

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4.1 Sample Code

Project 1: Voltage Comparator Configuration

```
#include "mb95430.h"

main ()
{
```

```
        __DI ();
        InitLrqLevels ();
        __EI ();

        /*Initialize the voltage comparator*/
        CMR0 = 0x00;                    // disable the interrupt first
                                        // enable analog input
                                        // disable analog output
                                        // turn off comparator
        CMR0_PD = 1;                    // turn on comparator

        __wait_nop ();                   // several us for comparator
        __wait_nop ();                  // becoming stable
        __wait_nop ();

        CMR0_IF = 0;                    // clear flag
        CMR0_IE = 1;                    // enable interrupt

        CMR0_VCOE = 1;                  // enable output if necessary

        /*loop*/
        while (1)
        {;}
}

__interrupt void VC0_ISR (void)
{
        if (CMR0_IF&CMR0_IE)            // interrupt flag was set
        {
                CMR0_IF = 0;            // clear interrupt flag
                if (CMR0_OS)            // is the "H" level which is expected?
                {;}                     // yes
                else
                {;}                     // no

        }
}
```

5 Document History

Document Title: AN205011 - F²MC-8FX Family, MB95430 Series Voltage Comparator

Document Number: 002-05011

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	RLIU	03/10/2010	Initial release
			04/12/2010	Updated by review
*A	5243090	RLIU	04/27/2016	Migrated Spansion Application Note MCU-AN-500079-E-11 to Cypress format

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