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AN204772

F²MC-16FX Family, Hardware Set Up

This application note describes how to set up a hardware environment for Cypress 16FX MCUs.

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1 Introduction

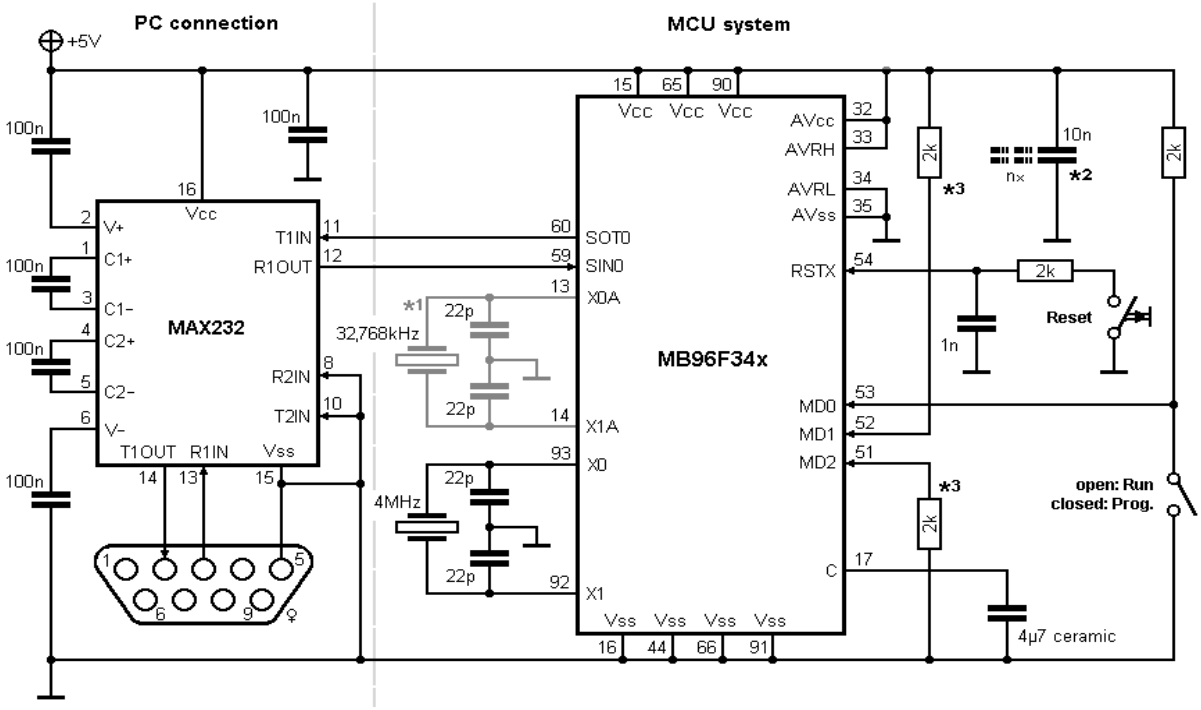
This application note describes how to set up a hardware environment for Cypress 16FX MCUs. As an example the MB96F34x MCU is used.

2 Minimal System

This Chapter Gives an Example of a Minimum Hardware System

2.1 Schematic

The following graphic shows a schematic of a minimum hardware system. Note that for other MCU families a different pinning is needed.



*1 only needed for dual clock devices.
*2 please refer to chapter 3
*3 If PCB has good EMI routing, resistors can be 0Ω for mode pins

2.2 Serial Interface

The “PC connection” section is only needed, if no 5V external serial data lines for programming are existing. The MAX232 is a standard level shifter, which converts the 5V levels of the MCU to ±12V RS232V24 levels and vice versa.

If you use a 3.3V system a MAX3232 is recommended.

Please consider, that the internal charge pumps of the level shifter can produce noise on the +5 Volts line, which can influence the ADC, if AVcc and AVRH are directly (unfiltered) connected to it.

If the system is set to Background Debugging Mode (BDM), the used DBM-USART SIN pin shall be terminated to V_{CC}. Please see chapter 6 for details.

2.3 Power supply

The power supply should be from 3 Volts to 5.5 Volts for normal usage. If a different supply voltage is used please refer to the MB96340 data sheet.

2.4 Analog Digital Converter Supply Pins

The analog converter supply pins (AVcc, AVss, AVRH, AVRL) should be connected even if the ADC of the MCU is not used. Please refer to our application note *mcu-an-300215-e-16fx_adc* for using the ADC and pin connection.

2.5 Analog Input Pins

Because the ADC works with an internal sample capacitor the input impedance and external capacity must be low. Cypress recommends an input impedance of not more than 15k Ohm. Choose the external capacity as low as possible (about 1 nF for EMI protection).

2.6 Reset Pin (RSTX)

To reset the MCU a switch connects this pin to Vss (Ground). Additionally a capacitor has to be connected between Vss and the reset pin for debouncing the switch and for EMI protection. From experience Cypress recommend a capacity of not more than 1 nF. This capacity covers the most common frequency protection in a wide range. Higher capacities and high impedance may cause latch-up effects together with an RSTX-Switch and low EMI protection.

For further information please refer to the general application note *mcu-an-300219-e-16fx_reset*.

2.7 C Pin

A 1..10µF ceramic capacitor (dielectric X7R, e. g. 4,7µF) *must* be connected close to the C pin of the MCU. Otherwise the MCU may not operate correct or will be damaged in worst case. Also see chapter 3.

2.8 Clock Source

A clock source must be provided to the MCU. Therefore crystals or external clock signals can be used. For external source pin X0 (X0A) is used whereby pin X1 (X1A) is not connected.

The sub clock X0A pin has to be pulled down, if sub clock is not used.

Please also refer to the chapter *Outline/Precautions for Device Handling* in the corresponding hardware manual for details.

2.9 Mode Pins

The mode pins signalize the MCU the current operation mode. For a minimal system only two modes are necessary: Flash-Asynchronous-Serial-Programming-Mode and Run Mode. They should be pulled-up with 2k resistors. If the PCB routing protects ESD and EMI influence, the mode pins can be connected directly to Vss and ground, but please see chapter 4.

For these programming modes and methods please refer to the application notes *mcu-an-300224-e-v10-16fx_mcu_flash_prog_bi_rom*.

The following settings are used for the both modes mentioned above:

2.9.1 Flash-(A)synchronous-Serial-Programming-Mode

MD0	MD1	MD2
0	1	0

2.9.2 Run Mode

MD0	MD1	MD2
1	1	0

2.9.3 NC Pins

Do not leave input pins open. Disable input pin functionality with `PIERxy_IEz = 0;` in this case.

Please read Chapter 4 for how to proceed with unused (not connected) pins.

3 Layout and Electromagnetic Compatibility

This Chapter Gives Some Tips for Layout Design

3.1 General

To avoid ESD problems and noise emission of the system some rules for the layout design has to be observed.

The most critical point is the C pin because this is the connection to the internal 1.8 V supply for the MCU core. Thus the two decoupling capacitors have to be placed very near to this pin.

Also the ground and Vcc routing has to be done carefully. Vcc lines should be routed in star shape. We recommend a Vss ground plane *on the mounting side* just under the MCU. For both Vcc and Vss only *one* connection to the rest of the circuit should be done, otherwise noise is carried-over from and to the MCU. Decoupling capacitors (DeCaps) has to be placed as nearest as possible to the related pins. If they are placed too far away their function becomes useless.

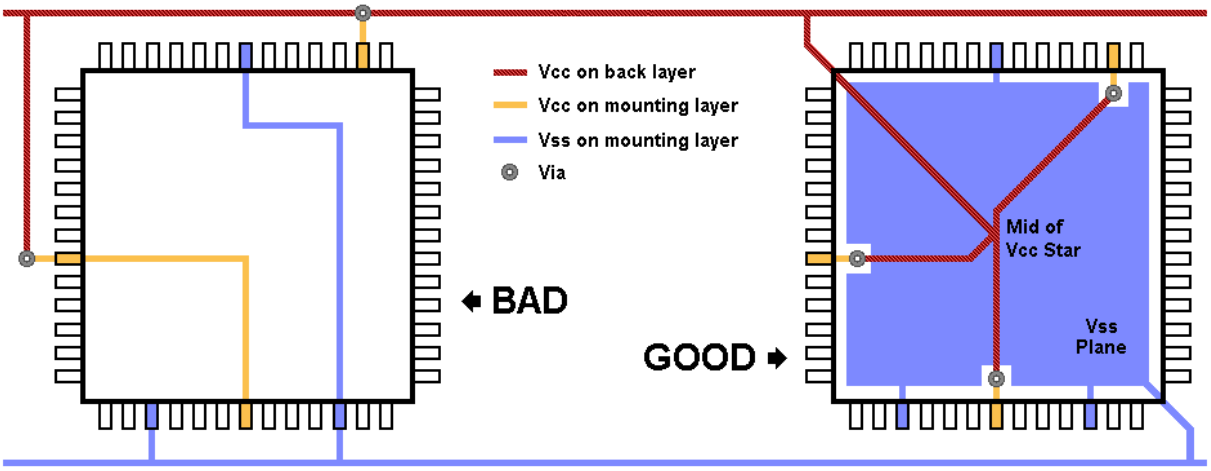
If crystals are used, they have to be placed as nearest as possible to the Xn(A) pins.

If possible all decoupling capacitors should be placed on the same mounting side as the MCU.

3.2 Power Line Routing

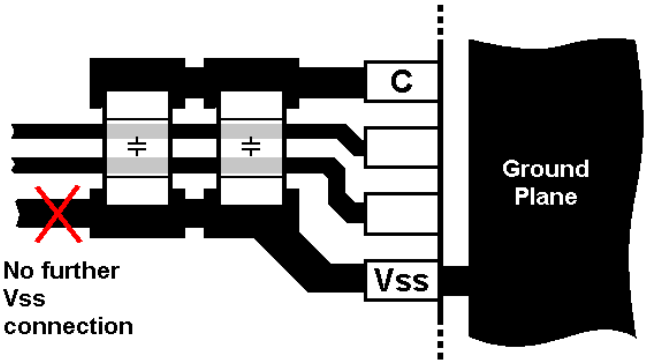
In general the Vcc and Vss lines should not be routed in “chains”, but in “star shape”. For Vss a ground plane is recommended which covers the chip package, and is connected in *one* point to Vss of the whole circuit.

Below is a example of a bad and a good power line routing:

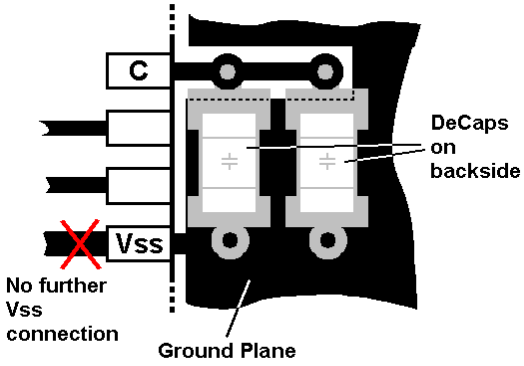


3.3 C Pin Decoupling

The following routing and placement for single sided metal layer is recommended (Note, that in all following illustrations the mounting metal layer is drawn in black and the back side metal layer in gray):

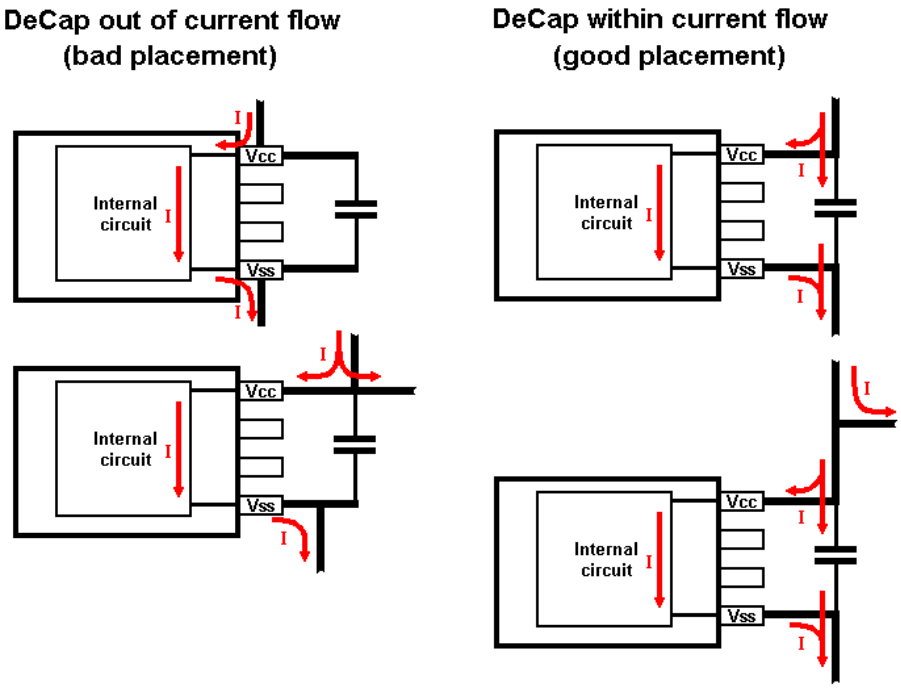


The following routing and placement for double sided metal layer is recommended. Note, that despite the capacitors are placed on the opposite side as the MCU, this solution is the best.



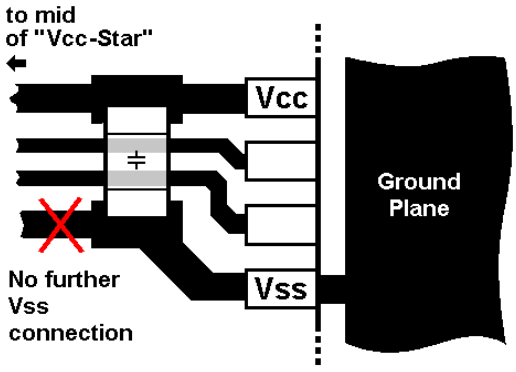
3.4 Power Supply Decoupling

DeCaps for power supply have to be placed within the “current flow”. Otherwise they are senseless, because then their function become inoperable. The following graphic illustrates this:

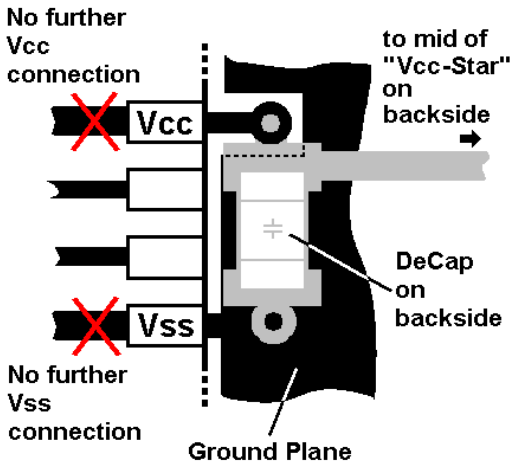


For EMI reasons all decoupling capacitors should have the same capacitance, so that all have a common resonance frequency. Cypress recommends 10nF (~100 MHz resonance) to 100nF (~10 MHz resonance) depending on application. For further detailed information please refer to the application note *16bit-EMC-Guideline*.

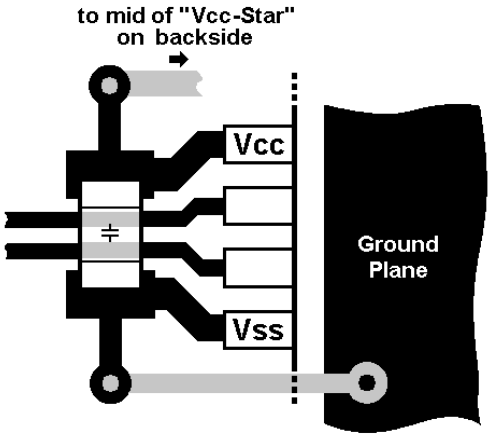
The following routing and placement for single sided metal layer is recommended:



The following routing and placement for double sided metal layer is recommended. Note, that despite the capacitor is placed on the opposite side as the MCU, this solution is the best like for the C pin.



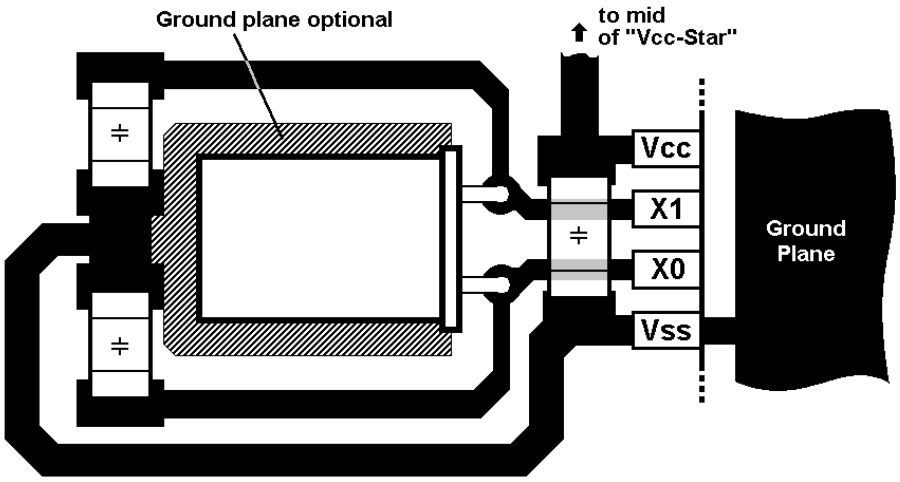
If mounting on both sides is not possible the following placement and routing is recommended:



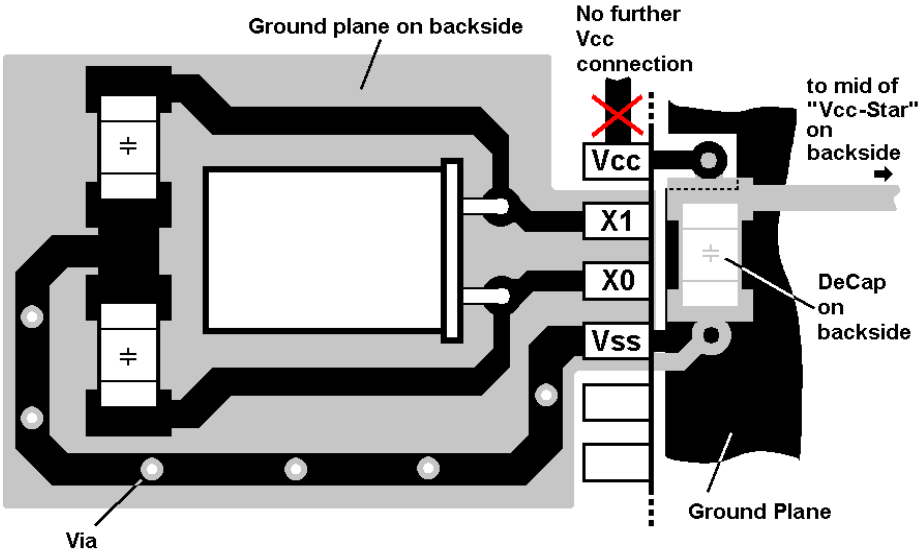
3.5 Quartz Crystal Placement and Signal Routing

The crystal has to be placed as nearest as possible to the MCU. Therefore the oscillator capacitors have to be placed “behind” the crystal.

For single metal layer circuit board the following placement and signal routing is recommended:



For double sided metal layer layout the following is recommended:



3.6 Other documents

For further detailed information please refer to the application note *16bit-EMC-Guideline*.

3.7 MCU Pin Summary

The following table shows the EMC critical pins and gives short information about how to connect them.

Pin name	Function
VCC	Main supply for IO buffer MCU core, close to input the internal 3.3V regulator, close to crystal oscillator
VSS	Main supply for IO buffer and MCU core, close to the internal 3.3V regulator, close to crystal oscillator
C	External 1..10µF ceramic capacitor (dielectric X7R) as smooth capacitors for internal 1.8V regulator output, it is used for supply of the MCU core. Note, that this pin leads the most of noise. Please refer to the DS of used MCU series for selection of capacitance value.
AVCC*	Power supply for the A/D converter
AVSS*	Power supply for the A/D converter
AVRL*	Reference voltage input for the A/D converter
AVRH*	Reference voltage input for the A/D converter
DVCC*, HVCC*	Power supply for the PWM (high current) outputs, it is not connected to VCC, should be connected to extra power supply
DVSS*, HVSS*	Power supply for the PWM (high current) outputs, it is not connected to VSS, should be connected to extra power supply
X0, X0A*	Oscillator input, if not used so shall be connected with pull-up or pull-down resistor (see please DS)
X1, X1A*	Oscillator output, the crystal and bypass capacitor must be connected via shortest distance with X1 pin, if not used so shall be open

*only if supported by device

4 Port Input / Unused Pins / Latch-up

How to connect Input Port Pins and how to proceed with unused Pins

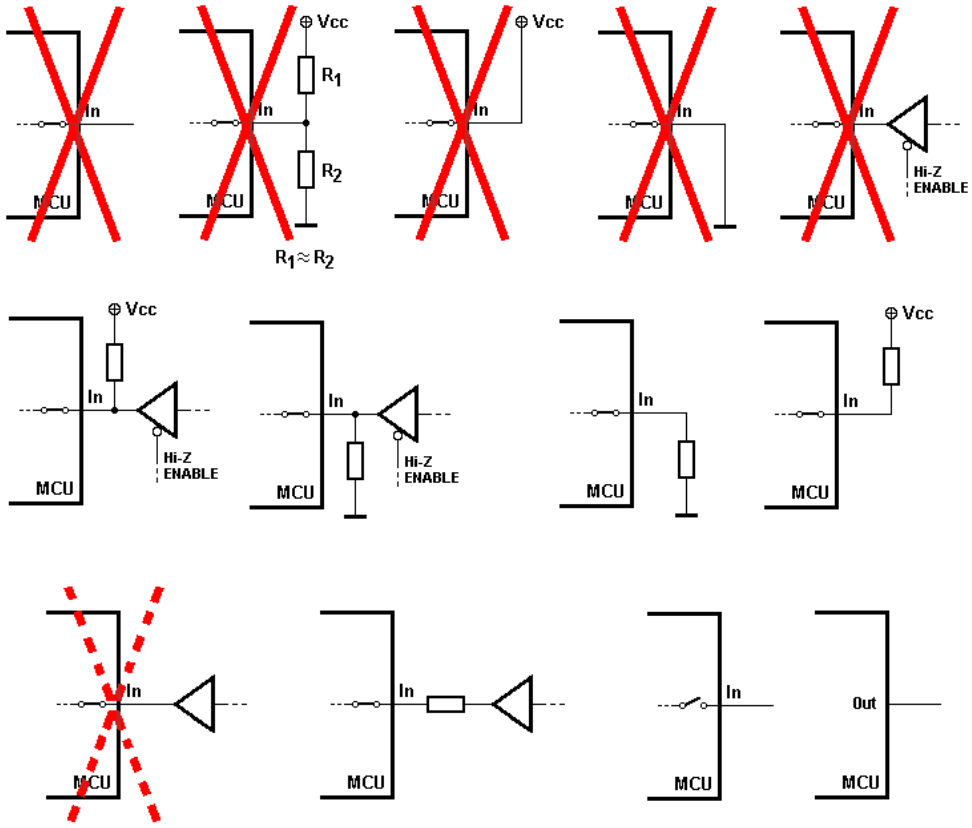
4.1 Port Input / Unused Pins

It is strongly recommended to do not pins unconnected, while they are switched to input. In this case those pins can enter a so-called *floating state*. This can cause a high I_{CC} current, which is adverse to low power modes. Also damage of the MCU can happen.

Use the internal pull-up resistors in this case. If not, use external pull-up or pull-down resistors to define the input-level.

The recommended way is to set the port input enable to "0", if a port pin is unconnected.

Never connect a potential divider with almost same resistor values.



Be careful with connection of input pins to other devices, which can go into High-Z states. Always use internal pull-up or external pull-up or pull-down resistors in this case.

Outputs from external circuits should always be connected via a serial resistor to a MCU input pin to prevent latch-up effects caused by under- or overshoots (4.2).

Debouncing and decoupling capacitors should always be chosen as smallest as possible. Please refer to chapter 4.2

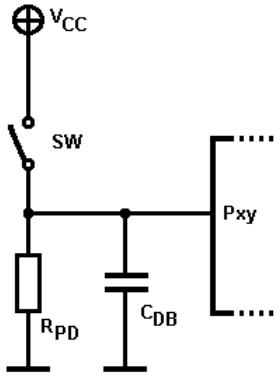
All pins are set to input disabled after its power-on default.

Do not connect any input ports directly to VCC or VSS (GND)! Always use pull up or down resistors (2k … 4k Ohms).

4.2 Latch-up consideration (switch)

Be careful with external switches to V_{CC} or ground together with debouncing capacitors connected to port pins.

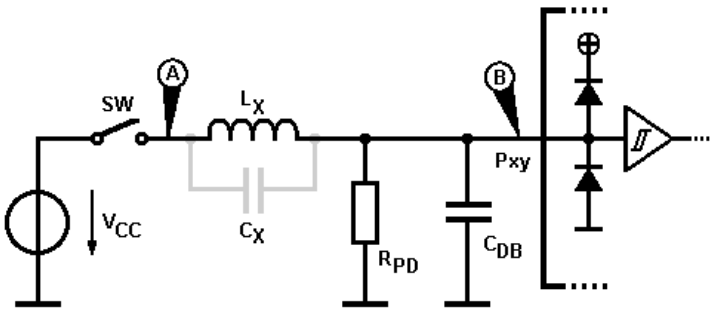
A usual configuration is shown in the following schematic:



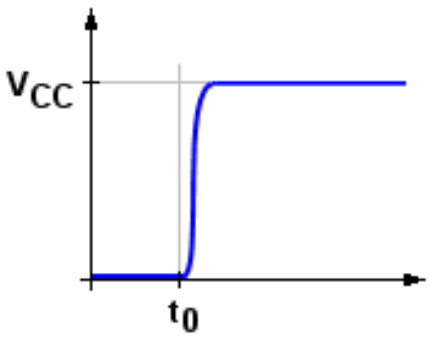
R_{PD} is a pull-down resistor and C_{BD} a debouncing capacitor. If the switch SW is open, a “0” is read from the port pin Pxy. If the switch is closed the input changes to “1”.

From the physical aspect, it has to be considered, that the switch is often placed in distance to the MCU by cable, wire, or circuit path. The longer the circuit path is the higher will be its inductivity L_X (and capacity C_X).

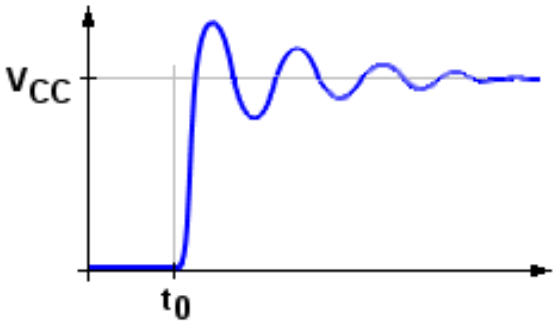
An equivalent circuit diagram looks like the following illustration:



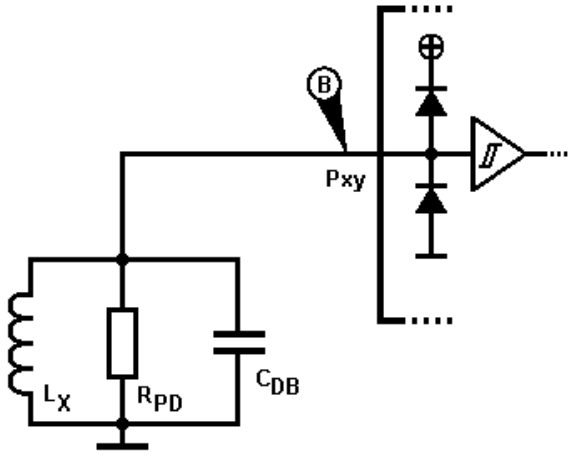
By closing the switch SW at time t_0 the following voltage can be measured at point (A):



But at the port pin Pxy on point (B) the following voltage can be measured:

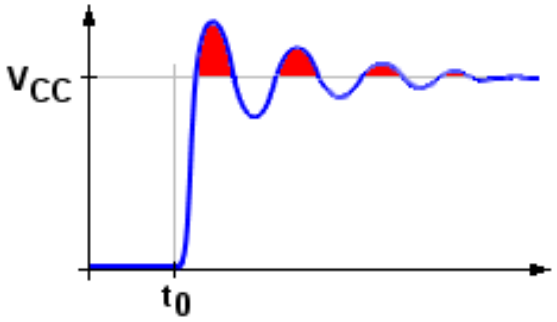


By closing the switch SW the circuit becomes a parallel oscillator with the wire-inductivity L_X, the debouncing capacity C_X and the damping R_{PD} of the pull-down resistor (Assume the power supply to be ideal, i. e. it has no internal resistance):



Because R_{PD} is often chosen high (> 50 K Ohms), its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin, drawn in red in the illustration below:



These overshoots may cause an internal latch-up on the port pin, because the internal clamping diode connected to V_{CC} becomes conductive. Similar is the effect, if the switch SW is opened. In this case there are under shoots on the port pin.

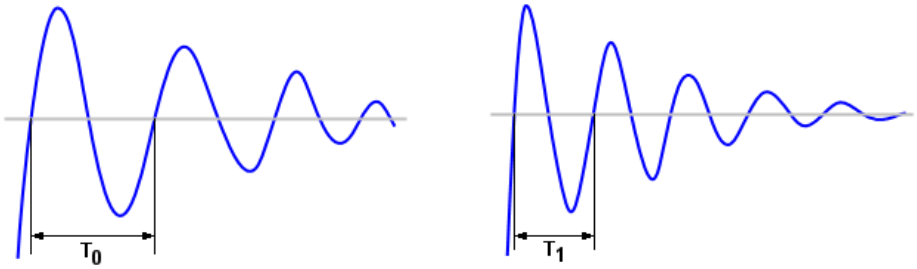
The frequency of the oscillation can be calculated by

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}} .$$

The inductivity L_X is the unknown value and depends on the PCB, its routing, and the wire lengths.

There are two counter measurements to prevent from latch-up.

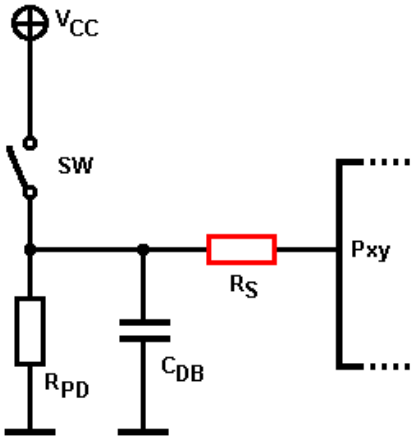
One solution is to decrease the capacity of the debouncing capacitor. This increases the oscillation frequency, and the over-all energy of the overshoots is smaller.



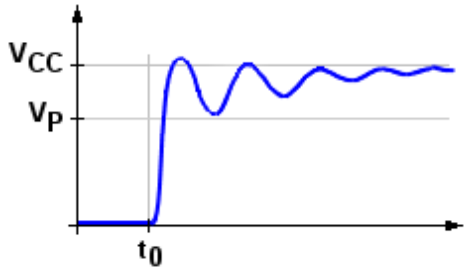
"big" capacity "small" capacity

This solution has two disadvantages: First the debouncing effect decreases and second, there is no guarantee, that the latch-up condition is eliminated.

A better solution is to use a series resistor at the port pin like in the following schematic:



The series resistor R_S reduces the amplitude of the oscillation and decreases the voltage offset at first. The resistor must not be chosen too high, so that the port pin input voltage V_P is within the positive CMOS/TTL/Automotive level.



5 Minimum Flash Programming Connection

This Chapter shows which Connections are needed for Programming

5.1 Run mode and Programming Mode

When using a target board, which normally operates in run mode, the mode pins of the MCU has to be set to MD0 = 1, MD1 = 1, MD2 = 0. It is possible to switch to serial programming mode via a connector. A programming device has to provide then certain voltage levels for the mode pins and port pins.

Additionally it is possible to enable USART scanning in run mode by setting the magic word at address `0xDF0034`. In this case the mode pins do not needed to be changed for programming and run mode. Programming is possible after Reset. If no communication is present after Reset, the application is started.

5.2 Programming Pins

For serial programming the following pins are affected:

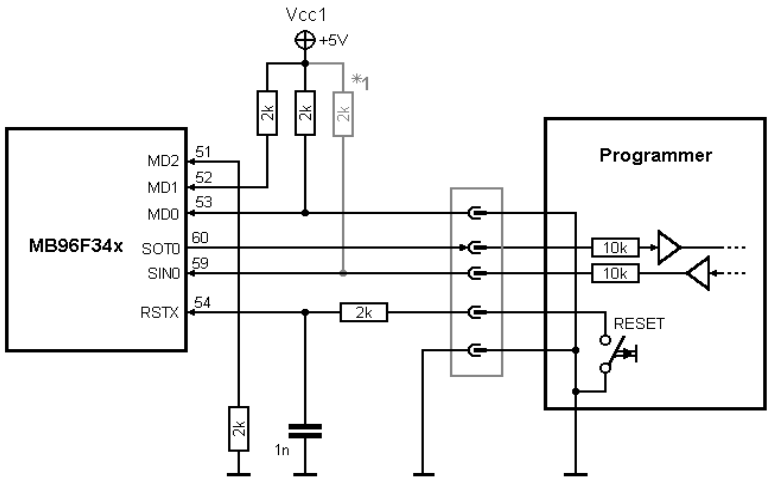
1. MD0
2. MD1
3. MD2
4. SINn
5. SOTn
6. SCKn (If synchronous programming is used)
7. RSTX

The electrical levels of the mode pins (MD0...2) are mandatory. These pins select the overall mode of the MCU after Reset (RSTX). The other pins are the communication pins of the USART (SINn, SCKn, SOTn).

In the examples below USART0 is used. Please refer to the Application Note *mcu-an-300224-e-16fx_mcu_flash_prog_bi_rom* for which USARTS can be used for programming.

5.3 Asynchronous Programming

The following schematic shows a possible configuration:



*1 please see chapter 6 for details

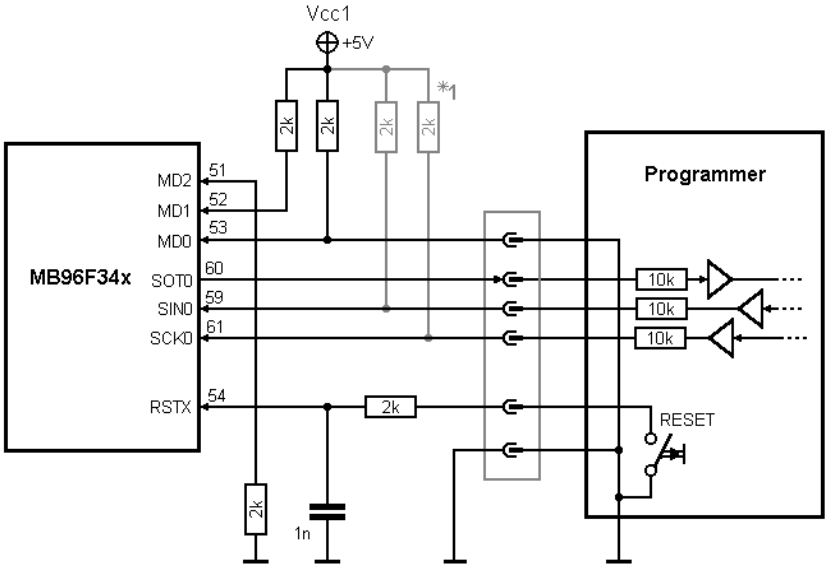
MD1 and MD2 can be directly connected to Vcc1 and ground, if these lines are short. If ESD pulses are to expect, two 2k pull-up and –down resistors have to be used, as shown in the schematic above.

When the programmer is connected, MD0 is connected to ground. This configuration with MD1 = 1 and MD2 = 0 the MCU is in serial programming mode then.

If USART scanning is enabled, the programmer connection to MD0 can be removed.

5.4 Synchronous Programming

The following schematic shows a possible configuration:



*1 please see chapter 6 for details

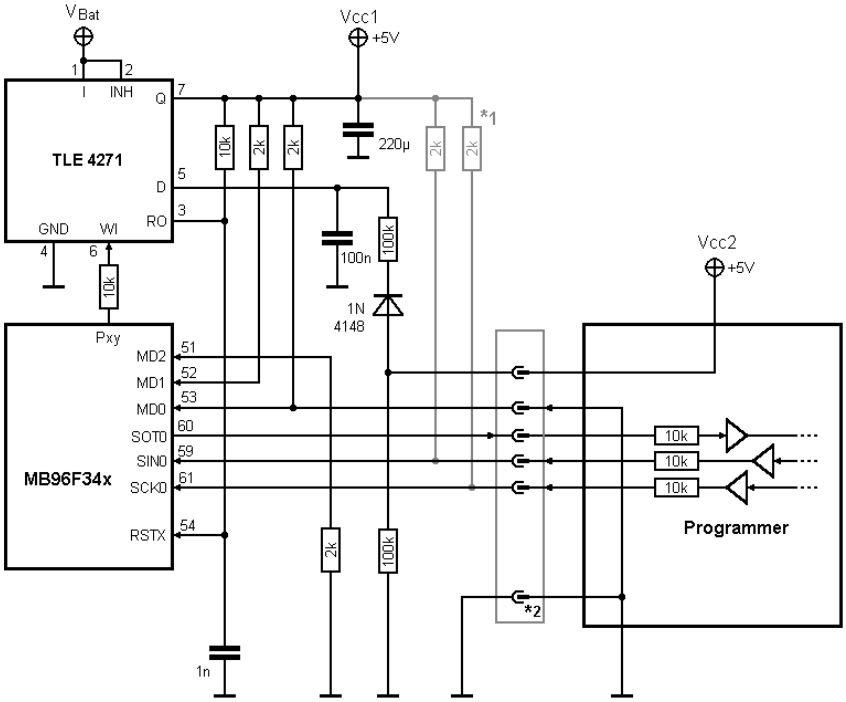
The recommendations for the port pin of SIN0 are the same as in the example above (5.3). Note, that SCK0 has to be threatened electrically equal to SIN0.

If USART scanning is enabled, the programmer connection to MD0 can be removed.

5.5 External Watchdog during Flash Programming

Assume an external watchdog is used, which is contained in many 5V Voltage regulators (e. g. TLE 4271). During flash programming the internal Burin-ROM code does not toggle the watchdog input and a reset would be performed. To prevent this, an additional circuit at the discharge capacitor can be used during programming mode. In this case the capacitor will not discharge and the watchdog itself will not perform a reset.

The following schematic shows a possible solution:



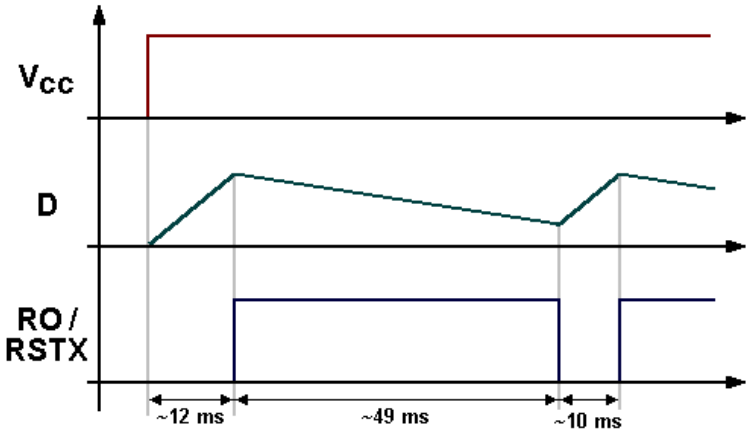
*1 please see chapter 6 for details

Assume the power of the MCUs circuits is off. Then the programmer is connected and the power is switched on – the reset phase begins. The “high level” from the Vcc2 connector of the programmer is used via a diode and a 100 k resistor to prevent the 100nF capacitor from discharging.

In normal run mode, the programmer is disconnected. The diode is insulating and even pulled-down, so that the capacitor for the watchdog is able to discharge again.

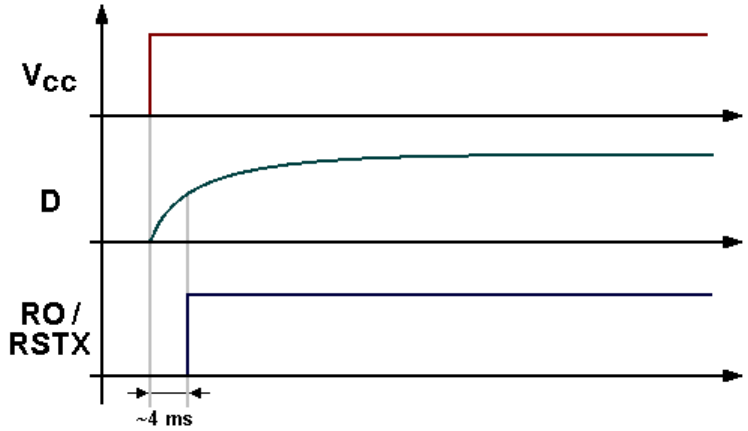
Connector at *2 can be removed with the connector chassis, if the ground levels of MCU board and programmer do not have a voltage pitch or shift. Additionally the MD0-ground connection can be removed, if USART scanning is enabled.

5.5.1 Timing Diagram of Run Mode



Note, that in this case the watch dog is not retriggered, so that the first watchdog reset occurs about 49 ms after the first power on reset.

5.5.2 Timing Diagram of Programming Mode



Note: The capacitor on the D-pin now is completely charged to 5 Volts, so that the power on reset time becomes shorter.

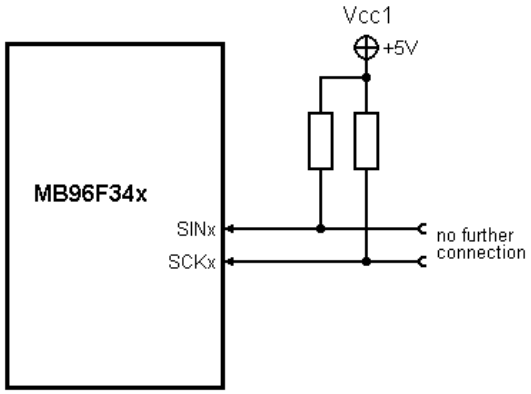
6 Background Debugging USART

Recommendation for BDM USART

6.1 Background Debugging Mode

If the Background Debugging Mode (BDM) is enabled with the magic word at address `0xDF0040`, the USART, which is configured for debugging, is enabled by the internal firmware after Reset. Therefore it is strongly recommended to terminate the SIN pin of this USART to V_{CC}, to avoid unwanted floating states at this input, disturbing the debugging mode.

The user application (if configured to auto-run) may not start or may stop during run time, when the SIN pin is left unterminated and unconnected.



Termination to system ground is *not* recommended, because the USART may interpret this as a start bit condition even if no falling edge occurred.

Note: If synchronous communication mode (not supported yet) is used, the same appears to the corresponding SCK pin.

7 Document History

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Document Number: 002-04772

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	MKEA	08/17/2006	Initial Release
			02/20/2007	Latch-up diagram corrected
			02/22/2007	C-pin with single ceramic capacitor X7R
			04/18/2007	Couple capacitors changed from 100nF to 10nF
			06/11/2007	BDM-USART recommendations added
*A	5060523	MKEA	12/22/2015	Migrated Spansion Application Note from MCU-AN-300223-E-V14 to Cypress format
*B	5834990	AESATMP8	07/27/2017	Updated logo and Copyright.

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