AN204771

F²MC-16FX Family, Alarm Comparator

This application note describes the functionality of the Alarm Comparator and gives some examples. The Alarm Comparator is used for detection of under-voltage or over-voltage conditions.

1 Introduction

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1.1 Key Features

- Detection of Under-Voltage and Over-Voltage by comparison of external voltage input with AVDD/AVSS or internal reference voltage
- Generation of Interrupt on detection of Under-Voltage or Over-Voltage condition
- Reference Voltage selectable as VREF or AVDD/AVSS
- Controlled power consumption by choosing appropriate power mode
- Run Mode by default (after power-on)

2 The Alarm Comparator

The Basic Functionality of the Alarm Comparator

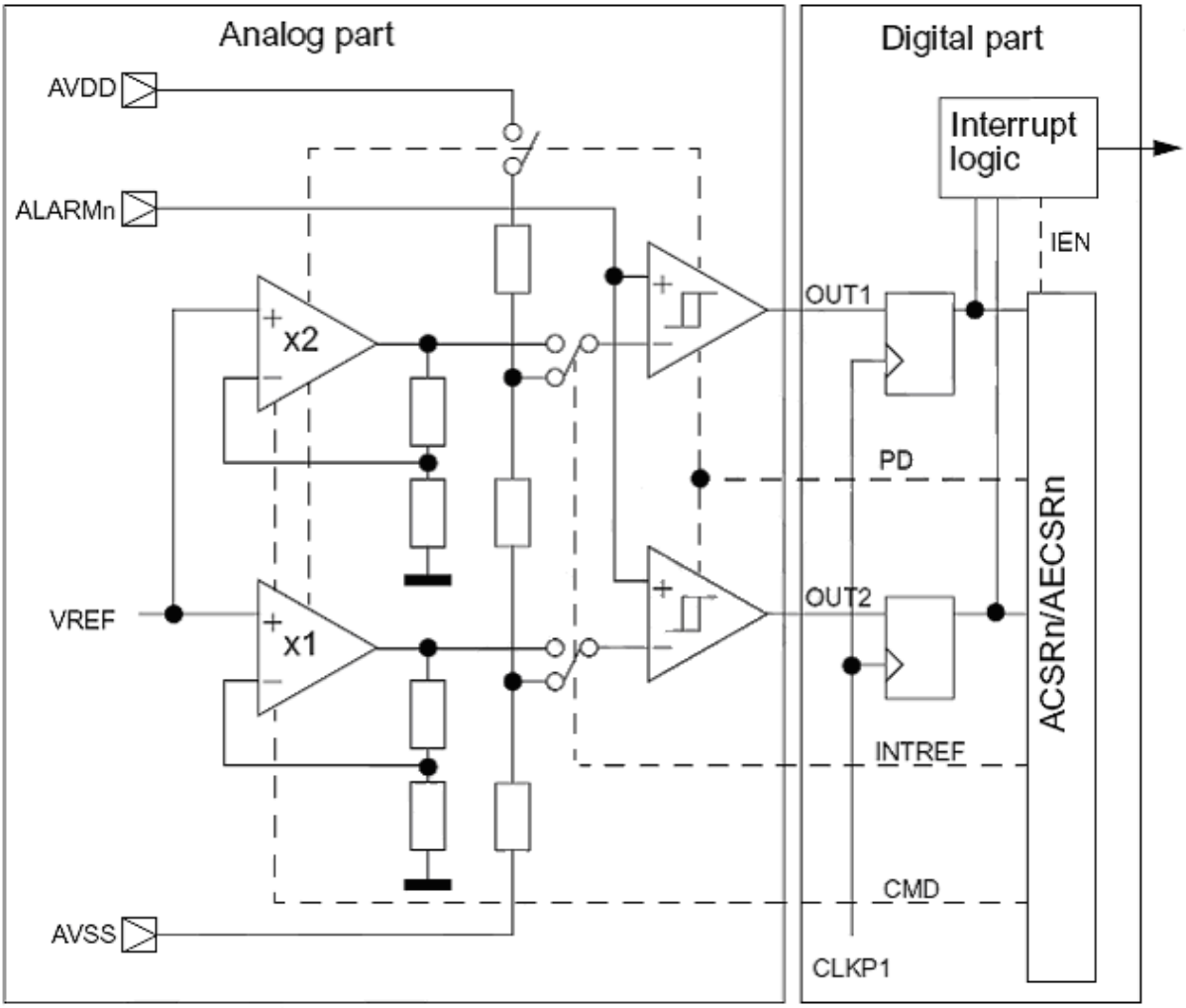
2.1 Introduction

The Alarm Comparator is used to detect under-voltage and over-voltage at an external analog input pin. It can be compared with AVDD/AVSS or an internal reference voltage. It can be switched to fast or slow detection mode. The slow mode reduces the power consumption of this module. By default, the alarm comparator is in run mode.

2.2 Block Diagram

Figure 1 shows the internal block diagram of the Alarm Comparator.

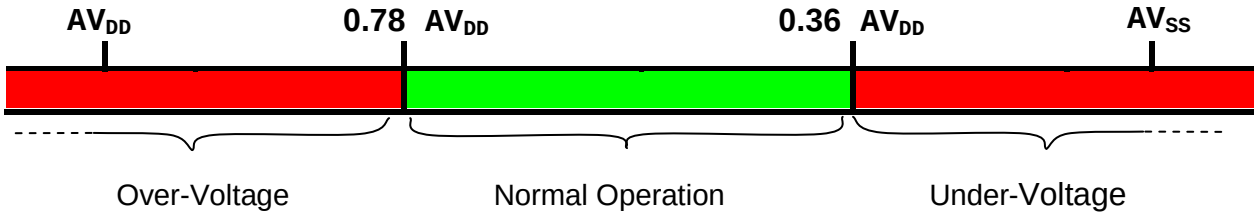
Figure 1. Alarm Comparator Block Diagram



2.3 Voltage Detection Areas

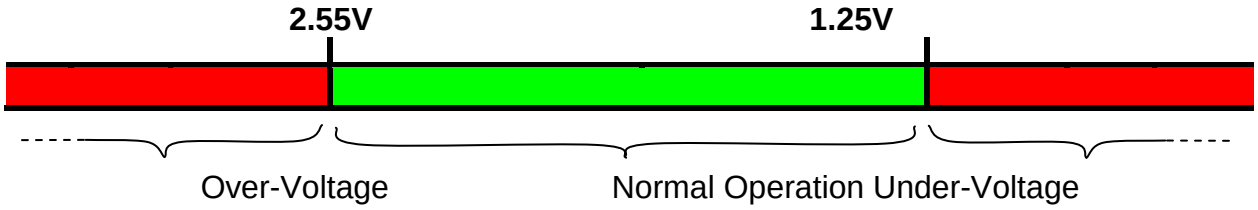
2.3.1 INTREF = 0 (AVDD/ADSS is Reference)

Figure 2. Voltage Detection Areas, INTREF = 0



2.3.2 INTREF = 1 (VREF is Reference)

Figure 3. Voltage Detection Areas, INTREF = 1



2.4 Standby Modes

It should be noted that the digital part of the alarm comparator is stopped in STOP or TIMER mode and it's operating in SLEEP mode. The analog part status is dependent on the PD bit of the ACSRn register. Hence it is possible to wake up only from the SLEEP mode (and not from STOP or TIMER mode) in the event of under / over voltage interrupts (if the analog comparator is in RUN mode and these interrupts are enabled).

Before switching to these modes it is advisable to put the alarm comparator in the power down mode, if the current consumption is critical for the application. For this purpose the interrupt should be disabled first and then alarm comparator should be put to power down mode.

2.5 Registers

2.5.1 Alarm Comparator Control/Status Register(ACSRn)

Table 1. ACSRn

Bit No.	Name	Explanation	Initial Value	Value	Operation	
7	CMD	Comparison Mode	0	0	Slow Mode (less power consumption)	
				1	Fast Mode (high power consumption)	
6	OVEN	Over-Voltage Interrupt Enable	1	0	No Interrupt in case of Over-Voltage	
				1	Interrupt in case of Over-Voltage	
5	UVEN	Under-Voltage Interrupt Enable	1	0	No Interrupt in case of Under-Voltage	
				1	Interrupt in case of Under-Voltage	
4	OUT2	Output of Alarm Comparator UV	X		AESCRn:INTREF=0	AESCRn:INTREF=1
				0	ALARMn< 0.36 *AVDD	ALARMn<1.25V
				1	ALARMn>0.36 *AVDD	ALARMn>1.25V
3	OUT1	Output of Alarm Comparator OV	X		AESCRn:INTREF=0	AESCRn:INTREF=1
				0	ALARMn<0.78 *AVDD	ALARMn<2.55V
				1	ALARMn>0.78 *AVDD	ALARMn>2.55V
2	IRQ	Interrupt Request	X	0	No Under-Voltage or Over-Voltage Condition detected	
				1	Under-Voltage or Over-Voltage Condition detected[1]	
1	IEN	Interrupt Enable	0	0	Disable Interrupt	
				1	Enable Interrupt	
0	PD	Power Down Mode	0	0	Run Mode (Analog Part)	
				1	Power Down Mode (Analog Part)	

States of OUT0 and OUT1 and Voltage Condition

Table 2. Analog Comparator Outputs in Different Voltage Conditions

OUT0	OUT1	Condition
0	0	Under-Voltage
0	1	Not possible
1	0	Normal Operation
1	1	Over-Voltage

[1]It should be noted that the IRQ bit will be set with the next positive transition of CLKP1 after detecting an interrupt event and it will remain set unless and until the under-voltage or over-voltage condition persists. In such situation if the IEN is set to 1, the interrupt service routine will be executed even after clearing the IRQ bit in it. Hence to clear an interrupt caused by a persistent Under-Voltage or Over-Voltage condition the OVEN and/or UVEN bits should be cleared first and then the IRQ bit should be cleared separately.

Alarm Comparator Extended Control/Status Register (AECSRn)

Table 3. AECSRn

Bit No.	Name	Explanation	Initial Value	Value	Operation
15 … 11	-	*Reserved Bits*	X	-	Always write 0 to these Bits
10	ACE	Analog Input Enable	0	0	Disable ALARMn Input
				1	Enable ALARMn Input
9	-	*Reserved Bit*	X	-	Always write 0 to this Bit
8	INTREF	Internal Reference Voltage Select	0	0	Select AVDD/AVSS for Reference Voltage
				1	Select VREF for Reference Voltage

3 Alarm Comparator Example

Example for the Alarm Comparator

3.1 Under-Voltage and Over-Voltage with AVDD and AVSS as Reference Voltage

In this example AVDD and AVSS are used for Reference Voltage. Please note that in this example the root cause for the Alarm Comparator interrupt is not reset. If under-voltage or over-voltage persists after the ISR, the interrupt is generated again. To prevent this, the IEN bit or OVEN and/or UVEN bits of theACSR0 may be set to “0” in the ISR before clearing the interrupt flag (IRQ).

Main.c

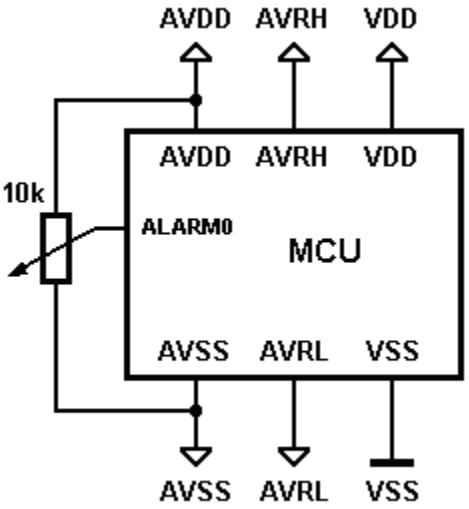
```
/* MICROELECTRONICS ACCEPTS NO RESPONSIBILITY OR LIABILITY FOR ANY ERRORS OR */
/* ELIGIBILITY FOR ANY PURPOSES.                                              */
/*----------------------------------------------------------------------------*/

void InitAlarmComp (void)
{
  ACSR0 = 0x62;  // Slow Mode, Over and Undervoltage, Interrupt enable, Run Mode
  AECSR0 = 0x04; // Analog Input Enable, AVDD/AVSS = Ref
}

/*----------------------------------------------------------------------------*/

void main(void)
{
  InitIrqLevels();
  __set_il(7);    // allow all levels
  __EI();         // globally enable interrupts

  InitAlarmComp();

while(1);
}

/*----------------------------------------------------------------------------*/

__interrupt void AlarmISR (void)
{
if (ACSR0_OUT1 && ACSR0_OUT2)
  {
// Overvoltage (Vin > 0.78 * AVDD)
    //
    // Do something...
  }
else
  {
// Undervoltage (Vin < 0.36 * AVDD)
    //
    // Do something...
}

  ACSR0 = 0x62;  // clear Interrupt
}
```

vectors.c

```
/* MICROELECTRONICS ACCEPTS NO RESPONSIBILITY OR LIABILITY FOR ANY ERRORS OR */
/* ELIGIBILITY FOR ANY PURPOSES.                                             */
/*---------------------------------------------------------------------------*/
void InitIrqLevels(void)
{
      . . .

      ICR = (77<< 8) | 2; // Priority Level 2 for Alarm Comparator 0 of
       // MB9634x Series
   . . .
}

/* ISR prototype */
__interrupt voidAlarmISR (void);

   . . .

#pragma intvect AlarmISR 77// Alarm Comparator of MB9634x Series

   . . .
```

With the following schematic, the code above can be tested easily.

Figure 4. Example Test Schematic



4 Additional Information

Information about Cypress Microcontrollers can be found on the following Internet page:

http://www.cypress.com/cypress-microcontrollers

The software example related to this application note is:

96340_alarmcomp

It can be found on the following Internet page:

http://www.cypress.com/products/16FX

5 Document History

Document Title: AN204771 - F²MC-16FX Family, Alarm Comparator

Document Number: 002-04771

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	MKEA	08/16/2006	Initial Release
			03/23/2007	Reviewed the document and updated with review findings
			08/14/2007	Updated with re-review findings
*A	5060512	MKEA	12/23/2015	Migrated Spansion Application Note from MCU-AN-300222-E-V12 to Cypress format
*B	5832403	AESATMP9	07/27/2017	Updated logo and copyright.
*C	6036665	NOFL	01/18/2018	Updated logo. Updated links. Updated Sales page and Copyright year.

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