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AN204415

FM3, Oscillator Control Method for Low Power Consumption Mode

This application note describes the method to control an oscillator from FM3 to achieve low power consumption.

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1 Introduction

This application note describes the method to control an oscillator from FM3 to achieve low power consumption.

When trying to achieve low power consumption while using an oscillator as the main clock of FM3, at the same time, it is required to control the current consumption of the oscillator itself. In general, the current consumption while the oscillator is operating is in the mA order. However, the current consumption on Standby Mode can be reduced to μA order. Users have to control the transitions to Standby Mode for the Oscillator manually.

The Low Power Consumption Mode of FM3 in this application note refers to the following modes.

- RTC Mode
- Stop Mode
- Deep Standby RTC Mode
- Deep Standby Stop Mode

The above four modes are described as “Low Power Consumption Mode” hereinafter.

For details of Low Power Consumption Mode of FM3, please refer to “FM3 PERIPHERAL MANUAL CHAPTER 6: Low Power Consumption Mode“.

1.1 Target Oscillators

In this application note, it is assumed that an oscillator is used as the Main Clock, which is supplied to FM3 externally. Targeted oscillators are those which have Standby Mode (STBY#) Control Pin and can be externally controlled to stop the oscillations.

In this application note, “Standby Mode” refers to the state which the oscillation stops in oscillators and “STBY**#**” refers to the Standby Mode Control Pin.

（STBY#：High = output oscillation, Low = stop oscillation）

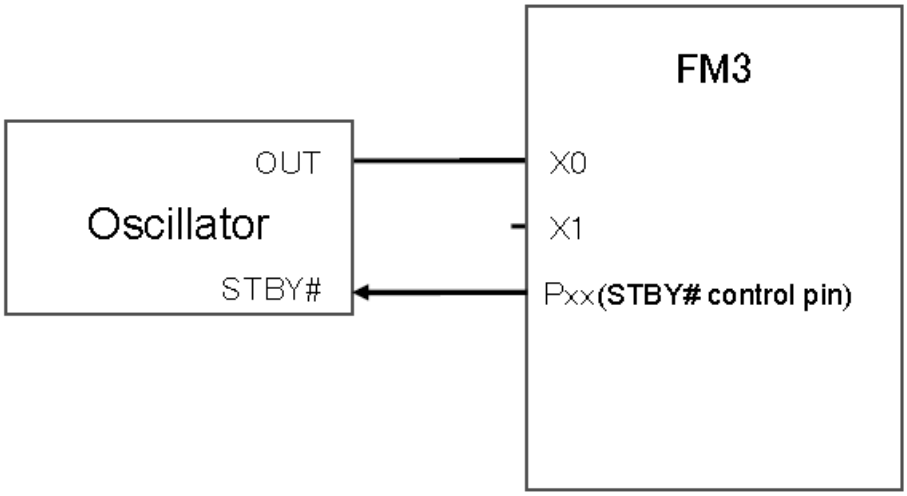
2 Controlling The Oscillator in Low Power Consumption Mode

2.1 Circuit Design

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The output of the oscillator (OUT) is connected to the external clock input pin of FM3(X0) and the standby control pin (STBY#) is connected to general-purpose I/O port of FM3. Do not connect X1 pin of FM3 to standby control pin (STBY#) of the oscillator.

Figure 1. Connection example of FM3 and oscillator

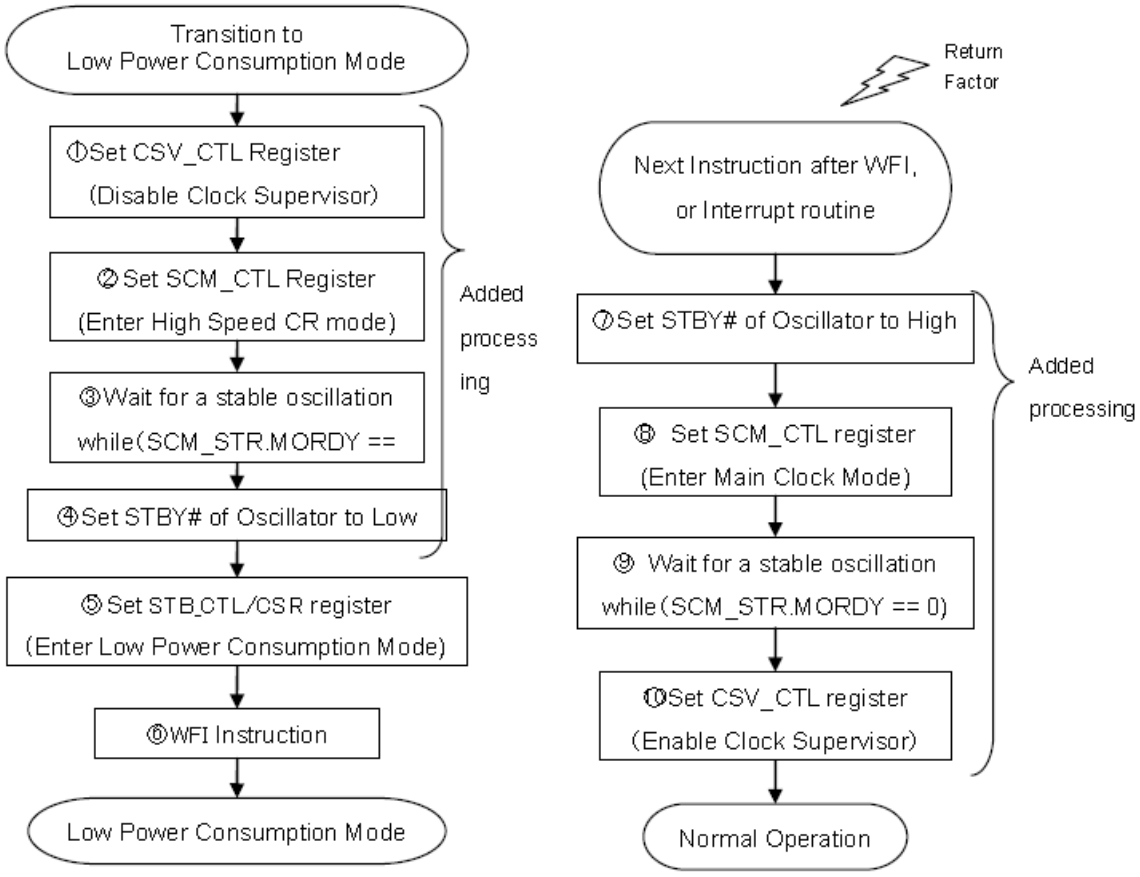


For details of the above port setting, please refer to “4.24 Special Port Setting Register (SPSR)” in “FM3 PERIPHERAL MANUAL CHAPTER 10: I/O Port”

2.2 Processing Flow

When conducting the transition to Low Power Consumption Mode on FM3, it is necessary to add the oscillator control process at the same time. Figure 2 shows the processing flows of transition to/return from Low Power Consumption Mode. The details of the processing flows are described below.

Figure 2. Processing flow charts of the transition to/return from Low Power Consumption Mode



The transition to Low Power Consumption Mode is executed by ⑤ setting the STB_CTL register of FM3 Low Power Consumption Mode function to STOP mode, setting the CRS register of Cortex-M3 core to DeepSleep, and ⑥ issuing the WFI instruction.

Please refer to “8.1 Standby Mode Control Register(STB_CTL)” in “FM3 PERIPHERAL MANUAL CHAPTER 6: Low Power Consumption Mode“ for the details of STB_CTL register, and refer to “System Control register” in “ARM Cortex-M3 Technical Reference Manual r2p0

Nested Vectored Interrupt Controller” for the CSR register.

It is necessary to ① disable Clock Supervisor (CSV) and ④execute Standby Mode transition of the oscillator before making the Low Power Consumption Mode transition. However, if the oscillator enters Standby Mode, the main clock of FM3 itself will not be supplied.

To avoid the above problem, ②It is necessary to switch the clock mode of FM3 to

High-speed CR Mode before putting the oscillator to Standby Mode. The clock mode is switched by setting the SCM_CTL register.

After switching to High-speed CR Mode, put the oscillator to Standby Mode by setting STBY# pin to Low.

If the oscillator enters the Standby Mode while CSV function is enabled, it will results in an abnormal clock operation. Therefore it is necessary to disable CSV function before the transition. CSV function is disabled by setting the CSV_CTL register.

The processing flow of return operation changes depending on the type of Low Power Consumption Mode used.

When returning from Stop Mode or RTC Mode, it is necessary to perform the return operation from Standby Mode immediately after the software operation (next instruction after WFI, or interrupt routine) starts.

The return operation is executed by ⑦setting STBY# pin High, ⑧changing the clock mode to Main Clock Mode, and ⑩enabling CSV function.

When returning from Deep Standby Stop Mode or Deep Standby RTC Mode, FM3 is reset immediately. Therefore, it is necessary to set STBY# pin to High within the startup process. After the clock mode is switched from Main Clock Mode to High speed CR Mode and vice versa, it is necessary to wait for the oscillation to stabilize. (③ and ⑨ in the processing flow chart) This is because the oscillation stabilization wait process is not executed by hardware , it is required to be executed by software processing when switching the clock mode.

2.3 Sample Program Explanation

As an example of implementation, the following sample program for Stop Mode transition is provided.

List 2.1 shows a sample source for the transition process to Stop Mode, and List 2.2 shows a sample source for the return process from Stop Mode, both included in the sample program.

In these sample sources, General-purpose I/O port P0A is used for STBY# of the oscillator. The numbers in the following sources ①-⑩ corresponds with the numbers described in Figure 2.

List 1. Implementation example of Stop Mode transition routine

```
/* enter STOP mode */
void enter_STOPmode()
{
  disable_CSV();                          ①      /* disable CSV function */

  FM3_CRG->SCM_CTL  = 0;                  ②      /* Set high-speed CR mode, PLLE & SOSCE & MOSCE = 0 */
  while ((FM3_CRG->SCM_STR & 0xe0) != 0); ③      /* wait before entering HS-CR mode */

  bFM3_GPIO_PDOR0_PA = 0;                 ④      /* XO STBY# to LOW */
  FM3_CRG->STB_CTL = FM3_CRG_STB_CTL_STM_STOP; ⑤ /* KEY=0x1ACC & STOP mode & SPL = 0 */
  SCB->SCR = SCB_SCR_SLEEPDEEP_Msk;

  __asm(" wfi");                          ⑥      /* Low Power mode */
}
```

List 2. Implementation example of Stop Mode return routine

```
/* exit STOP mode */
void exit_STOPmode()
{
  if ( ( FM3_CRG->SCM_STR & 0xe0) == 0) { /* only high-speed CR mode */

    bFM3_GPIO_PDOR0_PA = 1;               ⑦      /* XO STBY# to HIGH */
    FM3_CRG->SCM_CTL   = SCM_CTL_Val;     ⑧      /* Set Master Clock switch */

    if (SCM_CTL_Val & (1UL << 1)) {       ⑨      /* Main clock oscillator enabled ? */
      FM3_CRG->SCM_CTL |= (1UL << 1);             /* enable main oscillator */
      while (!(FM3_CRG->SCM_STR & (1UL << 1)));   /* wait for Main clock oscillation to stabilize */
    }
    if (SCM_CTL_Val & (1UL << 4)) {               /* PLL enabled ? */
      FM3_CRG->SCM_CTL  |= (1UL << 4);            /* enable PLL */
      while (!(FM3_CRG->SCM_STR & (1UL << 4)));   /* wait for PLL to stabilize */
    }

    enable_CSV();                         ⑩      /* enable CSV function */
  }
}
```

Software design points are summarized below.

- It is required to set Main Clock Oscillation Enable Bit to Disable before entering Low Power Consumption Mode. (SCM_CTL.MOSCE = 0, Processing ②)
  - In case of Main Clock Oscillation Enable Bit＝Enable, the hardware oscillation stabilization wait process is executed when returning from Low Power Consumption Mode. In case of Main Clock Oscillation Enable Bit＝Disable, the hardware oscillation stabilization wait process is skipped.
  - If the hardware oscillation stabilization wait process is executed when returning from Low Power Consumption Mode, the process will not be released indefinitely and the oscillator will be in Dead Lock state, because the oscillator will stay in Standby Mode and there will be no clock output.
- While entering Low Power Consumption Mode, it is necessary to always keep the output state of the general-purpose I/O port P0A (STB_CTL.SPL=0, Processing⑤)
  - If the output state is not kept and FM3 becomes Hi-Z, the Standby Mode could be unintentionally released and the oscillator could start to oscillate because generally, STBY# of oscillator is internally pulled up.

3 Precautions

The sample project which is included with this application note are created with IAR Embedded Workbench for ARM®(version 6.40).

4 Reference

- 32-BIT MICROCONTROLLER FM3 PERIPHERAL MANUAL (Fujitsu Semiconductor Limited, MN706-00002-5v0-E)
- Application Note “Transition to/Return from Low-power Consumption Mode”(Fujitsu Semiconductor Limited, AN706-00028-2v0-E)
- ARM Cortex-M3 Technical Reference Manual r2p0 (ARM Limited.)
- ARM Cortex-M3 Technical Reference Manual r2p1 (ARM Limited.)

※ This document is created based on the above documents.

Please get the latest version of each document when you refer to them.

5 Additional Information

5.1 Target products

This application note is described about below products;

(TYPE0)

Series	Part Number（without package suffix）
MB9A100A	MB9AF102NA,MB9AF104NA,MB9AF105NA MB9AF102RA,MB9AF104RA,MB9AF105RA
MB9B100A	MB9BF102NA,MB9BF104NA,MB9BF105NA,MB9BF106NA MB9BF102RA,MB9BF104RA,MB9BF105RA,MB9BF106RA
MB9B300B	MB9BF304NB,MB9BF305NB,MB9BF306NB MB9BF304RB,MB9BF305RB,MB9BF306RB
MB9B400A	MB9BF404NA,MB9BF405NA,MB9BF406NA MB9BF404RA,MB9BF405RA,MB9BF406RA
MB9B500B	MB9BF504NB,MB9BF505NB,MB9BF506NB MB9BF504RB,MB9BF505RB,MB9BF506RB

(TYPE1)

Series	Part Number（without package suffix）
MB9A110A	MB9AF111LA,MB9AF112LA,MB9AF114LA MB9AF111MA,MB9AF112MA,MB9AF114MA,MB9AF115MA,MB9AF116MA MB9AF111NA,MB9AF112NA,MB9AF114NA,MB9AF115NA,MB9AF116NA
MB9A310A	MB9AF311LA,MB9AF312LA,MB9AF314LA MB9AF311MA,MB9AF312MA,MB9AF314MA,MB9AF315MA,MB9AF316MA MB9AF311NA,MB9AF312NA,MB9AF314NA,MB9AF315NA,MB9AF316NA

(TYPE2)

Series	Part Number（without package suffix）
MB9B110T	MB9BF116S,MB9BF117S,MB9BF118S MB9BF116T,MB9BF117T,MB9BF118T
MB9B210T	MB9BF216S,MB9BF217S,MB9BF218S MB9BF216T,MB9BF217T,MB9BF218T
MB9B310T	MB9BF316S,MB9BF317S,MB9BF318S MB9BF316T,MB9BF317T,MB9BF318T
MB9B410T	MB9BF416S,MB9BF417S,MB9BF418S MB9BF416T,MB9BF417T,MB9BF418T
MB9B510T	MB9BF516S,MB9BF517S,MB9BF518S MB9BF516T,MB9BF517T,MB9BF518T
MB9B610T	MB9BF616S,MB9BF617S,MB9BF618S MB9BF616T,MB9BF617T,MB9BF618T
MB9BD10T	MB9BFD16S,MB9BFD17S,MB9BFD18S MB9BFD16T,MB9BFD17T,MB9BFD18T

(TYPE3)

Series	Part Number（without package suffix）
MB9A130LA	MB9AF131KA,MB9AF132KA MB9AF131LA,MB9AF132LA

(TYPE4)

Series	Part Number（without package suffix）
MB9B110R	MB9BF112N,MB9BF114N,MB9BF115N,MB9BF116N MB9BF112R,MB9BF114R,MB9BF115R,MB9BF116R
MB9B310R	MB9BF312N,MB9BF314N,MB9BF315N,MB9BF316N MB9BF312R,MB9BF314R,MB9BF315R,MB9BF316R
MB9B410R	MB9BF412N,MB9BF414N,MB9BF415N,MB9BF416N MB9BF412R,MB9BF414R,MB9BF415R,MB9BF416R
MB9B510R	MB9BF512N,MB9BF514N,MB9BF515N,MB9BF516N MB9BF512R,MB9BF514R,MB9BF515R,MB9BF516R

(TYPE5)

Series	Part Number（without package suffix）
MB9A110K	MB9AF111K,MB9AF112K
MB9A310K	MB9AF311K,MB9AF312K

(TYPE6)

Series	Part Number（without package suffix）
MB9A140NA	MB9AF141LA,MB9AF142LA,MB9AF144LA MB9AF141MA,MB9AF142MA,MB9AF144MA MB9AF141NA,MB9AF142NA,MB9AF144NA
MB9A340NA	MB9AF341LA,MB9AF342LA,MB9AF344LA MB9AF341MA,MB9AF342MA,MB9AF344MA MB9AF341NA,MB9AF342NA,MB9AF344NA
MB9AA40NA	MB9AFA41LA,MB9AFA42LA,MB9AFA44LA MB9AFA41MA,MB9AFA42MA,MB9AFA44MA MB9AFA41NA,MB9AFA42NA,MB9AFA44NA
MB9AB40NA	MB9AFB41LA,MB9AFB42LA,MB9AFB44LA MB9AFB41MA,MB9AFB42MA,MB9AFB44MA MB9AFB41NA,MB9AFB42NA,MB9AFB44NA

(TYPE7)

Series	Part Number（without package suffix）
MB9A130N	MB9AF131M,MB9AF132M MB9AF131N,MB9AF132N
MB9AA30N	MB9AFA31L,MB9AFA32L MB9AFA31M,MB9AFA32M MB9AFA31N,MB9AFA32N

(TYPE8)

Series	Part Number（without package suffix）
MB9A150R	MB9AF154M, MB9AF155M,MB9AF156M MB9AF154N, MB9AF155N,MB9AF156N MB9AF154R, MB9AF155R,MB9AF156R

(TYPE9)

Series	Part Number（without package suffix）
MB9B120M	MB9BF121K,MB9BF122K,MB9BF124K MB9BF121L,MB9BF122L,MB9BF124L MB9BF121M,MB9BF122M,MB9BF124M
MB9B320M	MB9BF321K,MB9BF322K,MB9BF324K MB9BF321L,MB9BF322L,MB9BF324L MB9BF321M,MB9BF322M,MB9BF324M
MB9B520M	MB9BF521K, MB9BF522K,MB9BF524K MB9BF521L, MB9BF522L,MB9BF524L MB9BF521M, MB9BF522M,MB9BF524M

Document History

Document Title: AN204415 - FM3, Oscillator Control Method for Low Power Consumption Mode

Document Number:002-04415

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NNAK	12/06/2012	First Edition.
*A	5655091	NNAK	03/09/2017	Converted Fujitsu Application Note “AN706-00057-1v0-E” to Cypress format
*B	5828170	AESATP12	07/27/2017	Updated logo and copyright.

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