The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
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AN204332

MB96300 to MB96600 Migration, F^{2}MC-16FX Family 16-Bit Microcontroller

Associated Part Family: Refer to Section 2

This application note compares MCUs of the MB96300 super series to MCUs of the MB96600 super series.

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1 Introduction

This chapter gives a small introduction about differences

This application note compares MCUs of the MB96300 super series to MCUs of the MB96600 super series.

The MB96300 super series consists of several different series with different pin-counts and pin-outs. These contain different peripheral types and a lot of different port-pin function shares. Both MB96300 and MB96600 super series are manufactured in 0.18 µm technology.

The MB96600 super series is pin based on the MB96300 super series. Migration from MB96300 to MB96600 is very easy.

Though different series with different pin-counts in MB96300 super series are available, for easy migration there are pin-based series of MB96600 super series available. Some global hardware topics for system setup are different, also some resources have been improved, nevertheless being downward compatible.

The emulation chip of the MB96300 super series is the MB96V300. For MB96600 super series there is no dedicated emulation chip available. For debugging devices of the F2MC Family 16-BIT MICROCONTROLLERMB96600 super series, the newly implemented On-Chip Debug Unit can be used.

2 Target products

This application note is described about below products;

Series	Product Number (not included Package suffix)
MB96310	MB96F313YS,MB96F313RS,MB96F313YW,MB96F313RW MB96F315YS,MB96F315RS,MB96F315YW,MB96F315RW
MB96320	MB96F326YS,MB96F326RS,MB96F326RW

Series	Product Number (not included Package suffix)
MB96330	MB96F336US, MB96F336UW MB96F338YS, MB96F338RS, MB96F338YW ,MB96F338RW, MB96F338US, MB96F338UW
MB96340	MB96345YS,MB96345YW, MB96345RS, MB96345RW MB96346YS, MB96346YW, MB96346RS, MB96346RW MB96F346YS, MB96F346YW,MB96F346RS, MB96F346RW MB96F347YS, MB96F347YW ,MB96F347RS, MB96F347RW MB96F348YS, MB96F348YW,MB96F348RS, MB96F348RW MB96F348HS, MB96F348HW, MB96F348TS, MB96F348TW MB96F345DS, MB96F345DW, MB96F345FS, MB96F345FW
MB96350	MB96F353YS, MB96F353YW, MB96F353RS, MB96F353RW MB96F355YS, MB96F355YW, MB96F355RS, MB96F355RW MB96F356RS, MB96F356RW, MB96F356YS, MB96F356YW
MB96370	MB96F378HS, MB96F378TS, MB96F378HW, MB96F378TW MB96F379RS, MB96F379YS, MB96F379RW, MB96F379YW
MB96380	MB96384YS MB96384YW,MB96384RS, MB96384RW MB96385YS, MB96385YW,MB96385RS, MB96385RW MB96F385YS, MB96F385YW, MB96F385RS, MB96F385RW MB96F386YS, MB96F386YW ,MB96F386RS, MB96F386RW MB96F387YS ,MB96F387YW, MB96F387RS, MB96F387RW MB96F388HS, MB96F388TS, MB96F388HW, MB96F388TW MB96F389YS, MB96F389YW ,MB96F389RS, MB96F389RW
MB96390	MB96F395YS, MB96F395YW, MB96F395RS, MB96F395RW
MB96610	MB96F612R, MB96F612A MB96F613R, MB96F613A MB96F615R, MB96F615A
MB96620	MB96F622R, MB96F622A MB96F623R, MB96F623A MB96F625R, MB96F625A
MB96630	MB96F633R, MB96F633A MB96F635R, MB96F635A MB96F636R MB96F637R
MB96640	MB96F643R, MB96F643A MB96F645R, MB96F645A MB96F646R MB96F647R
MB96650	MB96F653R, MB96F653A MB96F655R, MB96F655A MB96F656R MB96F657R
MB96670	MB96F673R, MB96F673A MB96F675R, MB96F675A
MB96680	MB96F683R, MB96F683A MB96F685R, MB96F685A

Series	Product Number (not included Package suffix)
MB96690	MB96F693R, MB96F693A MB96F695R, MB96F695A MB96F696R
MB966A0	MB96F6A5R, MB96F6A5A MB96F6A6R
MB966B0	MB96F6B5R, MB96F6B5A MB96F6B6R
MB966C0	MB96F6C5R, MB96F6C5A MB96F6C6R

3 On-Chip System Features

This chapter describes the global differences concerning the system features

Both MB96300 and MB96600 super series are very similar. The differences concerning system feature are listed in the following chapters.

3.1 Mode Setting

The assignment of the mode pin setting for the selected mode has changed.

For MB96300 there are three mode pins available, the assignment is shown in the following table:

Mode Pin Setting			MB96300
MD2	MD1	MD0	
0	0	0	External Vector Mode 0[*1]
0	0	1	External Vector Mode 1[*1]
0	1	0	Serial Communication Mode
0	1	1	Internal Vector Mode
1	0	0	Reserved
1	0	1	Reserved
1	1	0	External Vector Mode 2[*1]
1	1	1	Parallel Flash Programming mode

[*1]: Only available for devices with External Bus interface.

For normal use on MB96600 user application the number of mode pins is reduced to two. Following pins change accordingly:

- MD2 changes to MD
- MD1 is normally not available anymore for mode purposes, it is replaced by a GPIO pin
- MD0 changes to DEBUG I/F and gets additional functionality of serial debug interface

The assignment is shown in following table:

Mode Pin Setting		MB96600
MD	DEBUG I/F	
0	0	Serial Communication Mode
0	1	Internal Vector Mode

When migrating from a MB963xx series to a follower MB966xx series following modifications are necessary:

MD1 is not connected anymore for mode setting, can be used as GPIO.

MD2 is now called MODE but connected like before to Low via pull-down resistor.

MD0 is now called DEBUG I/F, but connected like before to High via a pull-up resistor.

Additional for debugging there is a connection to a series resistor from this DEBUG I/F to the debug interface, please see chapter 4.4 Debug Environment for further details.

Without the need of debugging for both modes “Serial Communication Mode” and “Internal Vector Mode” the wiring of MD (former MD2) and DEBUG I/F (former MD0) is the same for MB96300 and MB96600 super series. The only exception is MD1, which now can be used as GPIO (P17_0).

Table 1. Mode Pin Settings

Mode Pin Setting MB96300			Function	Mode Pin Setting MB96600		
MD2	MD1	MD0		MD	P17_0	DEBUG I/F
0	0	0	External Vector Mode 0[*1]	Not available		
0	0	1	External Vector Mode 1[*1]	Not available		
0	1	0	Serial Communication Mode	0	-	0
0	1	1	Internal Vector Mode	0	-	1
1	0	0	Reserved	Not available		
1	0	1	Reserved	Not available		
1	1	0	External Vector Mode 2[*1]	Not available		
1	1	1	Parallel Flash Programming mode	1	1	1

3.2 Clock Generation and Distribution

The MB96600 super series uses nearly the same clock unit as used in the MB96300 super series, too. The difference is that in MB96600 super series there are no devices with two possible hardware configurations concerning sub oscillator. In MB96300 super series there were parts with and without sub clock oscillator, coded by a suffix in the naming. In MB96600 super series all parts have an optional sub clock oscillator. This sub clock can be enabled by a marker in a dedicated flash area.

The maximum PLL frequency of MB96600 super series is 32 MHz MB96600 super series and must be considered. So in this case some prescaler settings have to be changed, if required.

	MB96300	MB96600
Main Clock	Yes	Yes
PLL	Yes	Yes
PLL Clock Modulator	Yes	No
Sub Clock	Yes[1]	Yes[2]
RC Clock (100 kHz and 2 MHz)	Yes	Yes
CLKP1	Yes	Yes
CLKP2	Yes	Yes
Max CPU Frequency [MHz]	56 / 40[3]	32

[1] Not available on devices with ‘S’ suffix.

[2:] Available on all devices, can be activated by a marker in flash area

[3:] 40MHz only if Low leakage RAM is implemented (MB96F345 / F378 / F379 / F385 / F388 / F389 / F395)

3.3 Memory Space

In contrast to MB96300 super series the peripheral memory access area is extended to the bank 0x0E for additional features of the peripherals. Registers which were available in MB96300 super series devices are at the same addresses in MB96600 super series devices.

3.4 Boot Rom

In the MB96600 series there are some new features added in the ROM configuration block (RCB). Take into account that the boot program execution also changed accordingly.

Below a list of added/changed features in the Boot Configuration Block (BCB):

- Block of debug interface connection
- NMI activation
- Location of interrupt vector table in the Table Base Register (TBR)
- Activation of sub oscillator
- Watch dog timer settings
- Locking the low voltage detection reset function

For details it is referred to the *start.asm* file

3.5 Reset

The reset handling in case of low voltage is enhanced by employment of low voltage interrupt. This one facilitates the user to execute an Interrupt Service Routine (ISR) before the reset.

In the MB96600 series there is no internal pull-up resistor at the reset pin.

Table 2. Internal Pull-Up Resistor at the Reset Pin

	MB96300	MB96600
Internal pull-up resistor at the reset pin	Yes	No

3.6 On-Chip Debug Unit (OCDU)

In the MB96600 super series an on chip debugger unit is implemented. As it is possible to read out the memory in general, the user can forbid memory access via the On-chip debug unit (OCDU).

Further information about debugging can be found in chapter 5.4.

3.7 Memory Patch Function

In the MB96600 super series the memory patch function is removed. The break point functionality is covered by the new OCD unit (see 3.6)

3.8 Standby Mode and Voltage Control Circuit

3.8.1 Voltage Control Circuit

The low power handling modes A and B of the on-chip core voltage regulator were changed. Besides these changes permitted output voltage levels of the internal voltage regulator were changed, too.

Table 3. Permitted Core Power Mode B Depending on Different Operation Modes

Operation mode	Permitted Core Power Mode B	
	MB96300	MB96600
Stop mode	yes	Yes
Sleep Mode	No	No
Timer Mode	No	No

In the next table a reduced number of permitted configurations for using low power mode A is shown in case of MB96600.

Table 4. Permitted Configurations for Manually Using Low Power Mode A

<table>
<tr><th></th><th colspan="5">Permitted Configurations for Using Low Power Mode A</th></tr>
<tr><th>Operation Mode</th><th>MB96300</th><th>MB96600</th><th>RC Oscillator</th><th>Main Oscillator</th><th>PLL</th><th>Sub Oscillator</th></tr>
<tr><td>RC run</td><td>Yes[1]</td><td>No</td><td rowspan="2">Active (set to 100 kHz)</td><td rowspan="3">Active with f_{osc} ≤ 4 MHz
or disabled</td><td rowspan="9">Disabled</td><td rowspan="5">Active or disabled</td></tr>
<tr><td>RC sleep</td><td>Yes[1]</td><td>No</td></tr>
<tr><td>RC sleep[2]</td><td>No</td><td>Yes</td><td rowspan="2">Active
(set to 100 kHz or 2 MHz)</td></tr>
<tr><td>RC timer</td><td>Yes</td><td>Yes</td><td rowspan="3">Active
(set to 100 kHz or 2 MHz) or disabled</td></tr>
<tr><td>Main sleep[2]</td><td>Yes</td><td>Yes</td><td rowspan="2">Active with f_{osc} ≤ 4 MHz</td></tr>
<tr><td>Main timer</td><td>Yes</td><td>Yes</td></tr>
<tr><td>Sub run</td><td>Yes[1]</td><td>No</td><td rowspan="3">Active with f_{osc} ≤ 4 MHz
or disabled</td><td rowspan="3">Active</td></tr>
<tr><td>Sub sleep[2]</td><td>Yes[1]</td><td>Yes</td></tr>
<tr><td>Sub timer</td><td>Yes</td><td>Yes</td></tr>
</table>

[1]: System clock 2 must be set to RC clock or sub clock. 2 MHz setting of RC is not permitted as system clock 2 in run or sleep mode.

[2]: System clock 2 must be set to Main clock, RC clock or Sub clock

3.8.2 Standby Mode

In the MB96600 super series the standby mode operation was extended by two functionalities:

- Flash power-down in standby mode
- Core bus start delay

For better understanding about the new functionalities a short description follows:

- Flash power-down in standby mode: The Flash can be powered down by switching the MCU into standby mode.
- Core bus start delay: With this function high current consumption is reduced during leaving MCU from standby mode to run mode by configuration of a delayed core bus start.

3.9 Interrupts

The interrupt vector table of MB96600 super series is different from interrupt table of MB96300 super series. But all devices of MB96600 super series have the same interrupt table (interrupt vector of a interrupt source has same interrupt number on all devices of MB96600 super series)

4 Peripherals

This chapter describes differences of the on-chip peripherals.

4.1 Changed Peripherals

4.1.1 I/O Address Area

In general in MB96600 super series old peripheral registers, known in MB96300 super series, are located on the same addresses. New introduced registers within one peripheral are out of the 16-bit access area. In these cases "__far" accesses must be executed.

4.1.2 Flash Memory

The flash macros used in MB96300 and MB96600 super series are different.

In MB96300 there are two different types of flash macros: a main flash with a sector size of 64 kB and a data flash with a sector size of 16 kB. For some devices there exists alternatively a Satellite flash with a sector size of 8 kB.

For MB96600 super series a completely different macro is used. It is called dual-operation-flash and consists of two banks with different sizes: The bank B sector size is 8 kB and is normally used for data storage or boot loaders, bank A has a sector size of 64 kB and is used for program storage. With this dual operation flash it is possible to read or execute from one bank while erasing or writing to the other one. Following table shows the differences:

Table 5. Differences of Flash Types and Sizes

	MB96300	MB96600
Program	Main Flash sector size of 64 kB	Dual Operation Flash sector size of bank A of 64 kB
Data	Data Flash sector size of 16 kB or Satellite Flash Sector size of 8 kB	Dual Operation Flash sector size of bank B of 8 kB

The performance of the flash macros differs in following way:

Table 6. Differences of Flash Performance with Zero Wait States

	MB96300	MB96600
Performance with zero wait state	Up to 28 MHz CLKB	Up to 32 MHz CLKB

Due to the performance changes and the new command sequencer mode, which can be used, the complex memory timing setup disappeared.

4.1.3 Watchdog Timer (WDG)

The concept of the watchdog differs between MB96300 and MB96600 super series. For MB96600 the watchdog is equipped with window-based functionality and is enabled by default after a reset. Following table shows the differences:

Table 7. Differences of Watchdog Timer

	MB96300	MB96600
Watchdog state after reset	disabled by default can be enabled by user software	enabled by default can be disabled by user software
Watchdog window-based	No	yes, watchdog is downward compatible to MB96300
WICM Marker for default interval time in BCB	No	Yes
Unlock of WDG via pattern sequence	No	Yes (once)

4.1.4 Programmable Pulse Generator (PPG)

The PPG of the MB96600 super series is fully downward compatible to the PPG of the MB96300 super series. But there were made some improvements:

Table 8. Differences of Programmable Pulse Generator

	MB96300	MB96600
Division from 16-bit PPG to two separate 8-bit PPGs	No	Yes
Triggering of ADC by PPG	No	Yes
Programmable Start delay[1]	No	Yes
Selection of all available RLT as clock source	No	Yes
Common trigger for all PPGs	No	Yes
Ramp mode[1]	No	Yes
Types of Interrupts: define timing point match within the PPG cycle end duty match during the ramp mode operation	4 No No	6 Yes Yes

1: Feature not available on all MCUs. Check for availability in corresponding data sheet.

As the 16-bit PPG counter can be divided into two 8-bit counters, two outputs are implemented for one PPG module. So in case of 16-bit resolution both outputs can drive the same (or inverted) signal, whereas in case of division into two 8-bit counters there are also two different output signals finally.

These extensions are not available for all MB96600 devices. Please refer to datasheet accordingly

4.1.5 USART

Despite enhancements and new features, as for instance 16-byte Rx/Tx FIFO buffer and LIN extensions, the USART module of the MB96600 is software downward compatible to MB96300.

Take for note, that bit timing and handling of Tx- and Rx-flags differ to MB96300 minimally. For detailed description, it is referred the hardware manual.

In the following table main differences within the USART are listed:

Table 9. Differences of USART

USART	MB96300	MB96600
16-byte Rx/Tx FIFO[1]	No	yes
LIN Auto baud rate generation / adjustment (without ICU)[2]	No	Yes
LIN checksum generation / verification [2]	No	Yes
Automatic LIN header transmission / detection[2]	No	Yes
LIN bus error detection[2]	No	Yes
LIN internal loop back feature[2]	No	Yes
SSR:TDRE/RDRF Bit timing	Changed, but backward compatible	
Extended interrupt sources	No	Yes
SPI baud rates > 6Mbit/s	No	Yes

1: Not in all MCUs available. Check for availability in data sheet

2: Not all USART instances have extended LIN features. USART modules with extended LIN features are listed in the product lineup of datasheet.

4.1.6 A/D Converter (ADC)

The enhanced A/D converter module of the MB96600 super series is downward compatible to MB96300. The following table shows the differences.

Table 10. Differences of AD Converter

ADC	MB96300	MB96600
Range comparator	No	Yes
Channel skip by Scan Disable Function[1]	No	Yes
Pulse detection for range comparator[1]	No	Yes
Eight A/D data buffers for conversion results[1]	No	Yes
Separate A/D converter trigger (see chapter 4.2.1)	No	Yes
Stop Mode	Yes	Yes Renamed to: Pause Mode

1: This extension is not available for all MB96600 devices. Please refer to Data Sheet accordingly

4.1.7 I/O Ports

The I/O cells were changed from MB96300 to MB96600 due to cost reduction. Main restriction is that the input level is fixed on MB96600 super series devices. Also driving strength and availability of pull-down resistors were changed (details see in chapter 5.5).

4.1.8 16-Bit Reload Timer (RLT)

Beside the new added TIN latch function the MB96600 16-Bit reload timer is fully downward compatible to MB96300.

Table 11. Differences of the 16-bit Reload Timer

RLT	MB96300	MB96600
TIN latch function	No	yes

4.1.9 Direct Memory Access (DMA)

The DMA module of the MB96600 super series is fully compatible to MB96300. In case of the DMA handling with respect to the USART transmission the software handling is compatible, but the improved implementation can be applied. For details it is referred for the hardware manual.

4.1.10 ROM Configuration Block

The access bit width to FLASH security marker in the Boot ROM was changed.

Table 12. Differences of the Access Bit Width to FLASH Security Marker

Flash Security Marker	MB96300	MB96600
The access bit width	8 bit	16 bit

4.2 New Peripherals

In this chapter only new peripherals on MB96600 super series are presented.

4.2.1 A/D Converter Trigger

One new module is the A/D converter trigger, which facilitates a triggering via PPG and RLT timer.

Following events can be selected as trigger:

- Timing point events from PPG
- Trigger due to the RLT timer output change
- External pin

4.2.2 Quadrature Position/Revolution Counter (QPRC)

The Quadrature Position/Revolution Counter (QPRC) is a new peripheral, which is applied for rotary encoding.

Alternatively the QPRC can be used as up/down counter.

4.3 Unchanged Peripherals

All other peripherals are equal between MB96300 and MB96600 super series.:

- Source Clock Timer
- 16-Bit I/O Timer
  - 16-bit Free-Running Timer (FRT)
  - Output Compare Unit (OCU)
  - Input Capture Unit (ICU)
- External Interrupts
- 400 kHz I2C Interface
- CAN controller
- Clock Output Function
- Real Time Clock
- Clock Calibration Unit
- Stepper Motor Controller
- Sound Generator
- ROM/RAM Mirroring Module

Some MB966xx series MCUs which are successors of MB963xx series MCUs (e.g. MB96310 → MB96610) may differ in terms of available peripheral instances. Please check the datasheet for availability of peripheral instances.

4.4 Unavailable Peripherals

As follows there is a list of all removed peripherals on MB96600 super series:

- Alarm Comparator
- Clock Modulator
- External Bus Interface
- USB

5 Hardware Environment and Electrical Characteristics

Main Differences in the Hardware Environment

5.1 Introduction

In this chapter the most important changes within hardware environment are presented. Nevertheless a detailed investigation of the datasheet is recommended.

5.2 Pin Assignment

The availability of some peripherals from one MB963xx series to the follow-up MB966xx series (e.g. MB96310 → MB96610) changed in some cases. So MB96600 super series is **not** 100% pin compatible to MB96300 super series.

Please check for all available instances of every peripheral and the pin assignment in the corresponding datasheet.

5.3 Mode Pins

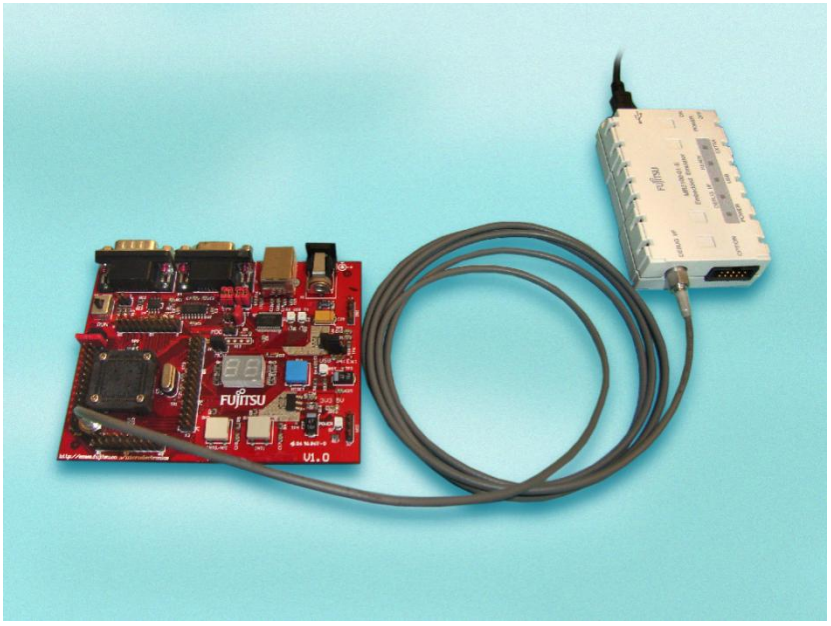
The number of mode pins changed in MB96600. For details about the mode pin settings see chapter 3.1.

5.4 Debug Environment

In MB96300 super series there are two possibilities for debugging: usage of emulator with EVA-chip and the low-cost alternative to debug the system via USART in the background debugging mode. Disadvantage of the latter solution is that the USART, which is used for debugging, is not available anymore for user application. On host system side the third-party debug tool EUROScope is necessary.

For MB96600 super series debugging is handled in a different way. The devices support on-chip-debugging via a single-wire interface. The according pin is called DEBUG I/F and is used exclusively for debugging purposes. Advantage of this kind of debugging is that target application can be debugged in real-time and in-system. There is no influence of additional adapter boards and probe cables. The on-chip-debugging also supports the feature to debug an already running application board from the field because the debugging system supports hot-plugging. The required hardware connection between application board and emulator box is very simple. This can be seen in the following figure:

Figure 1. Target Board with Single-Wire Connection to Emulator MB2100-01-E



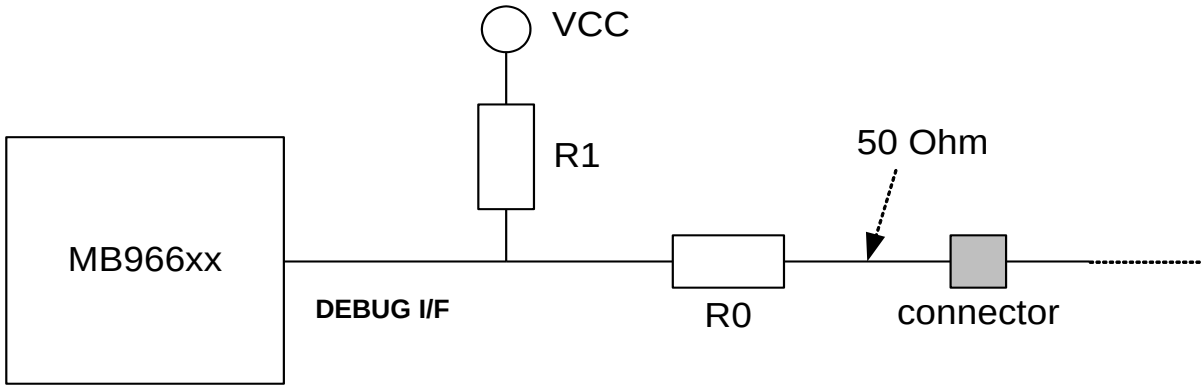
Only a series resistor and a pull-up resistor are necessary for the connection between MB2100-01-E emulator box and target application. Take into consideration, this pin (DEBUG I/F) is also used as mode pin. The emulator itself is connected to the development PC via a USB 2.0 interface. The emulator is fully supported by SOFTUNE V3 Workbench (ProPack Revision 300023 or later).

With the new Cypress debug tool there is no debug support by EUROScope for the MB96600 any more available.

Table 13. Differences in Debug Support

Debug Support	MB96300	MB96600
SOFTUNE V3	Yes	Yes min: V03L36 (ProPack rev300023)
EUROScope	Yes	No
Debug HW	MB2198-01-E + MB2198-500-E + MB2198-5xx-E (socket adapter) + EVA-Chip MB96V300	MB2100-01-E

Figure 2. Diagram of Debug Connection



Note: Please check for detailed OCDS layout design rules the MB2100-01-E manual and the chapter 'OCD' of the hardware manual.

5.5 I/O Ports

The I/O cells were changed from MB96300 to MB96600 due to cost reduction. Main restriction is that four input levels are not available for all pins anymore. Also driving strength and availability of pull-down resistors were changed. Following sub-chapters list the differences in more detail.

5.5.1 Input levels

The available input levels are listed in following table:

Table 14. Differences of Input Levels

Input Level	MB96300	MB96600
CMOS hysteresis 0307 High = 0.7 x VDD Low = 0.3 x VDD	all ports	CAN RX, USART SIN, SCK I2C
Automotive hysteresis High = 0.8 x VDD Low = 0.5 x VDD	all ports	all ports other than: CAN RX, USART SIN, SCK I2C
TTL High = 2.0 V Low = 0.8 V	all ports	DEBUG I/F
CMOS hysteresis 0208 High = 0.8 x VDD Low = 0.2 x VDD	all ports	RSTX

5.5.2 Driving strength

The driving strength of the output drivers is reduced like mentioned in the following table:

Table 15. Differences of Driver Strength

	MB96300	MB96600
Selectable driving strengths	2 mA, 5 mA, 30 mA (only some GPIOs)	4 mA, 30 mA (only some GPIOs)

5.5.3 Availability of internal pull-up- and pull-down resistors

The possibility of selecting internal pull-up or pull-down resistors is changed like mentioned in following table:

Table 16. Differences of Available Internal Resistor

Internal Resistor	MB96300	MB96600
Pull-down resistors	no	available on some pins (depends on device)
Pull-up resistors	yes	yes

5.6 Smoothing Capacitor

The smoothing capacitor Cs at the C-pin changed:

Table 17. Differences of Applied Capacitor at C-Pin

	MB96300	MB96600
Cs	4.7 µF (X7R)	1 - 4.7 µF (X7R)

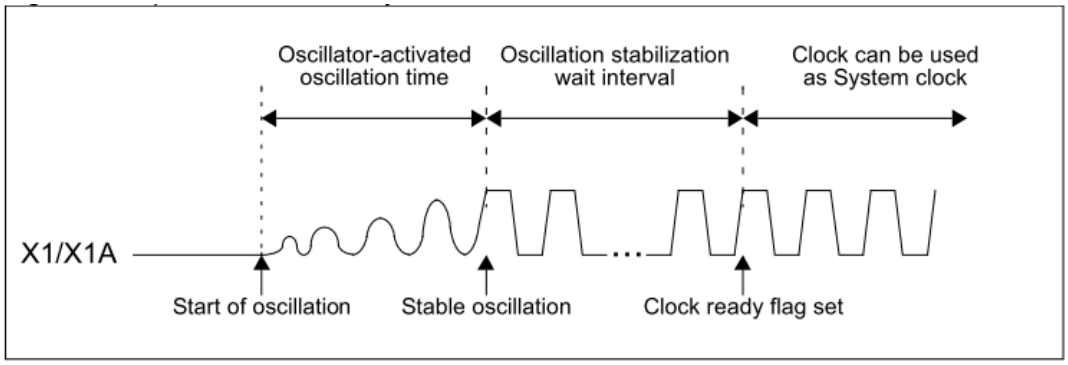
5.7 AC Characteristics

5.7.1 Stabilization Time

Beside reduction of the oscillation stabilization time, the reset extension counter is shared by the power on reset and external reset. This counter has 8-bit resolution, instead of 10-bit.

Table 18. Differences of Stabilization Time After Reset

Stabilization Time [RC cycles]	MB96300	MB96600
Power reset	700 + RC clock stabilization time	200 + RC clock stabilization time
External reset		
RC clock stabilization time	64(2MHz,100kHz)	256(2MHz) 16(100kHz)



5.7.2 Main clock input characteristics

The main clock input maximum frequency was changed in MB96600 series.

Table 19. Main Clock Input Characteristics

	MB96300	MB96600
Main clock input frequency (Max.)	16MHz	8MHz

5.8 Reset pin (RSTX)

The internal pull up resistor of the reset input pin RSTX was removed in MB96600 series. It is strongly recommended to add an external pull up resistor.

Table 20. Reset Input Pin

Reset Input pin	MB96300	MB96600
Internal pull up	Yes	No

6 Document History

Document Title: AN204332 - MB96300 to MB96600 Migration, F^{2}MC-16FX Family 16-Bit Microcontroller

Document Number: 002-04332

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	KHAS	06/11/2012	Rev 1.0 Initial Release
			01/31/2013	Rev 2.0 Added chapter “3.1.10 ROM Configuration Block“
			01/31/2014	Rev 2.1 Company name and layout design change
*A	5039827	KHAS	12/09/2015	Migrated Spansion Application Note from AN704-00004-2v1-E to Cypress format
*B	5787637	AESATMP9	06/27/2017	Updated logo and copyright.

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