AN2027

# PSoC® 1 - 32.768-kHz External Crystal Oscillator

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Associated Part Family: CY8C29x66, CY8C27x43, CY8C24x23A, CY8C28xxx, CY8C2xx45

Many microcontroller applications require a timing source more accurate than the typical internal oscillator. An external crystal can provide a solution. These crystals are used with an external crystal oscillator (ECO) to generate clocks as accurate as ±50 parts per million. PSoC® 1 can implement an ECO that uses a 32.768-kHz crystal.

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## 1 Introduction

PSoC 1 microcontroller's external crystal oscillator (ECO) can be used as a reference for timekeeping and other low-speed (<32 kHz) operations. It can also act as the reference for the phase-locked loop (PLL) mode of the internal main oscillator (IMO). The PLL uses the 32.768-kHz input to generate a more accurate 24-MHz clock signal. This is used for operations that require an accurate high-speed clock such as dual-tone multi-frequency (DTMF) signal generation, serial communications, and RTC. Optimal performance from the ECO for each of these functions requires different external components and control register settings.

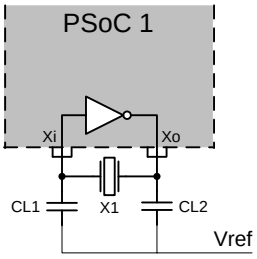
## 2 External Crystal Oscillator Theory

The goal of clock generation is to synthesize a signal that oscillates at a known frequency, duty cycle, and amplitude. The clock signal is used to clock data into and out of digital systems, and to govern the sampling of analog systems.

The ECO type used by PSoC 1 devices is a Pierce oscillator, which is shown in Figure 1. The dotted box indicates that the inverting amplifier is internal to the PSoC 1; all other parts are external. The crystal input and output (XtalIn and XtalOut) pins are also labeled in the diagram.

In this scheme, there are three discrete components, the crystal (X1) and two load capacitors (CL1, CL2). These components form a pi-network, which means that one component is in series and the other two are connected to a reference signal on either side.

Figure 1. Pierce Oscillator Topology

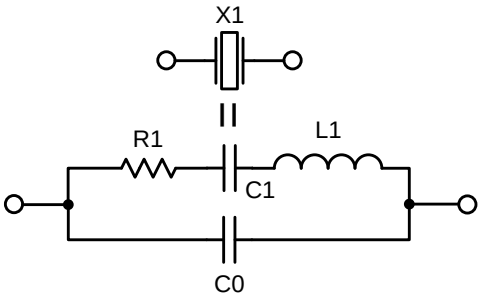



The crystal or resonator (X1) in the pi-network is physically designed to oscillate at the desired frequency. The capacitors (CL1, CL2) in the pi-network “load” the crystal or resonator to ensure proper oscillation. These capacitors are referenced to VRef, which is $V_{CC}$ in PSoC 1 devices. The inverting amplifier amplifies the output of the pi-network and drives the input terminal with the logical inverse. The pi-network provides 180 degrees of phase shift from input to output at the resonant frequency. When combined with the inverting amplifier, 360 degrees of phase shift exist in the circuit, leading to oscillations at the desired frequency.

## 2.1 Crystal Equivalent Circuit

Crystals can be modeled as a combination of passive components. The equivalent model is shown in Figure 2. C1 is known as the “motional capacitance” and L1 is known as the “motional inductance”. C0 is known as the “shunt capacitance”. Some or all of these characteristics are specified by the crystal manufacturer.

Figure 2. Crystal Equivalent Circuit




# 3 Crystal Selection

Proper selection of crystal is important because along with external components, internal parameters of the crystal also play a crucial role in the signal generation of a particular frequency. This section discusses the important crystal parameters to be checked before using in a design.

- Frequency of oscillation – A crystal is designed to operate at a particular frequency. The manufacturer’s datasheet specifies the nominal frequency at which crystal unit will oscillate. However, to successfully be able to oscillate at the required frequency, sustaining circuit must be carefully designed.
- Load capacitance – This is the capacitance that must appear across the two terminals of the crystal. Any deviation in the capacitance across the terminals will cause a change in the oscillating frequency.
- Drive Level – Drive level is used to express the amount of power dissipated across the crystal unit. It is expressed in microwatts (µW). A high drive level may cause problems such as instability and aging. On the other hand, a high drive level helps in better phase noise performance. Thus, a compromise must be established between the performance and aging.
- Motional Resistance – Motional resistance or ESR (effective series resistance) of the crystal is responsible for the losses in the network. The amplifier and external biasing network must compensate for the losses across the ESR to maintain a successful oscillation. This compensating of crystal ESR via an amplifier and biasing network is referred to as negative resistance of the oscillator circuit.

These parameters are discussed in more detail in the following sections.

## 3.1 Frequency of Oscillation

The crystal oscillator works at two resonant frequencies, series resonant (fs) formed by the series resonance of $L_1$ and $C_1$ and parallel resonant (fp) formed by the parallel resonance of $L_1$ and series combination of $C_1$ and $C_0$. Parallel resonant frequency is also known as the fundamental frequency of operation.

Figure 3. Resonator Reactance versus Frequency

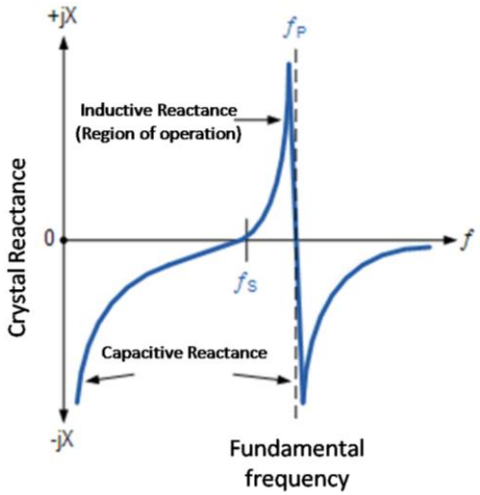



Figure 3 shows the reactance versus frequency curve of the crystal. At frequencies far from fp, the crystal appears capacitive; between fs and fp, it appears inductive. The region between fs and fp is the usual operating range of the crystal.

### 3.1.1 Crystal Selection

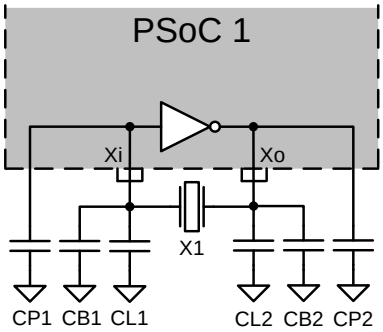
The crystals recommended for use with PSoC 1 are parallel resonant, 32.768-kHz crystals.

## 3.2 Load Capacitor Selection

Crystal oscillator circuits must be loaded with the proper capacitance to oscillate at the correct frequency. The pi-network capacitors should be chosen based on the chosen crystal's rated load capacitance, as well as stray capacitances from the PCB and PSoC pins. The total load capacitance applied is equal to the series combination of the two parallel combinations of the capacitances on each of the crystal input and output pins.

When designing the ECO circuit, choose the value of two discrete load capacitors, as shown in Figure 1. The circuit actually contains additional parasitic capacitances, as shown in Figure 4. Shown are the discrete load capacitors (CL1 and CL2), along with PSoC pin capacitances (CP1 and CP2) and PCB trace capacitances (CB1 and CB2). These parasitic capacitances will affect the applied load capacitance and should be considered when a high degree of accuracy is required. The total combination of these capacitances should equal the rated load capacitance of the crystal X1, which should be 12.5 pF.

Figure 4. ECO Circuit with Parasitic Capacitances



Capacitor values may be determined using the formula shown in General Load Capacitance Criterion Equation 1. In this equation, CL1 and CL2 are the ECO load capacitors shown in Figure 1, CP1 and CP2 are the PSoC pin capacitances, and CB1 and CB2 are the printed circuit board trace capacitances. When solving this equation, CL, CB1, CB2, CP1, and CP2 will be known, leaving one equation for two unknowns, CL1 and CL2. For this reason, another equation must be generated, describing the ratio between CL1 and CL2. This ratio will differ between applications. The advantages and disadvantages of different ratios are described in this application note.

General Load Capacitance Criterion Equation 1

$$CL = \frac{1}{\frac{1}{CL1 + CB1 + CP1} + \frac{1}{CL2 + CB2 + CP2}}$$

The package capacitances for the various PSoC MCU packages are found in the Clocking section of the Device Family Datasheets. The PCB trace capacitance depends on PCB geometry. For example, a layout with 0.20-inch long and 0.010-inch wide traces over a ground plane on a 4-layer 0.062-inch thick PCB, has a board parasitic capacitance of 0.3 pF on each pin. This value may be measured experimentally using an LCR meter, or determined theoretically using the physical characteristics of the PCB.

### 3.2.1 Balanced Load Capacitors

The most straightforward arrangement of discrete load capacitors is to have the same value for both, a situation that is described as “balanced”. Balanced configuration provides an advantage of lower jitter when compared to the unbalanced load capacitor configuration (discussed in next section). If CL1 and CL2 are assumed to be equal, the pin and trace capacitances are assumed to be the same on input and output, and CL is assumed to be 12.5 pF, this relationship may be simplified, as shown in the following equation.

Balanced Load Capacitor Criterion Equation 2

$$CL1 = CL2 = 25pF - CP - CB$$

Table 1 shows standard balanced capacitor values that are used with the various PSoC microcontroller packages, assuming 0.3 pF board capacitance as in the previous example.

Table 1. Example ECO Capacitor Values for Balanced Feedback Configuration

| Package | Typical CP | CL1 | CL2 |
|---|---|---|---|
| 8-Pin DIP | 0.9 pF | 22 pF | 22 pF |
| 20-Pin DIP | 2.0 pF | 22 pF | 22 pF |
| 20-Pin SOIC | 1.0 pF | 22 pF | 22 pF |
| 20-Pin SSOP | 0.5 pF | 22 pF | 22 pF |
| 28-Pin DIP | 2.0 pF | 22 pF | 22 pF |
| 28-Pin SOIC | 1.0 pF | 22 pF | 22 pF |
| 28-Pin SSOP | 0.5 pF | 22 pF | 22 pF |
| 44-Pin TQFP | 0.5 pF | 22 pF | 22 pF |
| 48-Pin DIP | 5.0 pF | 20 pF | 20 pF |
| 48-Pin SSOP | 0.6 pF | 22 pF | 22 pF |

### 3.2.2 Unbalanced Load Capacitors

By using an unbalanced pair of discrete load capacitors, the amplitude of the input signal can be increased, reducing the ECO’s noise susceptibility. In this case, the series capacitance of the load capacitors still needs to be the crystal’s rated load capacitance of 12.5 pF. An unbalanced pair of capacitors causes an increase in the operating current of the circuit, and is only recommended for ECO designs with noise susceptibility problems.

For the unbalanced configuration, the total capacitance on the XtalOut pin (Port 1, Pin 0) should be near 100 pF. The following equation shows the total capacitance at the XtalOut pin ($C_{P1[0]}$) if a 100-pF discrete load capacitor is used.

XtalOut (Port 1, Pin 0) Capacitance Equation 3

$$C_{P1[0]} = 100pF + CB2 + CP2$$

The load capacitor at the XtalIn pin is chosen so that the series capacitance at the crystal pins totals 12.5 pF. Equation 4 shows the calculation for the ideal value of CL1 (the capacitor on P1[1]: XtalIn).

XtalIn (Port 1, Pin 1) Capacitance Equation 4

$$CL1 = \frac{(CL2 + CP2 + CB2) * 12.5\,pF}{(CL2 + CP2 + CB2) - 12.5\,pF} - CP1 - CB1$$

Table 2 lists typical package capacitances and standard capacitor values for CL1 and CL2 closest to the calculated ideal values for various packages. Board parasitic capacitance is assumed to be 0.3 pF for these calculations.

Table 2. ECO Capacitor Values for Unbalanced Feedback

| Package | Typical CP | CL1 | CL2 |
|---|---|---|---|
| 8-Pin DIP | 0.9 pF | 12 pF | 100 pF |
| 20-Pin DIP | 2.0 pF | 12 pF | 100 pF |
| 20-Pin SOIC | 1.0 pF | 12 pF | 100 pF |
| 20-Pin SSOP | 0.5 pF | 12 pF | 100 pF |
| 28-Pin DIP | 2.0 pF | 12 pF | 100 pF |
| 28-Pin SOIC | 1.0 pF | 12 pF | 100 pF |
| 28-Pin SSOP | 0.5 pF | 12 pF | 100 pF |
| 44-Pin TQFP | 0.5 pF | 12 pF | 100 pF |
| 48-Pin DIP | 5.0 pF | 9 pF | 100 pF |
| 48-Pin SSOP | 0.6 pF | 12 pF | 100 pF |

### 3.2.3 Load Capacitance Trim Sensitivity

Variation of actual load capacitance has a tendency to “pull” the resonant frequency of the ECO. This effect is known as “trim sensitivity”. This effect can be both positive and negative. On the positive side, the designer may tune the resonant frequency of an oscillator by slightly modifying capacitor values. However, on the negative side, capacitance variation across parts and across temperature can cause the generated frequency to differ from the desired value.

Trim sensitivity is measured in PPM of added clock error per pF of variation in total actual load capacitance. It can be determined using crystal parameters described in the Crystal Equivalent Circuit section. Trim sensitivity is a function of the crystal’s rated load capacitance (CL), shunt capacitance (C0), and motional capacitance (C1). The function is shown in the following equation.

ECO Trim Sensitivity Equation 5

$$Trim\ Sensitivity = S = \frac{C1 * 1{,}000{,}000}{2 * (C0 + CL)^2}$$

**Note** This formula is a linearization of what is actually a second order function. For more details, ask your crystal vendor.

For example, here we calculate trim sensitivity for an Abracon AB38T-32.768-kHz crystal. This 32.768-kHz crystal has a typical C1 of 0.0035 pF, typical C0 of 1.6 pF, and CL of 12.5 pF. Thus, the trim sensitivity is determined as shown in Equation 6. This calculation shows that for 1 pF in error in the actual load capacitance, the frequency will shift by 8.8 PPM or 0.29 Hz.

**Note** 1 pF in discrete capacitor error will cause less than 1 pF of total actual load capacitance error, because of the relationship shown in Equation 1.

Trim Sensitivity Calculation Example Equation 6

$$S = \frac{C1 * 1{,}000{,}000}{2 * (C0 + CL)^2} = \frac{0.0035 * 1{,}000{,}000}{2 * (1.6 + 12.5)^2} = 8.8\,\frac{PPM}{pF}$$

Trim sensitivity implies requirements for load capacitor values and temperature coefficients. It should be considered along with resonator frequency accuracy and system performance requirements to determine what load capacitors to use.

## 3.3 Drive Level

Drive level of a crystal indicates the amount of current flowing through its electrodes. It is expressed as the power dissipation across the crystal unit. Drive level has a strong effect on the frequency of oscillation, and can adversely affect the crystal performance as well. It is important to understand the advantages and limitations of having higher drive levels.

Advantages:

- Higher drive level helps in meeting the startup requirement of higher gain to compensate for the drop across the ESR of the crystal.
- Higher drive level provides better phase-noise performance (deviation in phase causes the frequency to change in order to maintain the 2-nπ phase condition).

Limitations:

- As the drive level increases, the amplitude of crystal oscillations also increase. It may cause excessive aging and in some cases the crystal may also break.
- Increasing drive level can also cause shift in the oscillation frequency because of the temperature increase due to the dissipation across the crystal.

To ensure that drive level of the crystal unit is kept in control, the PSoC 1 device family has an inbuilt Automatic Gain Control (AGC), which reduces the gain of the amplifier if it crosses a particular threshold. The AGC is always active and cannot be turned off. This helps to reduce the drive level and has better stability.

Drive level can be expressed by Equation 7.

Drive Level Equation 7

$$DL = I_{L_RMS}{}^{2} * R_1$$

where, $I_{L_RMS}$ is the RMS current through the crystal, and $R_1$ is the motional resistance of the crystal.

Drive level is measured using a current probe, which measures the current entering or exiting the resonator. The ECO should be tested in the intended final configuration, without any resistance used for testing –R. The current measurement should be taken after ECO startup is complete and the automatic gain control has had time to stabilize at the steady state drive level of the circuit. The RMS current measurement may be used in conjunction with Equation 7 to calculate drive level.

### 3.3.1 Crystal Selection

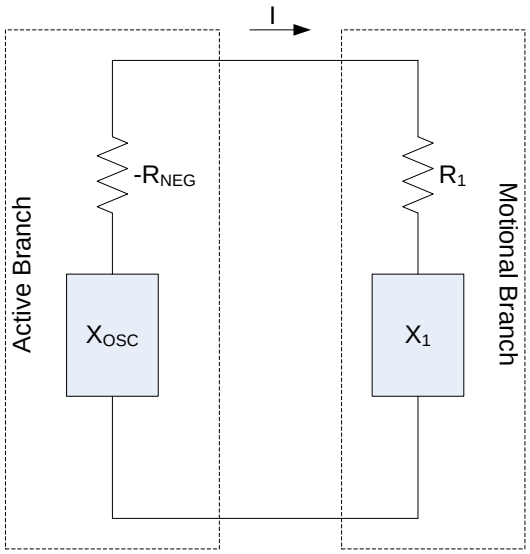
Drive level of a crystal is mentioned in the manufacturer's datasheet. It is strongly recommended to not drive the crystal at a rating higher than the one mentioned in the crystal's datasheet.

## 3.4 Negative Resistance

Negative resistance is not a physical parameter but is named after the change in the I-V characteristics of a tunnel diode when operated in a particular region. In tunnel diode, with the increase in voltage, it exhibits a dip in current. This effect is known as negative resistance.

Negative resistance model is widely used for the analysis of oscillation circuitry because it accurately determines whether the system provides sufficient gain to build the oscillation. Figure 5 explains the negative resistance model.

Figure 5. Negative Resistance Model




Similar to the Barkhausen criteria or oscillation, the negative resistance model is given by Equation 8 and Equation 9.

$$-R_{NEG} = R1 \quad \text{Equation 8}$$

$$-X_{OSC} = X1 \quad \text{Equation 9}$$

In the steady state, the oscillator must provide sufficient negative resistance to compensate for the losses in the resistance of the crystal. The reactive component of the crystal must cancel the reactive component of the oscillator; this determines the frequency of oscillation. Equation 8 and Equation 9 are valid only for the steady state. However when the oscillations build up, negative resistance must be higher to ensure that more energy is delivered to the crystal motional arm to build up the oscillations.

Table 3 provides some generic guidelines for the –R to ESR ratio for startup.

Table 3. –R to ESR Ratio Guidelines

| Ratio (–R : ESR) | Mode of Operation |
|---|---|
| Ratio < 2:1 | Unsafe |
| 2:1 < Ratio < 3:1 | Suitable |
| 3:1 < Ratio < 5:1 | Safe |
| 5:1 < Ratio | Very safe |

Negative resistance of an oscillator circuit is governed by a number of factors, which include amplifier gain or drive level, external components, and shunt capacitance of the crystal.

### 3.4.1 Crystal Selection

Lower the shunt capacitance, higher will be the –R and lower the ESR, lower will be the requirement for –R

It is important to consider that SMD crystals have lower shunt capacitance, but their ESR is generally on a higher side (typ. 60 kΩ). If higher ESR crystals are used with PSoC 1 or device is intended to operate at less than 0 $^0$C, then it is recommended to increase the amplitude level (see Increasing the Drive Current section) to meet the –R to ESR ratio requirement.

# 4 PCB Layout Tips

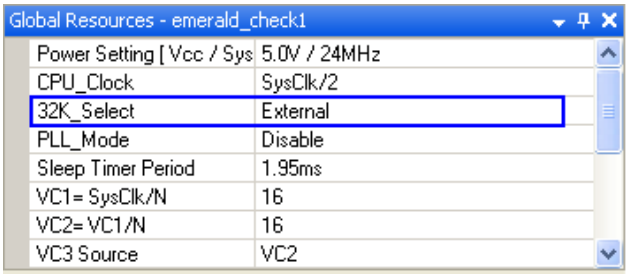
The ECO operates as a low-power oscillator. To accomplish this, it is designed as low-amplitude, high-impedance analog circuit. It must be treated as such during component placement and circuit layout. Layout is critical to performance. Also, note that the presence of contaminants on the PCB impacts the performance of the oscillator.

The crystal and the load capacitors must be placed close to the pins of the microcontroller. They must be placed over a common-ground plane. High-speed digital signals (signals with short rise and fall times) should not be routed close to the ECO circuit. Also, digital signals should not be routed near the ECO external components. When possible, the pins immediately adjacent to the ECO pins must be left unconnected or they must be used for lower-speed signals. Low-speed signals may be driven with the “strong slow” setting.

# 5 ECO Implementation Basics

The PSoC microcontroller’s 32.768-kHz clock uses either the low-accuracy ILO or the higher accuracy ECO for reference. The 32-kHz Select bit of the Oscillator Control Register 0 (OSC_CR0) determines which source is used. The easiest way to set this bit is to set the *32K_Select* parameter in the Global Resources table of PSoC Designer™ to ‘External’ (highlighted in Figure 6).

Figure 6. *32K_Select* Setting for ECO Operation

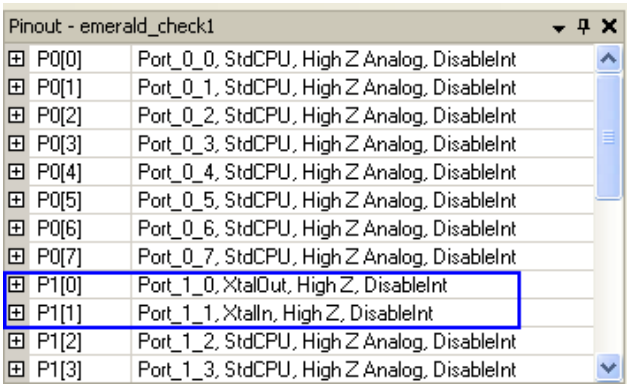



The ECO drive circuitry must be electrically connected to a 32,768 Hz crystal through the XtalIn and XtalOut pins of the PSoC MCU.

**Note** 32,768 Hz is used because it allows the power of two integer division to a 1-Hz clock signal, because 2^15 = 32,768.

The XtalIn and XtalOut pins must have their drive modes set to HI-Z (highlighted in Figure 7) for the ECO to work properly. If the pin drive modes are not set to HI-Z, the drive circuitry will free-run at an incorrect frequency.

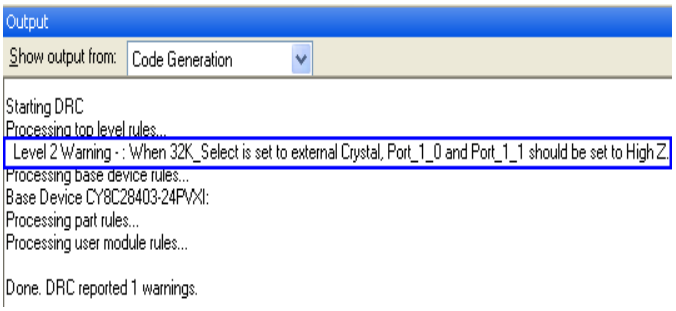
Figure 7. XtalIn and XtalOut Pin Drive Settings for ECO Operation




The pins are automatically set to High Z if the “Select” parameters are set to XtalOut and XtalIn in the Pin Description table. The correct configuration of P1[0] and P1[1] is confirmed by running the Design Rule Checker in PSoC Designer (Tools > Design Rule Checker); you can see the results in the output window.

Figure 8 shows the output of the DRC when P1[0] and P1[1] are not correctly configured.

Figure 8. Design Rule Checker Output



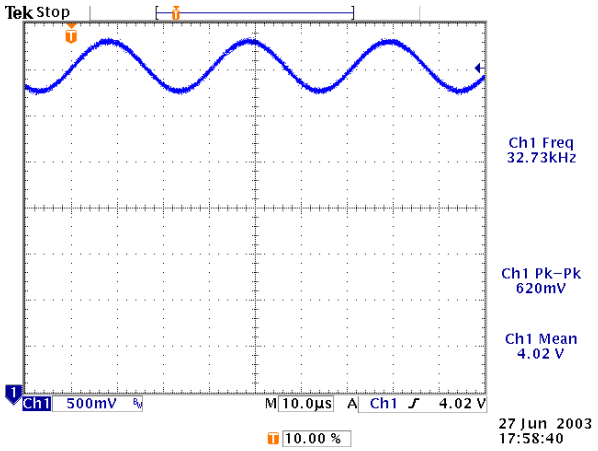

# 6 ECO and PLL Mode

The IMO maybe be sourced with a signal from the PLL, using the ECO as a reference. This results in an IMO with a more accurate frequency and less voltage and temperature drift than can be accomplished with the IMO alone. Normally, the IMO operates with 2.5 percent accuracy over the full temperature and voltage range. When using the PLL, the IMO can be as accurate as the ECO itself, less than ±100 PPM of error, depending on the ECO configuration.

When configuring the IMO in PLL mode, a number of changes must be made. The design must use an unbalanced load capacitor configuration and include a local bypass capacitor. Also, an increased drive current must be used. The unbalanced feedback configuration has already been discussed, and increased drive current is described later in this document.

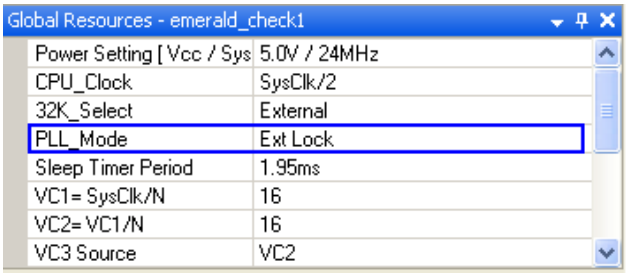
The use of unbalanced load capacitors boosts the amplitude of the signal at XtalIn (P1[1]). See Figure 9 for a waveform at P1[1], captured with the aid of the circuit shown in Figure 15. See Observing ECO Operation to understand how to view ECO signal on an oscilloscope. The amplitude at XtalIn is now approximately 600 $mV_{p-p}$.

Figure 9. ECO Waveform with Unbalanced Capacitors




The PLL Mode bit of the *OSC_CR0* register enables the PLL mode of the IMO. The easiest way to set this bit is to set the *PLL_Mode* parameter to '*Ext Lock'* in the Global Resources window of PSoC Designer (highlighted in Figure 10).

Figure 10. *PLL_Mode* Setting for IMO Operation



In general, a PLL requires a low jitter reference to remain stable. Because the PSoC microcontroller's ECO uses a low-amplitude signal, the presence of noise causes the apparent position of the clock edges to jitter from cycle to cycle. The base frequency of the ECO remains accurate but the jitter can cause the IMO to be unstable. The purpose of the unbalanced load capacitors is to reduce the jitter caused by noise on the 32-kHz waveform.

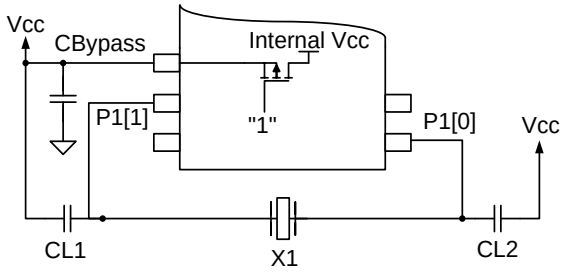
When using the PLL mode of the IMO, PCB layout is the most critical factor in minimizing jitter on the ECO. By carefully designing the PCB, the amount of noise present in the ECO circuit can be minimized. See PCB Layout Tips for more details.

Other required modifications to increase the stability of the ECO are providing a local $V_{CC}$ bypass and increasing the ECO drive current.

## 6.1 Providing a Local Bypass when Using PLL Lock Mode

When using the PLL configuration of the IMO, additional filtering of the $V_{CC}$ power is required. For this purpose, a local $V_{CC}$ bypass capacitor is added near the XtalIn pin (Port 1, Pin 3). To do this, configure the pin's drive mode to Resistive Pull Down and write a '1' to the Data Register (*PRT1DR*). Connect the pin to $V_{CC}$ and connect a 0.1-µF capacitor between the pin and $V_{SS}$ (see Figure 11). This connects the internal power bus to $V_{CC}$ through the pin pull-up FET; providing a local low-impedance connection to $V_{CC}$.

Figure 11. PLL Mode Electrical Configuration




A drive mode of Pull Down is recommended so that if a '0' is accidentally written to P1[3] it results in a 5.6-kΩ resistance between $V_{DD}$ and $V_{SS}$, instead of a short between $V_{DD}$ and $V_{SS}$.

# 7 Startup Requirements

Both the ECO and IMO experience periods of instability when they are first started. Therefore, the ECO output is not used as a source for the internal 32-K clock or as a reference for the PLL mode of the IMO until it has had time to stabilize. The IMO experiences a frequency overshoot when the PLL is first enabled. As a result, the CPU clock speed must be lowered when the IMO is initially switched to PLL mode to prevent the CPU clock from exceeding its operational limit.

These circumstances require the ECO and IMO PLL mode to follow a specific startup sequence. The *boot.asm* meets this requirement if the appropriate settings (*32KSelect = External* and *PLL_Mode = Ext Lock*) are selected in the Global Resources grid in the Device Editor of PSoC Designer.

## 7.1 Starting the ECO

When the ECO is first enabled, its output is not connected to the 32-K clock tree within the PSoC microcontroller. Instead, the 32-K clock continues to be driven by the ILO until the ECO has had time to stabilize. This time is approximately 1 second. The *boot.asm* configures the sleep timer for 1 second, and then waits until the sleep timer reaches terminal count. With this mechanism, the sleep timer is used to delay connecting to the ECO until its output has stabilized.

The following steps are followed by *boot.asm* when starting the ECO:

1. The sleep timer is set to one second and cleared. The sleep timer interrupt need not be enabled.
2. ECO is enabled; set the 32-K Select bit of *OSC_CR0* to '1'.
3. When the sleep timer reaches terminal count (one second later), the ECO is automatically selected as the source for the 32-K clock tree and can now be used as a clock source for event timing.

4. The *boot.asm* holds off entry to *main()* until all the clocks are stable. This means that calling main is delayed by about one second when using the ECO.

**Note** The sleep timer uses the ILO, which is –50% to +100% accurate, so this “1 second” sleep time can vary from 0.5 to 2 seconds.

If some tasks must be accomplished before the one-second period expires, add the initialization code to *boot.asm* (remember that the edits must be made to the template file: *boot.tpl*). You can also choose to write your own clock initialization code as long as the rules in this section are upheld.

*The boot.asm* contains a flag, *WAIT_FOR_32K*, which forces the program to wait for the clocks to stabilize before calling main. If you change this flag to ‘0’, *boot.asm* starts the ECO, but does not wait for it to stabilize and does not set the *PLL_Lock* bit. If this is done, you must provide code elsewhere that enables the ECO through the same process as the original startup sequence. However, for this to work, the *PLL_Mode* must be disabled in the Global Resources window so that it is not enabled by *boot.asm* before the ECO is enabled by the user’s code. If the PLL is used in the application, it must also be enabled by the user’s code after the ECO is enabled correctly.

## 7.2 Starting the IMO PLL Mode

The IMO cannot be phase-locked to the ECO until the ECO is stable—this takes approximately one second. Also, the CPU clock frequency cannot exceed 3 MHz when the PLL mode is first set. Both of these restrictions are in place to prevent the CPU clock frequency from temporarily exceeding 12 MHz for 3 V operation (or 24 MHz for 5 V operation). As mentioned earlier, *boot.asm* holds off entry to *main()* until all of the clocks are stable when using the ECO. When the PLL mode is used, the following delays are also present in *boot.asm*:

- A one-second delay is added whenever the ECO is enabled to wait for the ECO to become stable.
- Following the one-second delay, the CPU speed is set to 3 MHz, PLL is enabled, and a delay of 16 ms is introduced. After the 16-ms delay, the CPU speed is set to 12 MHz and the rest of the initialization code continues.

**Note** The CPU speed is set to the desired speed as configured in the Global Resources at the end of *boot.asm*.

## 7.3 Recommendations

Under normal conditions, the recommended setting for the External Crystal Oscillator Trim (ECO_TR) register is 7Ah. The ECO_TR register sets the adjustment for the 32.768-kHz ECO. This is the lowest amplitude setting with output buffer B bias control enabled. For higher gain settings, amplitude of the ECO_TR register can be changed. Make sure that the drive level is below the maximum limit specified in the crystal datasheet. See Table 4 for reference.

**Notes**

1. Setting the *32K_Select* Global Resource to ‘Internal’ and *PLL_Mode* Global Resource to ‘External Lock’ is an invalid configuration. There is no connection from the ILO to the IMO (see the Clock Tree diagram in the CY8C27x43 Family Datasheet). The requirement is evaluated by the Design Rule Checker provided in PSoC Designer (Tools > Design Rule Checker).
2. The XtalIn and XtalOut pins are also used for in-system serial programming (ISSP). The pins can be configured to function for both operations in the same design. For more information on in-system programming, see PSoC 1 – ISSP Programming Specifications.
3. For the CY8C27x43 Rev. A chip, bits 2 and 3 of CPU_SCR1 register cannot be used.

# 8 Using the ECO in Sleep

The 32-kHz ECO may be used as a clock source for digital blocks during sleep, but care must be taken to desynchronize the clock inputs from the IMO, because it will be turned off. If any clock is synchronized to a static signal, all clock edges will be masked.

Digital block input clock resynchronization is controlled using the AUXCLOCK[7:6] bits in the DxBxxOU registers. A value of 0x00 in the AUXCLOCK bits will select the unsynchronized clock input. Clock synchronization is described in depth in the PSoC 1 TRM sections “Input Data Synchronization” for both analog and digital blocks.

# 9 Sharing of ISSP and ECO Pins

## 9.1 Dual Purpose ECO Pins

In PSoC 1 family, Xin and Xout pins of ECO are on P1.1 and P1.0, which are also the dedicated pins for ISSP programming. This dual functionality of ISSP/ECO pins does not add any constraint on ISSP lines because the capacitor required on Xin and Xout lines are in the order of 10 to 100 pf, which does not impose any problem for ISSP programming protocol. But capacitance added to Xin and Xout because of ISSP traces and connector may cause a shift in crystal's oscillating frequency (discussed in section Load Capacitor Selection). For precise frequency generation following guidelines should be followed:

- Keep ISSP traces as small as possible to minimize the additional capacitance.
- Compute the value of C1 and C2 by considering the capacitance of ISSP traces into account.

OR

- For production boards, add a 0-Ω resistor in between ISSP header and pins. Remove 0-Ω resistors to remove the capacitance during operation.

# 10 32-kHz ECO Using the CY3210 Kit

The CY3210-EVAL1 kit has traces and footprints to allow the installation of a 32.768-kHz crystal and pi-network capacitors. The crystal network is connected to pins P1[0] and P1[1]. These pins are also connected to a header for use as standard GPIOs. This connection is made through 0-Ω resistors R8 and R9, so that the parasitic capacitance of these traces may be removed from the oscillator. This portion of the schematic is shown in Figure 12, and a picture of the related portion of the PCB configured for ECO use is shown in Figure 13

To install and use a 32.768 kHz ECO with the CY3210-EVAL1 kit, perform the following steps:

1. Remove resistors R8 and R9.
2. Install a 0805 12 pF capacitor as C10.
3. Install a 0805 100 pF capacitor as C9.
4. Install a can-style 32.768-kHz, 12.5-pF crystal as Y1 (such as Abracon AB38T – 32.768KHz).

Figure 12. ECO Portion of CY3210-EVAL1 Kit Schematic

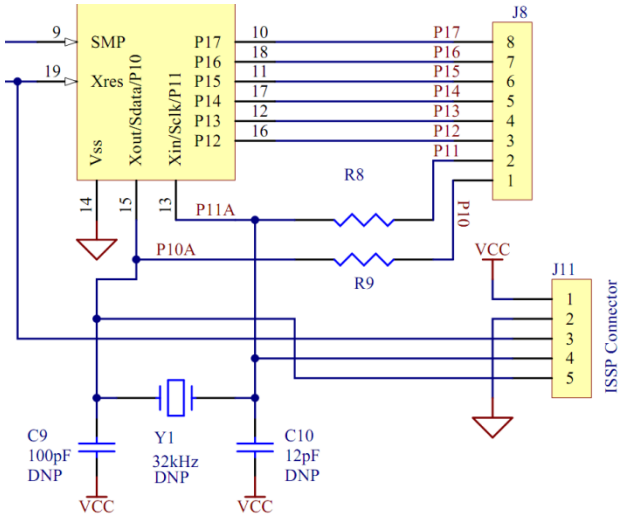
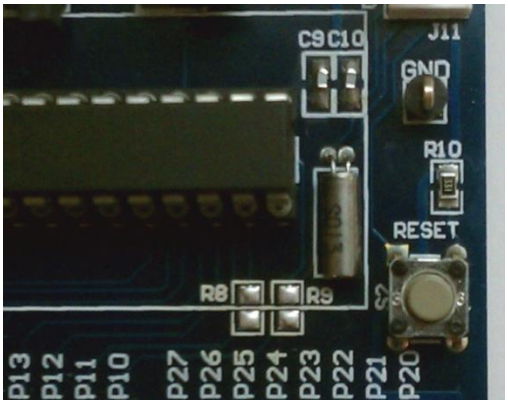


Figure 13. CY3210-EVAL1 ECO Components




**Note** The label for component Y1 is beneath the body of the crystal can, and is thus not visible in this picture.

# Appendix A. Appendix A

## A.1 Observing ECO Operation

Because the ECO circuit is high-impedance and low-amplitude, a standard oscilloscope probe cannot be used to view the signal. The load of a standard oscilloscope probe distorts the waveform and impacts performance. One option is to use a unity gain opamp to buffer the signal so that it is viewed with an oscilloscope. Figure 14 shows the ECO waveform at the XtalIn pin (P1[1]) captured with the aid of the circuit shown in Figure 9.

Figure 14. ECO Waveform

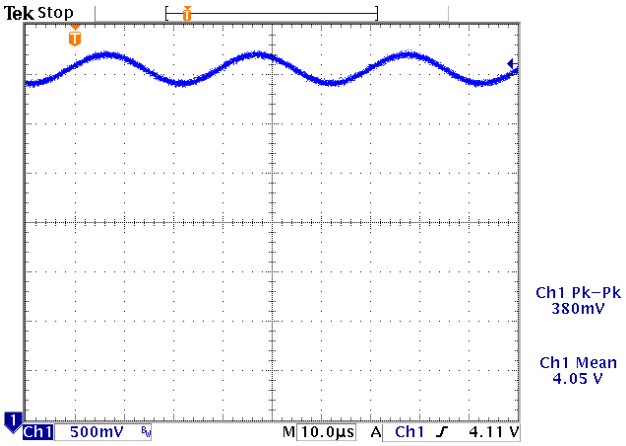
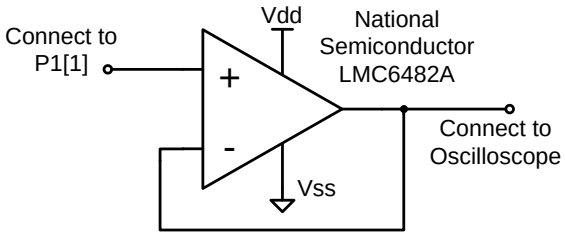


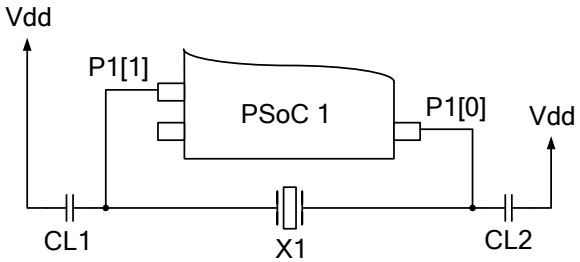

Figure 15. Unity Gain Buffer




The analog signal has a DC offset of approximately 4 V and peak-to-peak amplitude of approximately 400 mV.

Figure 16 shows the external circuit that is used for the ECO. Note that the load capacitors are connected to $V_{CC}$. This is the optimal configuration because the ECO driver is referenced to $V_{CC}$. If the capacitors are incorrectly referenced to $V_{SS}$, the ECO will operate at the correct frequency, but is slightly more susceptible to power supply noise.

Figure 16. ECO Electrical Connections




For standard ECO operation (when not used as a reference for the IMO PLL), the configurations described in the Device Family Datasheets should be used. This includes a 32.768 kHz, 12.5 pF, 1 µW or less watch crystal, and temperature stable (NPO) ceramic capacitors.

## A.2 Increasing the Drive Current

To increase the drive current of the ECO network, update the ECO_TR register. This register controls the amplitude level of the amplifier used available inside PSoC 1.

## A.3 ECO_TR Register

When using the ECO, there are a few components that must be set by the trim register for satisfactory operation. They include Comparator or Output Buffer A and B and the Amplitude Control. Output Buffer A is an improvement from an older design while Output Buffer B is a new addition. The *ECO_TR* register is write only, which means that bitwise logical operations cannot be used to change specific bits. This register is shown in Table 4.

## A.4 Bit Description

### A.4.1 Output Buffer 'A' Bias Control [0]

This bit is used to set the startup (unregulated) bias current of the crystal oscillator output buffer A. In normal operation, this bias level exceeds what is required for stable oscillation and as a result, the amplitude of the signal on the crystal increases. The signal then approaches the level set by the amplitude control bits and the bias level is reduced by the amplitude control loop until stable oscillation is maintained at the defined level.

0 = minimum bias

1 = maximum bias

### A.4.2 Output Buffer B Bias Control [1]

This bit is used to set the bias reference level for the crystal oscillator output buffer B. Because output buffer B uses a fixed bias level, this operates at a fixed level independent of the oscillator amplitude settings.

0 = minimum bias

1 = maximum bias

### A.4.3 Amplitude Control [3:2]

These bits are used to control the amplitude of the crystal oscillator. The settings are:

01 = Highest

00 = Medium High

11 = Medium Low

10 = Lowest

### A.4.4 Output Buffer B Enable [4]

This bit is used to enable the extra output buffer B. This buffer operates at a fixed bias level, which is controlled by the bias control bit 1. That also means that bit 1 elicits no effect if bit 4 does not enable buffer B.

0 = enables operation only for buffer A

1 = enables operation for buffer B and bias generator

### A.4.5 Output Buffer B Hysteresis Enable [5]

This bit provides approximately 30 mV of hysteresis to the output buffer. However, the value of bit 5 elicits no effect if output buffer B is not enabled by bit 4.

0 = Disables Hysteresis

1 = Enables Hysteresis

### A.4.6 Reserved [6:7]

These bits are unused by this operation, but are assigned to functions elsewhere in the IC.

Table 4. ECO_TR Register Description

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | Output Buffer B Hysteresis | Output Buffer B Enable | MSB | LSB | Output Buffer B Bias Control | Output Buffer A Bias Control |
| Reserved | | Output Buffer B Control | | Amplitude Control | | Bias Control | |

Table 5. Amplitude Setting

| Amplitude Setting | ECO_TR |
|---|---|
| Highest | 0x77 |
| Medium High | 0x73 |
| Medium Low | 0x7F |
| Lowest | 0x7B |

## Document History

Document Title: AN2027 - PSoC® 1 - 32.768-kHz External Crystal Oscillator

Document Number: 001-40399

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 1532004 | EDT | 11/13/2007 | Submitted to ECN system |
| *A | 2551067 | MAXK/JVY | 08/11/2008 | Rolled in changes from multiple revisions that were never formalized. Updated for more recent devices and programming software. |
| *B | 3157509 | MAXK | 01/30/2011 | Added CY3210 kit details. Added operation in sleep. Updated title and abstract. |
| *C | 3266143 | MAXK | 05/25/2011 | Added CY8C28xxx, CY8C2xx45 to Associated Part Family. |
| *D | 3478292 | MAXK | 12/29/2011 | Added information on ECO theory, equivalent model, and trim sensitivity<br>Updated load capacitor nomenclature to CL1 and CL2<br>Improved diagram clarity<br>Updated template |
| *E | 3714751 | PMAD | 08/16/2012x | Added selection information for drive level and negative resistance.<br>Added advantages of balanced capacitor configuration.<br>Added Appendix A and Sharing of ISSP and ECO Pins.<br>Updated template. |
| *F | 4422007 | PMAD | 06/27/2014 | Updated template. Sunset Review. |
| *G | 5709392 | AESATP12 | 04/26/2017 | Updated logo and copyright. |
| *H | 6318910 | DIMA | 09/24/2018 | Updated copyright |

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