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AN202487

Differences Among FM0+, FM3, and FM4 32-Bit Microcontrollers

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Associated Part Family: All FM0+, FM3, and FM4 Parts

Related Application Notes: See Related Resources

AN20248 highlights the similarities and differences in peripheral support among Cypress's FM family portfolios. For each peripheral, it provides comprehensive information on any differences, including features and register usage.

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1 Introduction

The FM0+, FM3, and FM4 MCU families share peripherals. The way that each peripheral is implemented can vary slightly among those families. This application note offers a high-level overview of which features are available in the different families and device types. Each device type within a device series represents a variation in the silicon design, which sometimes has an effect on peripheral implementation. For a complete overview of FM MCU device types, refer to the Peripheral Manual's appendix.

All peripherals are not present on all devices. In general this application note does *not* list the availability of peripherals for specific devices. Availability is only discussed when necessary. Always refer to the device's datasheet for the feature set.

For very complex differences, for example the multifunction timer (MFT), the text will refer you to the Peripheral Manual for more information.

See Related Resources on page 22 for links to peripheral manuals, datasheets, and other resources.

See Appendix A: Device Type and Product Series on page 23 to relate a particular device type to a product series.

This application note is intended for software engineers who do not use preconfigured high-level software libraries, but want to program an FMx MCU at the register and bit level to get highly optimized code. You may prefer to develop software using the Cypress Peripheral Driver Library (PDL), which accommodates the differences noted in this app note. The PDL provides a high-level API to configure, initialize, and use a peripheral driver. The PDL provides numerous code examples that demonstrate how to use the peripherals. You can also use the PDL source code as a guide.

Table 1 shows the symbols used in the tables in this document.

Table 1. Table Symbols

Symbol	Meaning	Description
	Not included	Feature not available
√	Included	Feature available
A/B/…	Implementation type	Device type dependent on peripheral version
0, 1, …	Numbered item	Number of feature of peripheral

2 Features

2.1 FM0+ Device Type Differences

Table 2 gives an overview of the resource differences among the FM0+ device types.

Table 2. FM0+ Device Type Differences

Feature	Device Type		
	1	2	3
Maximum Clock Speed (MHz)	40[1]		
PLL Settings	Refer to FM0+ Family Peripheral Manual.		
Interrupt Table Type[1]	1-A/1-B	2-A/2-B	3
HS-CR Frequency Trimming BT0-3	√	√	√
HS-CR Frequency Trimming Bits	10	10	10
HS-CR Clock Divider Bits	3	3	3
HS-CR Temperature Trimming	√	√	√
Fast GPIO	√	√	√
Indication of Low Power and Power-On Reset	√	√	√
Low-Voltage Detection Type[1]	A	B	C
Unique ID	√	√	√
DMA Channels	4		
DSTC Support		√	√
MTB (Micro Trace Buffer)	√	√	√
RTC Clock Control/ Count Block Type[1]	A	B	A
DTTI Analog Noise Canceler		√	
PPG-IGBT	√	√	
Quadrature Position/Revolution Counter	√	√	
MFS I^2S Controller		√	√
USB Support		√	√
Smart Card Interface		√	√
Dedicated USB PLL		√	
VBAT Domain		√	
LCD Controller[1]	A	B	

[1] Refer to FM0+ Family Peripheral Manual for details.

2.2 FM3 Device Type Differences

FM3 devices are organized into four performance groups:

- Basic (B)
- High Performance (HP)
- Low Power (LP)
- Ultra Low Leakage (UL)

Table 3 gives an overview of the resource differences among the FM3 device types.

Table 3. FM3 Device Type Differences

Feature	Device Type												
	0	1	2	3	4	5	6	7	8	9	10	11	12
FM3 Group	HP	B	HP	UL	HP	B	LP	UL	LP	B	B	B	B
Maximum Clock Speed (MHz)	80	40	144	20	144	40	40	20	40	72	72	40	60
PLL Settings	Refer to the FM3 Family Peripheral Manual.												
Dual-Operation Flash							√		√	√			√
Work Flash					√	√							
ECC Flash		√	√		√	√							
Flash Accelerator (Main Flash)			√		√								
Interrupt Table Type[2]	A	A	A	C	A/B	A/B	A/B	C	A/B	A/B	A/B	A/B	A/B
HS-CR Frequency Trimming ICU3	√	√	√	√	√	√		√		√			√
HS-CR Frequency Trimming BT0							√		√	√	√	√	√
HS-CR Frequency Trimming Bits	10	8	8	10	8	8	10	10	10	10	10	10	10
HS-CR Clock Divider Bits	2	2	2	3	2	2	2	3	2	2	2	2	2
HS-CR Temperature Trimming									√	√	√	√	√
Indication of Low Power and Power-On Reset				√				√					
Low-Voltage Detection Type[2]	A	A	A	B	A	A	C	B	C	C	C	C	C
Unique ID							√		√	√	√	√	√
ETM (Embedded Trace)	√	√	√		√		√[1]	√[1]	√				√
DMA Redirect to USB Ch. 1			√										
Watch Counter Prescaler Type[2]	A	A	A	A	A	A	A	A	A	A	A	A	B
RTC Clock Control Block Type[2]	B	B	B	A	A	A	B	B	B	B	B	B	B
Base Timer I/O Selection Type[2]	A	A	B	A	A	A	A	A	A	A	A	A	A
PPG-IGBT								√		√		√	√
Quadrature Decode Position Rotation Count Register				√	√	√	√	√	√	√	√	√	√
ADC Type[2]	A	A	A	B	A	A	B	B	B	B	B	B	B

[1] Depends on package size.
[2] Refer to the FM3 Family Peripheral Manual for details.

2.3 FM4 Device Type Differences

Table 4 gives an overview of the resource differences among the FM4 device types.

Table 4. Resources in Different FM4 Device Types

Feature	Device Type					
	1	2	3	4	5	6
Maximum Clock Speed (MHz)	160	160	200	160	180	160
PLL Settings	Refer to the FM4 Family Peripheral Manual.					
Dual-Operation Flash			√			
Work Flash	√	√				√
ECC Flash	√	√	√	√	√	√
Flash Accelerator (Main Flash)	√	√	√	√	√	√
Clock Gear Function			√	√	√	√
Interrupt Table Type[1]	A	A	A	B	A	A
Low-Voltage Detection Type[1]	A	A	B	B	B	A
Unique ID	√	√	√	√	√	√
ETM (Embedded Trace)	√	√	√	√	√	√
HTM (AHB Trace Macro Cell)			√			
RTC Clock Control Block Type[1]	A	A	B	B	C	A
RTC Clock Counter Block Type[1]	A	A	B	B	C	A
Analog Noise Canceller			√	√	√	√
Base Timer I/O Selection I/O Mode 9					√	√
External Bus Interface: SRAM, NOR, NAND Flash, SDRAM	√		√	√	√	√
Graphic Display Engine				√		
HyperBus Interface				√		
SD Card Interface	√		√	√		
Smart Card Interface					√	
High-Speed Quad SPI			√	√		
I^2S Controller			√	√		
CAN FD			√	√		
VBAT Domain Type[1]	A	A	B	B		A

[1] Refer to the FM4 Family Peripheral Manual for details.

3 System

3.1 Device Type Mode Pin Settings

FM devices can be set to different system modes with the mode pins. Table 5 shows the mode pin settings.

Table 5. Device Type Mode Pin Settings

Mode Pins		Operation Mode
MD1[1]	MD0	
0	0	User Mode (Flash Startup)
0	1	Programming Mode
1	0	FM3 device type 0: not allowed
		FM3 device types other than 0, and FM4: User Mode (Flash Startup)
1	1	Not allowed

[i] Pin MD1 is not available for FM0+ type 1.

3.2 Bus Systems Availability

FM devices have several bus systems on-chip. Table 6 lists the availability of these buses.

Table 6. Bus System

Device Type	AHB	APB0	APB1	APB2	DMAC	DSTC	AXI
FM0+, Type 1	√	√	√		√		
FM0+, Types 2, 3	√	√	√			√	
FM3, all	√	√	√	√	√		
FM4, all	√	√	√	√	√	√	Type 4

3.3 Flash Accelerator Availability

To speed up execution time, several FM devices provide a flash accelerator. Table 7 shows the availability.

Table 7. Flash Accelerator Availability

Device Type	Flash Accelerator
FM0+, all	
FM3, Types 2, 4	√
FM3, other types	
FM4, all	√

Note that for all FM0+, for MCU frequencies greater than 20 MHz, one wait cycle must be inserted.

3.4 Memory Architecture

3.4.1 Flash Memory Types

FM devices have different flash memories such as single, dual-operation, and additional work flash. Table 8 lists the differences.

Atomic access to RAM and peripheral bits are done by the bit band alias region. These areas are the same for all FM devices.

The start address of the peripheral I/O area is `0x4000 0000` for all FM family devices. The addresses of the peripherals themselves differ among the FM family devices.

Table 8. Flash Memory Types

FM Family	Main Flash	Work Flash	Dual Operation Flash	SRAM	SRAM Bit Band Alias Area Address	Peripheral Bit Band Alias Area Address
FM0+	√		Type 2	1 RAM area	0x2200 0000	0x4200 0000
FM3	√	Types 4, 5	Types 6, 8, 9, 12	2 RAM areas		
FM4	√	Types 1, 2	Type 3	3 RAM areas		

3.4.2 Peripheral Bus Distribution

The FM0+, FM3, and FM4 devices have up to three peripheral bus systems (APBn). The distribution of the peripherals among these buses differs. Refer to the peripheral manuals for details.

FM0+ and FM4 devices provide one peripheral bus that can be clocked by the base clock (HCLK) with a 1:1 divider setting even at high frequencies (> 80 MHz). This means that the speed of the connected peripherals, such as the MFT and the ADC, is doubled. For a detailed description, refer to the corresponding datasheet.

For FM3 devices with a base clock lower than 72 MHz, 1:1 clocking may also be allowed, but no real speed increment is generated. Refer to the corresponding datasheet for the possibility.

Figure 1 shows an example of AC characteristics from a device datasheet.

Figure 1. Example Electrical Characteristics

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	$V_{CC} \geq 2.7V$	8	48	MHz	When the crystal oscillator is connected
			$V_{CC} < 2.7V$	8	20		
			-	8	48	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	20.83	125	ns	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock*1 frequency	F_{CM}	-	-	-	40.8	MHz	Master clock
	F_{CC}	-	-	-	40.8	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	40.8	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	40.8	MHz	APB1 bus clock*2
Internal operating clock*1 cycle time	t_{CYCCM}	-	-	24.5	-	ns	Master clock
	t_{CYCC}	-	-	24.5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.5	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	24.5	-	ns	APB1 bus clock*2

4 Peripherals with No Differences

Table 9 lists peripherals that are the same across all FM families and series. Some peripherals are not available on all devices.

Table 9. Peripherals with No Differences

Peripheral	Availability
Cyclic Redundancy Check (CRC)	All
Clock Supervisor (CSV)*	All
Consumer Electronics Control (CEC)	All
Dual Timer (DT)	All
Graphic Display Controller (GDC)	FM4 Type 4
Hyperbus Interface (HPBI)	FM4 Type 4
Programmable CRC (PRGCRC)	FM4 Types 3 and 4
SD Card Interface (SD)	FM4 Types 1,3, and 4
Smart Card Interface	FM4
Unique ID (UID)	FM0+, FM3 Types 6, and 8 to 12, FM4;

5 Analog-to-Digital Converter (ADC)

Table 10 lists the differences in conversion times and support for range comparison for the ADC. If range comparison is supported you can test whether the ADC result is inside or outside of a range within a continuous detection time.

Table 10. ADC Conversion Times

Device Type	Minimum Conversion Time	Range Comparison
FM0+, Type 1	0.8 µs @ 5 V	√
FM0+, Type 2	1.0 µs @ 2.7-3.6 V	√
FM0+, Type 3	2.0 µs @ 2.7-3.6 V	√
FM3[1], all	0.8 µs @ 5 V	
FM4, all	0.5 µs @ 5 V	√

[1]For FM3 ADC types, refer to Table 3.

5.1 Connection to MFT

Refer to the Multifunction Timer (MFT) section for details on different connections to the timer in the FM0+, FM3, and FM4 devices.

6 Base Timer (BT) and I/O Selection (BTIOSEL)

The functionality of the base timer is the same in all FM0+, FM3, and FM4 devices. I/O selection varies.

Base Timer I/O Selection (FM3)

FM3 device type 2 – I/O Select Function (B) – cannot use the TIOA9 input pin of BT channel 8 and 9 in Timer Full Mode (I/O mode 1) to trigger the timer.

The I/O Select Function (A) of all other FM3 device types does not have this restriction.

Base Timer I/O Selection (FM0+/FM4)

FM0+ and FM4 devices use the same I/O Select Function (A) as FM3 without the restriction of I/O Select Function (B).

FM4 device types 5 and 6 provide I/O Mode 9.

7 Controller Area Network (CAN)

All FM3 and FM4 devices which support a CAN interface use the same Bosch C_CAN.

FM0+ does not support CAN.

CAN Input Clock (FM4)

The input clock for device types 1 and 2 is 16 MHz maximum. For other types, the maximum frequency is 40 MHz.

CAN with Flexible Data Rate (CAN FD)

(Non-ISO) CAN FD is available only on FM4 devices. Refer to the datasheet for availability. It is based on the M_CAN macro.

8 Clock (CLK)

Table 11 provides the similarities and differences for CLK features. Refer to the peripheral manual for details.

Table 11. CLK features

Device Type	Peripheral Clocks	CR Division	Clock & Reset Gating
FM0+, all	2 (PCLK0, PCLK1)	3 bits with dedicated dividers	√
FM3, Types 3, 7	3 (PCLK0, PCLK1, PCLK2)	3 bits with dedicated dividers	
FM3, other types	3 (PCLK0, PCLK1, PCLK2)	2 bits with dedicated dividers	
FM4, all	3 (PCLK0, PCLK1, PCLK2)	3 bits with dedicated dividers	√

Clock Gating (FM0+/FM4)

FM0+ and FM4 devices provide clock and reset gating of peripherals. Note that some registers may not exist depending on package size and peripheral features.

Clock Gear Control (FM4)

FM4 device types 3 to 6 support the Clock Gear Control function. Therefore, the additional register PLLG_CTL is available.

Peripheral Clock (FM4)

One peripheral bus can be clocked at the HCLK speed. Refer to the Multifunction Timer (MFT) section on page 17 for details.

Sub Clock (FM0+/FM4)

The sub clock oscillator in FM4 devices is located in the VBAT domain. FM0+ device type 2 also provides the VBAT domain sub clock.

9 CR Trimming (HS-CR)

These tables detail the implementation of CR trimming. Table 12 lists the number of frequency trimming bits. Table 13 lists the number of temperature trimming bits. The usable timer for trimming the High-Speed-CR clock depends on the FM3 device type, as specified in Table 14.

Table 12. HS-CR Frequency Trimming Bits

Device Type	Trimming Register Bits
FM0+, all	10
FM3, Types 0, 3, 6 to 12	10
FM3, Types 1, 2, 4, 5	8
FM4, all	10

Table 13. HS-CR Temperature Trimming Bits

Device Type	Trimming Register Bits
FM0+, Types 1, 2	5
FM0+, Type 3	7
FM3, Types 0 to 7	
FM3, Types 8 to 12	5
FM4, all	5

Table 14. FM3 Timers for Trimming HS-CR

Device Type	MFT – ICU Ch. 3	Base Timer Ch. 0
FM3, Types 0 to 5, 7	√	
FM3, Types 6, 8		√
FM3, Types 9 to 12	√	√

10 Digital-to-Analog Converter (DAC)

Table 15 shows the DAC resolutions. Refer to the peripheral manuals for DAC availability.

Table 15. DAC Resolution

FM Family	Resolution
FM0+	10 bits
FM3	10 bits
FM4	10 bits/12 bits selectable

11 Debug Interface

Table 16 shows the differences in the debug capability among the FM families. Note that some restrictions may apply depending on package size. Refer to the device datasheet for details.

Table 16. Debug Interface

FM Family	JTAG	SWD	Trace
FM0+		√	√
FM3	√	√	√
FM4	√	√	√

Trace Clock (FM3/FM4)

FM3 and FM4 devices support the extended trace module (ETM). Table 17 shows available settings. FM0+ devices provide only the Micro Trace Buffer (MTB).

Table 17. FM3 Trace Clock Dividers

Device Type	TPIU Clock Divider Settings
FM3, Types 0, 1	1/1 and 1/2
FM3, Types Other than 0, 1	1/1, 1/2, 1/3, …, 1/8
FM4, all	1/1, 1/2, 1/3, …, 1/8

Trace Pins (FM4)

FM4 types 3 and 5 allow you to use up to 16 trace data pins.

AHB Trace Macro Cell (FM4)

FM4 type 3 devices provide an AMDA AHB Trace Macro Cell (HTM).

12 Direct Memory Access (DMA)

Table 18 shows the differences in DMA and DSTC support.

Table 18. DMA and DSTC Support

Device Type	DMA/DSTC support	DMA Channels
FM0+, Type 1	DMA	4
FM0+, Types 2 and 3	DSTC	
FM3, all	DMA	8
FM4, all	Both	8

Priority (FM3)

For FM3 device type 0, the DMA may block the CPU in burst transfer mode. For other FM3 device types, the bus priority uses the round-robin method.

Additional Selector (FM3)

FM3 type 2 products have an additional selector (DQESEL register) to switch certain vectors of dedicated peripherals to USB Channel 2 endpoints.

Descriptor System Data Transfer Controller (DSTC) (FM4)

In FM4 devices, peripherals that have an interrupt capability can be switched to DMA or DSTC.

13 Descriptor System Data Transfer Controller (DSTC)

See the Direct Memory Access (DMA) section for details.

14 External Interrupts (EXINT)

The functionality of the external interrupts is the same for all FM devices.

FM0+/FM3

External interrupt channels 0 to 7 share one interrupt vector. External interrupt channels 8 and greater share one interrupt vector.

FM4

External interrupt channels 0 to 15 each have their own interrupt vector. External interrupt channels 16 to 19, 20 to 23, 24 to 27, and 28 to 31 each have one interrupt vector.

External Interrupt Vector Level Register 2 (ELVR2) (FM4)

In addition to the detection of low and high levels, falling and rising edges, FM4 device types 5 and 6 allow the detection of both edges with the ELVR2.

15 External Bus Interface (EXTIF)

Table 19 shows the differences in EXTIF support.

Table 19. EXTIF Support

FM Family	EXTIF Support	NAND Support	SDRAM Support
FM0+			
FM3[1]	√	See datasheet	
FM4[1]	√	√	√

[1] Devices with a pin count less than 100 do not support an external bus interface.

FM3 Device Type 0

FM3 device type 0 does not support the following:

- Separate and multiplex mode
- Signal timing and polarity based on ALE, CS, and so forth
- Clock output
- RDY functionality

16 Flash Memory (FLASH)

Memory organization (single flash, dual-operation flash, work flash) differs in every family. Refer to the corresponding flash programming manual for details. Table 8 gives an overview.

17 General-Purpose I/O (GPIO) Ports

Some FM families support fast GPIO. With additional FPOERn registers, FM0+ and FM4 devices can switch GPIO output and/or input from the peripheral bus to the core bus, allowing faster output signals to be generated. See Table 20.

Table 20. Fast GPIO support

FM Family	Fast GPIO Output	Fast GPIO Input
FM0+	√	√
FM3		
FM4	√	

Note that some registers may not exist, depending on package size and peripheral features.

Handling of Serial Chip Select (SCS) Bit (FM4)

The handling of the SCSn bits of EPFR16 and EPFR23 differs among device types. Refer to the Multifunction Serial (MFS) Interface section.

18 High-Speed Quad SPI (HSSPI)

FM4 device types 3 and 4 support HSSPI. In type 4, the HSSPI is connected to the AXI bus instead of the AHB bus, allowing slightly higher throughput.

19 Inter-IC Sound (I^2S)

The devices listed in Table 21support I^2S. No other FM devices support I^2S.

Table 21. I^2S Support and Modes

Device Type	Modes
FM0+ Type 2	Master only
FM0+ Type 3	Master only
FM4 Type 3	Master and slave
FM4 Type 4	Master and slave
FM4 Type 5	Master only

FM4 types 3 and 4 have a dedicated I^2S PLL. Refer to the peripheral manual for details.

20 Interrupts (IRQ)

FM4 interrupt sources are typically distributed to specific interrupt vectors.

FM0+ and FM3 devices may have more possible interrupt sources than there are interrupt vectors. The same vector may be used to support multiple interrupts. Interrupt relocation and interrupt source selection features assist in handling interrupt muxing.

Interrupt Relocation

Some FM devices support interrupt relocation. This allows you to choose between two alternate interrupt vector tables, in effect an A/B switch. Which vector table you use is controlled by the value of the **IRQCMODE** register. Consult the Peripheral Manual for your FM device series for details on mapping of interrupts to vectors in each vector table. Table 22 lists the differences among device types

Table 22. Interrupt Relocation Support

Device Type	Relocation	IRQCMODE	Uses
FM0+, Type 1	Available	0	Interrupts Type 1-A
		1	Interrupts Type 1-B
FM0+, Type 2	Available	0	Interrupts Type 2-A
		1	Interrupts Type 2-B
FM0+, Type 3	Not available	Not available	Interrupts Type 3
FM3, Types 0 to 2	Not available	Not available	Interrupts Type A
FM3, Types 3, 7	Not available	Not available	Interrupts Type C
FM3, Types 4 to 6, 8 to 12	Available	0	Interrupts Type A
		1	Interrupts Type B
FM4, Types 1 to 3, 5, 6	Not available	Not available	Interrupts Type A
FM4, Type 4	Not available	Not available	Interrupts Type B

Interrupt Source Selection

FM0+ types 1 and 2, and FM4 devices have eight selectable interrupt vectors, which can each be connected to a peripheral interrupt source. The advantage of these interrupts is that a specific flag bit of an interrupt monitoring register can be selected even if the corresponding interrupt cause of this bit shares its vector with others. For FM0+, these selectable interrupts are available only in Interrupts Type 1-B and Type 2-B (IRQCMODE = 1). Table 23 lists available sources.

Table 23. FM0+/FM4 Interrupts Available for Source Selection

FM0+ Peripheral (Interrupt Type 1-B)	FM0+ Peripheral (Interrupt Type 2-B)	FM4 Peripheral
EXTINT 0 – 11	EXTINT 0 – 11	EXTINT 0 – 7
BT 0 – 7	BT 0 – 7	QPRC0/1
MFS Rx 0 – 3	MFS Rx 0 – 3	MFT0/1/2
MFT0/1/2	MFT0	DTIF
DMA0 – 4		PPG0/2/4/8/10/12/16/18/20
MFS Rx 8 – 15		BT0 – 7
MFS Tx 8 – 15		DT

Interrupt Monitoring (Batch Read Registers)

If a peripheral shares an interrupt vector with other peripherals, you can use the interrupt monitoring registers to retrieve the interrupt cause.

Although FM4 devices have individual vectors, the monitoring registers can be used to retrieve the cause by reading the dedicated monitoring register instead of reading the interrupt flags of the peripheral registers.

The contents of the Batch Read Registers differ among FM0+, FM3, and FM4 devices.

FM3 Device Type 2

FM3 device type 2 products have an additional DQESEL register, which allows replacing several interrupts with the endpoint interrupts of the second USB (USB1) peripheral. Refer to the peripheral manual for details.

21 Liquid Crystal Display (LCD)

The LCD peripheral is identical for all FM3 devices.

The LCD peripheral for FM0+ type 1 and type 2 differs. Refer to the peripheral manual for details.

FM0+ Type 3, and the FM4 family do not provide an LCD peripheral.

22 Low-Power Modes (LPM)

Table 24 shows the differences in low power modes among FM devices.

Table 24. Low Power Modes

Device Type	Standby				Deep Standby			
	SLEEP	TIMER	RTC	STOP	DS-RTC	DS-RTC (RAM retention)	DS-STOP	DS-STOP (RAM retention)
FM0+, Type 1	√	√	√	√				
FM0+, Types 2,3	√	√	√	√	√	√	√	√
FM3, Types 0,1,2,4	√	√		√				
FM3, Types 3, 7	√	√	√	√			√	
FM3, Types 5,6,8,9,12	√	√	√	√	√	√	√	√
FM3, Types 10,11	√	√	√	√				
FM4, all	√	√	√	√	√	√	√	√

FM3 Control Registers

FM3 device types 6 and 8 to 12 support a sub oscillator voltage control register.

FM3 device types 6 and 7 to 12 support a sub clock control register.

FM4 Modes

The real-time clock and backup registers are part of the VBAT domain (except type 5).

FM4 type 3 devices provide an additional bit for HDMI-CEC/remote control for sub clock connection.

23 Low-Voltage Detection (LVD)

Voltage range differs among device types. Depending on the current consumption groups and voltage range, the thresholds for generating an interrupt and reset are different. Refer to the peripheral manual for the device in use for details.

For FM4 types 1 and 2, the handling of the Deep Standby Return Enable Register (WIER) differs from that of the other types. Refer to the peripheral manual for details.

Reset Detection Bit

FM4 devices provide this bit.

FM0+ devices do not provide this bit.

FM3 device types 3 and 7 provide an additional LVDH bit, which indicates a low-voltage detection reset, in addition to the power-on reset bit.

24 Multifunction Serial (MFS) Interface

Table 25 lists the main differences among the FM families.

Table 25. MFS Features and Differences

Feature	FM0+	FM3	FM4
Automatic Chip Select Signal (SCS[1])	Up to 4[4]		Up to 4[4]
Serial Timer	√		√
TX- and RX-FIFO Depth	Up to 128[4]	8	64
SDA/SCL Read and Write in I2C Mode[2]		Type >5	√
I2C Noise Filter[3]		√	√
Maximum Data Width per Single Transfer	16 Bits	9 Bits	16 Bits

[1] SCS pin is not available for every MFS and depends on package size. Refer to the corresponding datasheet for availability.

[2] This functionality is intended to read the bus state and to force the bus to certain values for I2C bus error corrections.

[3] Register structure differs between FM3 and FM4.

[4] Refer to the corresponding datasheet.

Chip Select Pin Independent Operation (FM4)

Device types 1 and 2 differ in functionality. Refer to the corresponding peripheral manual.

Chip Select Pin Round-Robin Operation (FM4)

Device types 1 and 2 do not support this functionality.

Serial Chip Select Format/Timing and Transfer Byte Register (FM4)

Depending on the number of available chip select pins, the number of SCSFRn, SCSTRn, and TBYTEn registers differs.

In general, FM4 device types 1 and 2 provide only one chip select signal.

Extended Serial Control Register (ESCR) (FM0+/FM4)

FM4 device types 1 and 2 do not provide the Serial Chip Select Format Enable Bit (CSFE).

This bit is provided in all FM0+ devices.

Serial Chip Select Control/Status Register (SCSCR) (FM0+/FM4)

FM4 device types 1 and 2 do not provide the SST1, SST0, SED0/1, SCD0/1, CSEN1/2/3 bits.

These bits are provided in all FM0+ devices.

25 Multifunction Timer (MFT)

Because of the complexity of the MFT, this section gives an overview of the MFT differences. It does not explain the differences in the features in detail. It is strongly recommended that you refer to the corresponding peripheral manual for the exact details of the differences.

FM0+ and FM4 devices use almost the same MFT macro, but this macro differs from that of FM3. It is possible to set the FM0+/FM4 MFT to FM3 compatibility mode. However, because some register names and functionalities are different, the compatibility mode is functional only and not one-to-one software compatible.

The main difference in the two kinds of MFT is the ADC Compare Unit (ADCMP). For FM0+/FM4 devices, ADCMP provides a much more complex connection and more trigger possibilities for the ADC units. It needs dedicated configuration settings.

Note that The MFT is not available on FM0+ Type 3.

Table 26 lists the differences among the FM families.

Table 26. MFT Features and Differences

Feature	FM0+	FM3	FM4
Free Running Timer Control Register B (TCSB)		√	
Free Running Timer Control Register C (TCSC)	Types 1, 2		√
Free Running Timer Counter Mode Operation with Offset (TCSD)	Type 2		Types 3–6
Free Running Timer Simultaneous Start Control Register (TCAL)	Types 1, 2		√
Output Compare Unit Control Register A (OCSA): Buffer function of OCCP(n) register	Types 1, 2	√	
Output Compare Unit Control Register B (OCSB): FM3 compatibility mode	Types 1, 2		√
Output Compare Unit Control Register D (OCSD): Buffer control of OCCP(n) register	Types 1, 2		√
Free Running Timer mask counter linked with OCU buffer transfer and OCU comparison condition expansion (OSCD)	Type 2		Types 3–6
Output Compare Unit Control Register E (OCSE): Several FRT state conditions compared to OCCP(n)	Types 1, 2		√
Wave Form Generator Control Register A (WFSA)	Types 1, 2	See WFG Control Register A (WFSA)	
Wave Form Generator Timer Value Register (WFTA/WFTB)	Types 1, 2		√
Wave Form Generator RT Dead Time Timer and Filter Mode Operation, PPG Dead Timer and Filter Mode Operation Expansion (WFSA.TMD)	Types 1, 2		Types 2–6
Wave Form Generator Timer Value Register (WFTM)		√	
Wave Form Generator Pulse Counter Value Register (WFTF)	Types 1, 2		√
DTTIX (Dead Time Trigger Input)Digital Noise Filter Cancel Width Expansion			Types 3–6
Analog DTIF Function	Type 2		Types 3–6
ADC Compare Unit: FM3 compatibility mode	Types 1, 2		√
ADC Compare Unit Buffer Transfer Linked with FRT Mask Counter	Type 2		Types 3–6
ADC Compare Unit Start Linked with FRT Mask Counter	Type 2		Types 3–6

For FM4 device types 3 to 5, the OCU/ADCMP/FRT selection range is expanded. For FM4 type 6, one MFT unit is independent. Refer to the peripheral manual for details.

25.1 WFG Control Register A (WFSA)

DCK Bits

FM3: Count clock cycles can be set to PCLK, 1/2, 1/4, 1/8, …, 1/64.

FM0+ types 1 and 2, and FM4 devices: Count clock cycles can be set to PCLK, 1/2, 1/4, 1/8, …, 1/128.

TMD Bits

The modes listed in Table 27 are available in all devices that support the MFT.

Table 27. MFT: WFG Mode Bits

WFG Operation Modes	FM0+/FM4	FM3
Through	√	√
RT-PPG	√	√
Timer-PPG	√	√
RT-Dead Timer	√	
RT-Dead Timer Filter	√	√
PPG-Dead Timer	√	√
PPG-Dead Timer Filter	√	

25.2 MFT Noise Canceller Control Register (NZCL)

Analog Noise Canceller (FM0+/FM4)

Clock-less noise suppression is available to FM0+ type 2 and FM4 type ≥3 devices.

DTIEA Bit (FM0+/FM4)

This bit is available to FM0+ types 1 and 2, and FM4 devices. It allows additional asynchronous (clock-less) DTTI functionality with an additional analog filter (FM4 type ≥3 devices).

NWS Bits

In FM3 devices, the noise-canceling width can be set from 4, 8, 16, 32 PCLK cycles.

In FM0+ type 2 and FM4 type 3 devices, the range is from 4, 8, 16, … to 256 PCLK cycles. Other FM0+ and FM4 devices provide a maximum of 128 PCLK cycles only.

SDTI

This bit has the same functionality in all FM family devices.

Remaining Bits

The remaining bits – DIMA, WIM10, WIM32, and WIM54 – are available only in FM0+ and FM4 devices. Refer to the peripheral manual for detailed functionality.

The DTIEB, DHOLD, and DIMB bits are available only in FM0+ type 2 and FM4 type ≥3 devices.

25.3 WFG Interrupt Control Register (WFIR)

DTIC, DTICA, DTICB, DTIF, DTIFA, DTIFB

FM3 devices provide only the DTIC and DTIF bits in the WFIR.

DTICA and DTIFA bits are available in all FM0+ and FM4 devices.

DTICB and DTIFB bits are available only in FM0+ type 2 and FM4 type ≥3 devices, but with almost the same functionality. Refer to the peripheral manual for details.

25.4 ADCMP Connecting FRT Select Register (ACFS) (FM0+/FM4)

This register connects FRT channels to the ADCMP unit. On FM0+ and FM4 devices, the ACSA register sets the FM3 compatibility mode.

Refer to the peripheral manual for details.

25.5 ADCMP Control Register A (ACSA)

In FM3 devices, the control bits connect FRT channels to a channel of the ADCMP unit.

In FM0+ types 1 and 2, and FM4 devices, the control bits enable or disable the FM3 compatibility mode.

25.6 ADCMP Control Register B (ACSB) (FM3)

This register is available only in FM3 devices. It enables and disables the ACCPn and ACCPDNn buffer functions.

25.7 ADCMP Control Register C and D (ACSC, ACSD) (FM0+/FM4)

These registers are available only in FM0+ and FM4 devices. ACSC enables and disables the buffering of the ACMP register and transfers it according to the FRT connection.

ACSD allows setting the ADCMP unit to offset mode.

The ACSC:APBM bit is available in FM0+ type 2 and FM4 type ≥3 devices.

Refer to the peripheral manual for details.

25.8 ADCMP Mask Compare Value Storage Register (ACMC) (FM0+/FM4)

This register is available in FM0+ type 2 and FM4 type ≥3 devices.

25.9 OCU Control Register D (OCSD) (FM0+/FM4)

For FM0+ type 2 and FM4 type ≥3 devices, the OCSD register has additional bits to set different buffer transfer timings. This register is not available in other device types and not in FM3 in general.

26 Programmable Pulse Generator and IGBT (PPG)

PPG implementation is identical in all FM families. Support for IGBT mode varies, as shown in Table 28.

Table 28. PPG and IGBT Support

Device Type	IGBT Mode
FM0+, Types 1, 2	√
FM3, Types 7, 8, 9,11, 12	√
FM4, all	

27 Quadrature Position and Revolution Counter (QPRC)

When available, the QPRC has the following difference among the FM devices:

QPRC Quadrature Counter Position Rotation Count Register (QPRCRR)

This 32-bit register for reading the count and revolution in a single access is available in all FM0+ and FM4 devices that support the QPRC.

For FM3 devices, this register is available only in device types greater than 2.

QPRC Input Filter

FM0+ and FM4 devices provide an input filtering of the QPRC pins (AIN, BIN, and ZIN). This filtering is selectable by the additional registers NFCTLA, NFCTLB, and NFCTLZ.

QPRC Extension Control Register (QECR)

FM4+ device types 1, 2, and 6 provide an additional PEC bit, which controls both edge counting.

28 Reset (RESET)

LVD Reset Factor (FM3)

There are differences in the reset factor registers among the FM3 device types. FM3 types 3 and 7 provide an additional LVDH bit, which indicates a low-voltage detection reset.

Power-On Reset Factor (FM3)

FM3 device types 3 and 7 provide an additional deep-standby transition reset factor indication besides power-on reset and low-voltage reset.

Reset Factors (FM0+/FM4)

FM0+ and FM4 devices do not provide low-voltage and deep-standby transition reset factors.

29 Real-Time Clock (RTC)

29.1 RTC Voltage Domain (FM0+/FM4)

In FM4 devices and FM0+ device type 2, the RTC is located in the VBAT domain and thus can be battery buffered. Setting and reading out the RTC are handled differently in other FM families. Refer to the FM0+ and FM4 peripheral manuals for details on how to handle value transition to and from the VBAT domain.

29.2 RTC Control Block Registers

Table 29 lists the differences among FM devices for the RTC control block registers.

Table 29. RTC Control Block Registers

Device Type	Control Register (WTCR)	Counter Cycle Register (WTBR)	Clock Selection Register (WTCLKS)	Time Setting Register (WTTR)
FM0+, Type 1	Two 32-bit registers[1]	√	√	One 32-bit register
FM0+, Type 2	Six 8-bit registers[2]	[4]	[4]	Three 8-bit registers[3]
FM0+, Type 3	Two 32-bit registers[1]	√	√	One 32-bit register
FM3, all	Two 32-bit registers[1]	√	√	One 32-bit register
FM4, all	Six 8-bit registers[2]	[4]	[4]	Three 8-bit registers[3]

[1] WTCR1, WTCR2

[2] WTCR10, WTCR11, WTCR12, WTRC13, WTCR20, WTCR21

[3] WTTR0, WTTR1, WTTR2 (WTTR functionality is the same on all FM devices)

[4] The RTC can be clocked only by the sub clock oscillator, so these registers are missing

WTCR10 TRANS Bit (FM4, FM0+ Type 2)

WTCR10 (comparable to lower byte of WTCR1) has an additional TRANS bit, which indicates the completion of transfer of new RTC values to and from the VBAT domain.

WTCR20 (FM4, FM0+ Type 2)

The WTCR20 register has several additional bits for controlling and transferring data to and from the VBAT domain. Refer to the Peripheral Manual for details.

29.3 RTC Clock Control Block

Each FM family supports two or more RTC Control blocks, designated A, B, and C. Block A in one family is not the same as Block A in another family. Consult the peripheral manual for the device in use for details.

Table 30 lists which device types use which control block, and some differences in registers.

Table 30. RTC Clock Control Block Type

Device Type	RTC Clock Control Block Type	Frequency Correction Value Register (WTCAL)[1]	(Frequency Correction Period Register (WTCALPRD)
FM0+, Types 1, 3	FM0+ A	One 16-bit register	√
FM0+, Type 2	FM0+ B	Two 8-bit registers	√
FM3+, Types 3, 4, 5	FM3 A	One 16-bit register	
FM3, other types	FM3 B		√
FM4, types 1, 2, 6	FM4 A	Two 8-bit registers	√
FM4, Types 3, 4	FM4 B		√
FM4, Type 5	FM4 C	One 16-bit register	√

[1] On some devices the Frequency Correction Value register, WTCAL, is split into two 8-bit registers (WTCAL0 and WTCAL1). Functionality is the same in all devices.

29.4 RTC Backup Registers

Only FM devices that have a VBAT domain provide battery-buffered backup registers.

30 Universal Serial Bus (USB)

USB is available in FM4, FM3, and FM0+ types 2 and 3 devices. Refer to the datasheet for the availability on a particular device.

USB IN Byte Count

FM3 type 0 devices do not support an odd number of bytes using IN endpoint transfer.

USB Clock

Depending on the number of USB interfaces, the USB clock registers differ among FM families (registers and bits for the second USB interface missing).

FM3 device type 0 does not provide the UPLLM register for the USB PLL clock.

Refer to the peripheral manual for the different PLL settings of FM devices.

31 Watch Counter (WC)

The watch counter is supported by all FM families. Prescaler implementation varies.

Prescaler (FM3)

FM3 device type 12 uses a prescaler setting (more dividers, LS-CR clockable) different from other device types. Refer to the peripheral manual for details.

Prescaler (FM0+/FM4)

FM0+ and FM4 devices use the same prescaler.

32 Software and Hardware Watchdog Counter

On FM3 devices, the Watchdog Counter (WDG) does not implement window watchdog mode, which detects whether the counter reload occurs within a particular time window.

As a result, FM3 devices do not include the following registers or bits:

- The SMD and TWD bits in the Software Watchdog Timer Control Register (WdogControl)
- Software Watchdog Timer Window Watchdog Mode Control Register (WdogSPMC)

33 VBAT Domain (VBAT)

The VBAT voltage domain is available only in FM4 devices (except type 5) and FM0+ type 2 devices.

It contains the sub clock oscillator, the RTC, and the backup registers. Refer to Table 4.

34 Related Resources

I Want To	Resources
Get Started with FM Programming	Explore the FM Family product pages on the Cypress website. FM4 FM3 FM0+ Purchase a starter kit. Click the Kits tab on the product page. Read a Getting Started app note. FM4 FM0+
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Learn About the Peripheral Driver Library and Code Examples	Download the PDL and read the PDL Quick Start Guide. Read the *Build and Run a PDL Project* section of the *PDL Quick Start Guide*. Explore the PDL code examples installed with the PDL
Learn About Particular Peripherals	Search for an FM Family app note. Some examples include: AN202488 – Servo Motor Speed Control AN203980 – S6E2Cx Series Over the Air Update AN99218 – Multi Function Serial Interface of FM MCU
Develop Low-level Software for FM Family	Read the *Creating a Custom Project* section of the *PDL Quick Start Guide*. Use project files and startup code from the PDL *devices* folder. Use PDL source code to see low-level programming techniques Refer to device datasheets. FM4 FM3 FM0+ Use the Peripheral Manuals as a technical reference. FM4 FM3 FM0+

A Device Type and Product Series

Refer to Table 31 to map device type to product series.

Table 31. FM Device Types and Product Series

Device Type	Current Product Series
FM0+ Portfolio	
Type 1	S6E1A
Type 2	S6E1B
Type 3	S6E1C
FM3 Portfolio	
Type 0	n/a
Type 1	MB9Ax10A
Type 2	MB9Bx10T
Type 3	MB9Ax3x
Type 4	MB9Bx10R
Type 5	MB9Ax10K
Type 6	MB9Ax4x
Type 7	MB9AxAx
Type 8	MB9Ax5x
Type 9	MB9Bx20M
Type 10	MB9Bx20J
Type 11	MB9AX20L
Type 12	MB9Bx20T
FM4 Portfolio	
Type 1	MB9BFx6xM/N/R-
Type 2	MB9BFx6xK/L
Type 3	S6E2C
Type 4	S6E2D
Type 5	S6E2G
Type 6	S6E2H

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**	5048991	MAWI	12/14/2015	New application note
*A	5556048	JETT	12/16/2016	Added information for FM0+ Type 3 Added device type to product series decoder ring Combine some tables and make presentation consistent Change some text discussions to tables for easier understanding General edits and fix typos, updated to latest template
*B	5688022	AESATMP8	04/19/2017	Updated logo and Copyright.

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