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AN2014

Basics of PSoC® 1 Programming

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Related Application Notes: For a complete list of the application notes, click here.

If you have a question, or need help with this application note, contact the author at arvi@cypress.com.

AN2014 serves as a quick start guide to PSoC® 1 Programming. It describes the Programming Interface connections, Programming modes, Programming protocol, and also the different tools and applications available for programming PSoC 1 devices. The term "programming" used in this context refers to loading the user code onto the device Flash (a.k.a Flashing) and is not to be confused with creating your program or user code. To learn how to create your custom program for PSoC® 1 using the PSoC Designer™ software, please refer to AN75320 - Getting Started with PSoC® 1.

Introduction

PSoC 1 devices can be programmed after they have been installed in a system. In-circuit programming is convenient for prototyping, manufacturing, and in-system field updates. This allows a PSoC 1 device to be programmed during prototyping, later in the manufacturing flow, or reprogrammed in the field at a later date. PSoC 1 uses in-system serial programming (ISSP) protocol for programming. ISSP is a two-wire protocol that uses a bidirectional data line (SDATA) and a clock line (SCLK) from the host to PSoC 1 to perform device Programming. There are various Programming tools that are available to program PSoC 1 using ISSP protocol. PSoC 1 supports two ISSP modes: Reset and Power Cycle programming.

PSoC 1 Programmers

Cypress offers a variety of programmers to program PSoC 1 devices. Depending on the application requirements and the stage of end product development, the appropriate programming tool can be used for programming. The programming options available are:

1. **MiniProg1 Programmer** (CY3217-MiniProg1): This is a Programmer from Cypress that you can use to program all PSoC 1 devices, except the CY25/26xxx devices.

Figure 1. CY3217 PSoC MiniProg1

2. **MiniProg3 Programmer** (CY8CKIT-002 PSoC® MiniProg3 Program and Debug Kit): This is an all-in-one programmer from Cypress for PSoC 1, PSoC 3, PSoC 4, and PSoC 5 architectures and a debug tool for PSoC 3, PSoC 4, and PSoC 5 architectures. It provides a 5-pin ISSP programming header for programming PSoC 1 devices.

Figure 2. CY8CKIT-002 PSoC® MiniProg3

3. **In-Circuit Emulation Cube** (ICE-Cube CY3215A-DK): The ICE development kit is used for Debugging PSoC 1 devices. It can also program PSoC 1 devices. The CY3215A-DK is used for prototyping and developing applications with PSoC 1 IDE (PSoC Designer™, PSoC Programmer™). This kit supports in-circuit emulation and the software interface allows access to the contents of specific memory locations.

Figure 3. CY3215A-DK In-Circuit Emulation Cube (debugger)

4. **Third party Programmers**: Besides the programmers from Cypress, there are a host of third party vendors who offer programming tools to program PSoC 1 devices in production. A list of third party Programmers that support PSoC 1 programming is available at the General PSoC® Programming page.

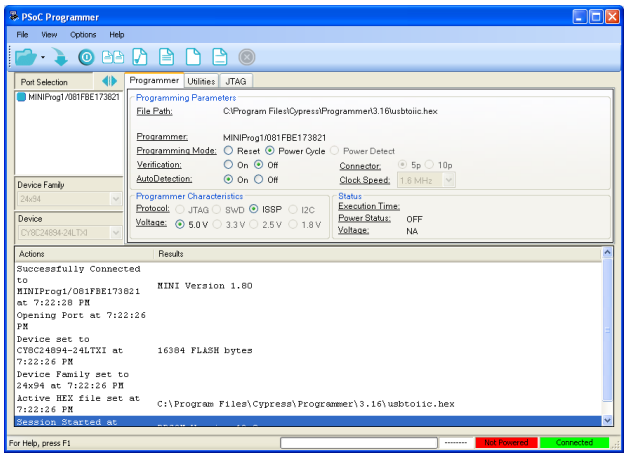
5. **Custom Host Programmers**: Customers may sometimes want to develop their own custom host programmers to program PSoC 1 devices. The host programmer could be a Microcontroller, a DSP or an FPGA. The Programming procedure described in the PSoC 1 ISSP Programming Specification series (previously known as *AN2026a*, *AN2026b*, and *AN2026c*) has to be implemented on the host to program PSoC 1. To reduce the development time required to create host programmers, a practical implementation of Programming procedure described in ISSP Programming Specification series is provided as reference code in C-language in the Host-Sourced Serial Programming (HSSP) application notes (*AN44168*, *AN59389*).

PSoC 1 Programming Software

PSoC Programmer/PSoC Designer:

PSoC Programmer is a flexible, integrated programming application for programming PSoC devices. You can use PSoC Programmer with PSoC Designer IDE to program any design onto a PSoC 1 device. PSoC Designer is the integrated design environment (IDE) that you can use to customize PSoC 1 to meet your specific application requirements. You can program PSoC 1 devices directly from the PSoC Designer IDE without having to open PSoC Programmer. Programming in PSoC Designer/PSoC Programmer can be performed only with the In-Circuit Emulation Cube (ICE-Cube CY3215-DK) or MiniProg (MiniProg1, MiniProg3) programmer.

Figure 4. PSoC Programmer Interface



Programming Modes

The programming mode determines how the programmer acquires the device for programming. There are two programming modes: Reset and Power Cycle.

Reset Programming Mode

This method uses the XRES pin of the PSoC 1 device to acquire and program the device. Reset programming mode works only if the target board is self-powered and an XRES pin is available. Reset programming mode is preferred, but if an XRES pin is not available or accessible to the programmer in application, Power Cycle programming mode must be used.

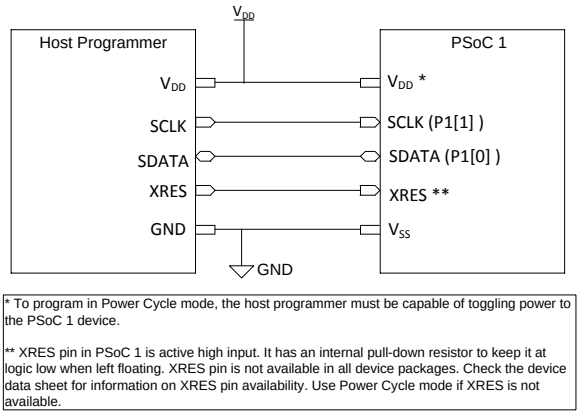
Power Cycle Programming Mode

In Power cycle Programming mode, the host programmer toggles (cycles) the power to the PSoC 1 device to acquire and program the device. This method will work for all device packages.

Host Programmer – PSoC 1 Programming Interface

Figure 5 shows the connections between Host Programmer and the Target PSoC 1 device.

Figure 5. Host Programmer - PSoC 1 Interface



* To program in Power Cycle mode, the host programmer must be capable of toggling power to the PSoC 1 device.

** XRES pin in PSoC 1 is active high input. It has an internal pull-down resistor to keep it at logic low when left floating. XRES pin is not available in all device packages. Check the device data sheet for information on XRES pin availability. Use Power Cycle mode if XRES is not available.

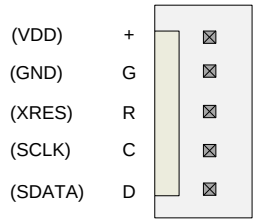
The electrical pin connections between the programmer and the target shown in the figure are listed in Table 1. This includes two signal pins, a reset pin, a power pin, and a ground pin. Leave the other pins floating. The pin naming conventions and drive strength requirements are also listed in Table 1.

Table 1. Pin Names and Drive Strengths

Pin Name	Function	Programmer HW Pin Requirements	PSoC 1 Drive mode behavior
P1[0]	SDATA – Serial Data In/Out	Drive TTL Levels, Read TTL, High Z	Strong drive (while sending data to host), Resistive pull down mode (Reading data from host, Waiting for data from host)
P1[1]	SCLK – Serial Clock	Drive TTL Levels	High Z Digital input
XRES	Reset	Drive TTL Levels. Active High	Active high Reset input with internal resistive pull-down
V_{SS}	Power Supply Ground Connection	Low Resistance Ground Connection	Ground connection
V_{DD}	Positive Power Supply Voltage	0 V, 1.8 V, 3.3 V, 5 V. 20 mA Current Capability	Supply voltage

The PSoC 1 SDATA pin drive modes vary during the programming operation. When the PSoC 1 drives the SDATA line to indicate it has started up completely or to send data back to the host, SDATA is in a strong drive configuration. When it waits for data or receives data from host, SDATA is in a resistive pull-down configuration. It is important to design the Host external pin drive mode circuitry such that a strong high to resistive low transition can be detected, and also so that the pin can be driven both high and low when it is in resistive pull-down mode. Due to internal pull-down resistor (5.6 K) on SDATA line, the presence of external pull-up resistors on the SDATA line might cause the host to miss the high to low transition on the target device due to resistive voltage divider. It is not recommended to use external pull-up resistors on the SDATA line due to this reason.

Figure 6. ISSP Header (Top View)



A five pin, 0.1” spaced header is available on the PSoC evaluation boards and can be incorporated on production boards to enable ISSP. The part number of this connector is available in the knowledge base article: Part Number for the MiniProg1 target connector, 5-pin ISSP header in MiniProg3. The CY3215A-DK development kit includes a cable with RJ45 connection on one end and an ISSP connection on the other.

See Figure 7 and Figure 8 for example connections using ICE–Cube Emulation kit, MiniProg1. Refer to the respective kit documentation for more information about the Programming tools.

Figure 7. Hardware Configuration with ICE-Cube

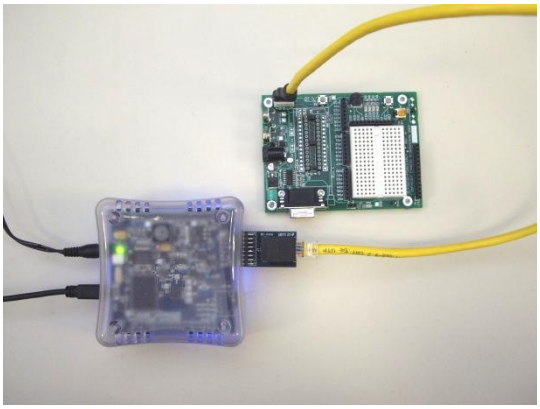
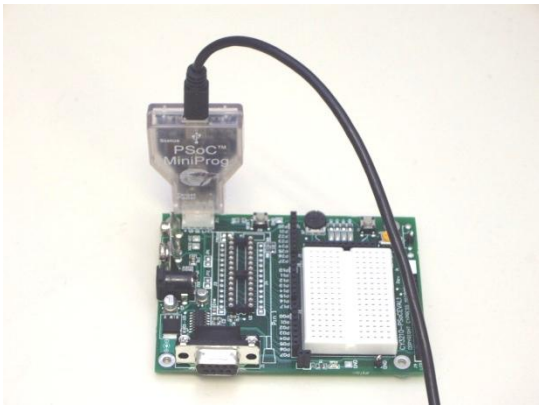


Figure 8. Hardware Configuration with MiniProg1



Using External Crystal Oscillator

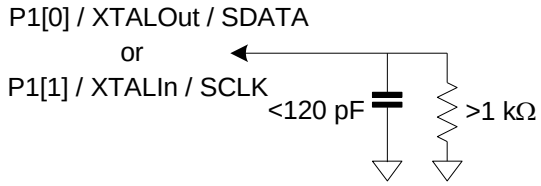
The Programming pins on PSoC 1 (SCLK (P1[1], SDATA (P1[0]) are also shared by the external 32-kHz crystal. If the external 32-kHz crystal is used, the programming connections to ports P1[0] and P1[1] need to be kept as short as possible. The total capacitance on each side of the crystal should be close to 25 pF, including the capacitance of the package leads. (See the device datasheet for pin capacitance.) Excessive trace length on these signals could adversely affect the operation of the oscillator. During programming, the 32-kHz crystal loading does not add loading to the programming pins.

Pin Loading Requirements

The SDATA and the SCLK pins each have three functions. These pins are configurable as an external 32-kHz crystal, I^2C interface pins, and as general-purpose I/O pins.

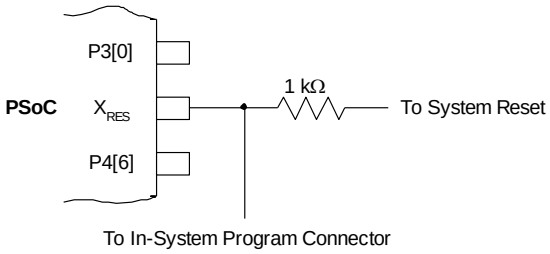
The equivalent load on these pins should not exceed 120 pF in parallel with a 1-kΩ resistor.

Figure 9. Maximum Load Data and SCLK Pins



The XRES signal is a single function pin. This signal should be connected directly to the programmer connector. Some designs may drive the XRES signal from another source, such as a system reset, to force reset at a known time. In this case, a resistor may be placed in series with the signal source and the XRES pin. The programmer is then connected on the pin side of the register. See the following figure. This will allow the programmer to overdrive the XRES pin.

Figure 10. XRES Connection



PSoC 1 ISSP Programming Specification

Detailed information about the PSoC 1 programming protocol is available in the *PSoC® 1 ISSP Programming Specifications*:

- PSoC® 1 ISSP Programming Specifications TRM #1 (AN2026a): This application note supports the following devices: CY8C21xxx / CY8C22xxx / CY8C24xxx / CY8C24xxxA / CY8C27xxx, CY8CTMG110, and CY8CTST110
- HSSP Source Code and Instructions are found in AN44168
- PSoC® 1 ISSP Programming Specifications TRM #2 (AN2026b): This application note supports the following devices: CY8C21x45, CY8C22x45, CY8C24x94, CY8C28xxx, CY8C29x66, CY8CTST120, CY8CTMA120, CY8CTMG120, and CY7C64215
- HSSP Source Code and Instructions are found in AN44168

- PSoC® 1 ISSP Programming Specifications TRM #3 (AN2026c): This application note supports the following devices: CY8C20045, CY8C20055, CY8C20xx6, CY8C20xx6A, CY8C20xx7/S, CY8CTMG2xx, CY8CTST2xx, CY7C643xx and CY7C604xx.
- HSSP Source Code and Instructions are found in AN59389

Troubleshooting

If an error occurs during programming, verify all connections. Also, verify that the electrical loading on the SDATA, SCLK, and XRES signals does not exceed the specified maximum ratings.

If using the Power Cycle programming mode with ICE CUBE or MiniProg, verify that the target board does not require more than 100 mA. For larger systems that require more than 100 mA, it may be possible to use the V_{DD} signal from the programmer to control the power supply on the target board.

The following table shows which mode is supported for the previously described configurations:

Table 2. Programming Condition

Condition	Reset	Power Cycle	Note
V_{DD} = 4.5 to 5.5 V (ICE-Cube and MiniProg)	Yes	Yes	
V_{DD} = 3.0 to 3.6 V (ICE-Cube only)	Yes	Yes	Power cycle should only be used if target is 5 V tolerant.
RST pin available	Yes	Yes	
RST pin unavailable	No	Yes	
Programmer unable to supply power to target	Yes	No	Target requires more than 100 mA or complex power system.

Summary

This application note provides a brief overview of the different tools and applications for Programming PSoC 1. It also explains the connections between the host programmer and the PSoC 1 device. The different considerations to be made while using Programming pins for other applications are also discussed. Troubleshooting techniques are also listed to aid in solving commonly encountered programming problems.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1063380	MKEA	05/11/2007	Obtain spec. # for note to be added to spec. system. Update copyright. Add source disclaimer, revision disclaimer, Samples Request Form URL, PSoC App. Note Index URL. Same title in DMS, .doc, and web. This note had no technical updates. CCD, PSoC: Please replace existing version on cypress.com.
*A	3018345	MKEA	08/30/2010	Updated PSoC Designer and Programmer references and screenshots.
*B	3187063	VVSK	03/03/2011	Changed the title, and updated the content.
*C	3363578	VVSK	09/06/2011	Removed spec from the system.
*D	3725225	ARVI	08/05/2012	Updated references, diagrams. Updated template. Removed the point on 'CY3207ISSP Programmer'.
*E	3837753	ARVI	12/11/2012	Updated Document Title to read "Basics of PSoC® 1 Programming - AN2014". Updated Abstract. Updated PSoC 1 Programmers. Updated PSoC 1 Programming Software (No change in contents, updated Figure 4 only). Updated PSoC 1 ISSP Programming .
*F	4015243	ARVI	05/30/2013	Updated device references in document. Updated Abstract.

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