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AN13666

PSoC® 1 Driving Analog Buffer Output to the Rail

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Associated Project: No

Associated Part Family: CY8C24xxx, CY8C27xxx, CY8C28xxx, CY8C29xxx

Software Version: PSoC® Designer™ 5.1

AN13666 provides a model for the PSoC® 1 analog column buffers' output drive and outlines a simple external circuit to extend the drive capability all the way to the rail.

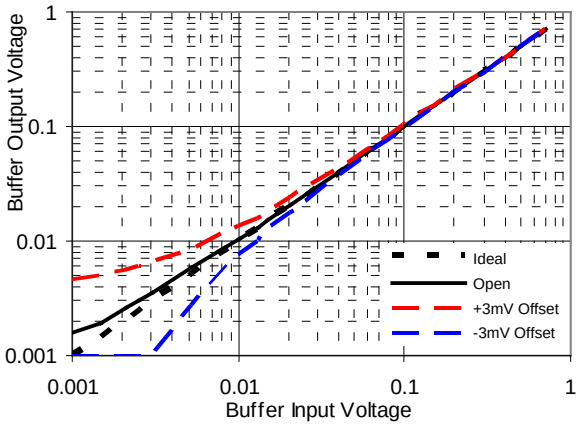
Introduction

The PSoC analog output buffer is designed to drive current to analog ground (AGND) usually set near mid-supply. The buffer is capable of driving 1.3 V into a 32 ohm load. With a 5.0 V supply and AGND set to Vdd/2, this gives 1.2 volts of headroom, enough to absorb any output impedance in the buffer. If your application requires driving closer to V_{SS} or V_{DD}, there may be a problem. In this application note, we examine the limits and a simple external circuit to compensate for the problem.

Buffer Nominal Performance

The buffer output is designed to drive near, but not to, the supply rails. A simple test project with a RefMux User Module, set to PMux, and connected to the analog column buffer, enables testing of the buffer's performance. The project even takes zero bytes of code, because in this mode, the RefMux does not require a start command. The performance of a typical output buffer in the CY8C29466 is shown in Figure 1. The measured output follows the "ideal" output (identical to the input) down to a few millivolts. The typical buffer offset for the CY8C29466 is 3 mV; the one used in Figure 1 has a Vos of about 0.6 mV. The more widely divergent lines show the differences that might occur with larger offset voltage.

Figure 1. Unloaded Buffer Output Drive Level

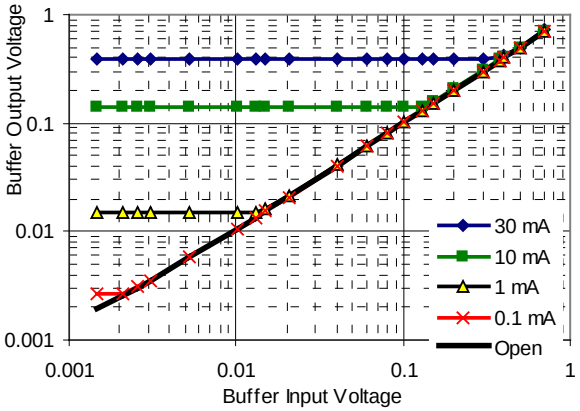


With no load, the buffer output drive limit is the offset voltage. If the load is to circuit ground (V_{SS}, not AGND), the output still follows the slope of Figure 1.

Using the measurement case but with a resistive load from the buffer output to V_{DD}, we can evaluate the drive capability of the buffer. When the PSoC is sinking current (that is, into the chip from pull-up resistor or V_{DD}-referenced load), the output voltage may not reach the expected limit at Vss. For current loads of 0.1, 1.0, 10.0, and 30.0 mA, the output is shown in Figure 2. At each current level, the buffer output voltage follows the no-load curve until the output impedance limit is reached.

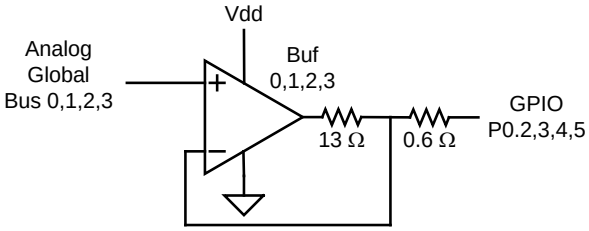
There is a small variation (that is, too small to show up in the plot, but still in the data) in the output curve at each current level before the output curve reaches the drive limit.

Figure 2. Loaded Buffer Output Drive Level



The output of the buffer can be reduced to a simple model, shown in Figure 3.

Figure 3. Buffer Output Model



The 13Ω represents the dynamic output impedance of the buffer opamp. The closed gain drives the output voltage very close to the input, resulting in essentially zero output impedance until the lower output device (an N-channel FET) is driven all the way on. At this point it looks like 13 Ω. The 0.6-Ω resistor represents the resistance of the on-chip routing and the bond wire.

Even at only 10 mA sinking current, the output limits at about 140 mV. If the circuit is a filter or amplifier output, then the absolute output voltage limit usually does not matter as much. Here DAC output performance is more important. The output of a DAC is a function of AGND and reference values in addition to the digital code sent to it. For any AGND and reference combination, the low limit output voltage is given by Equation 1:

$$V_{OutLow} = V_{AGND} - (2^{n-1} - 1) \bullet \frac{V_{ref}}{2^{n-1}}$$

……Equation 1

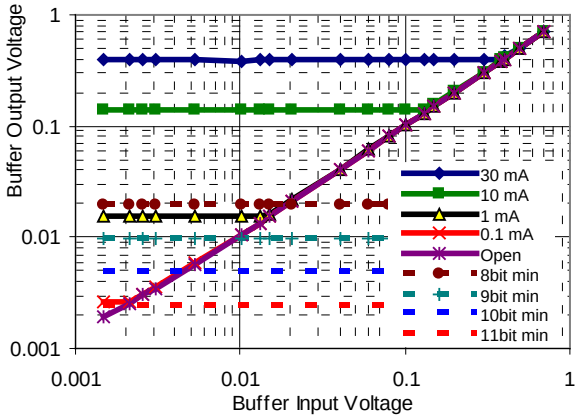
Minimum DAC output voltage for various reference settings is listed in Table 1.

Table 1. Minimum DAC Output for Selected Reference, V_{DD}=5.0

Bits	Vdd/2±Vdd/2	1.6*Vbg±1.6*Vbg	Vbg±Vbg
8	19.5 mV	16.25 mV	10.1 mV
9	9.76 mV	8.13 mV	5.08 mV
10	4.88 mV	4.06 mV	2.54 mV
11	2.44 mV	2.03 mV	1.27 mV

Figure 4 shows the required output at minimum code value compared to the loaded output level.

Figure 4. DAC and Buffer Drive Limits



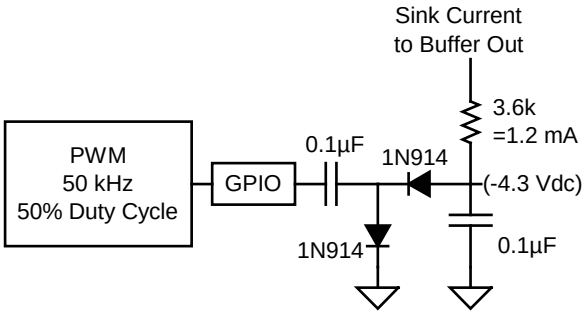
This shows that you can meet the required minimum output voltage level for a 9-bit converter only if the sinking current is less than 700 µA. This may not be enough drive current for a typical application. A typical example is a resistive load terminated to $V_{DD}/2$ or a capacitive coupled load, which results in a maximum resistive load of 2.5 V/0.7 mA = 3.48 kΩ. An example circuit is DAC output for a synthesized signal driven to the zero code at the bottom of its range.

Extending the Output Range

The solution getting more drive current at low voltage is to add a pull down helper. An external pull down resistor can provide the drive current when the output gets below the drive limit. This is done with a resistor to a negative voltage source. If the board does not have a negative supply, make one.

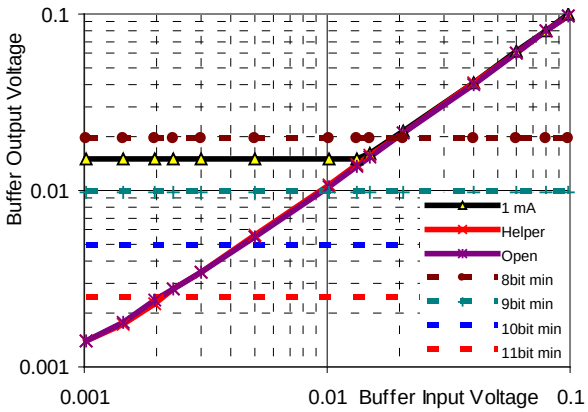
Place a 50 percent duty cycle PWM User Module with an output frequency high enough to filter easily and then connect the boost circuit of Figure 5.

Figure 5. Negative Power Supply



This circuit provides the sinking current near the rail. With the original configuration - a 9-bit DAC and a 1.0 mA pull up load - the buffer could not get down to the required voltage. Adding a 1.2 mA pull down current (3.6 kΩ to negative source), the output now swings all the way to V_{SS}, as shown in Figure 6, tracking the unloaded output all the way to the rail.

Figure 6. Output Tracking with Pull Down



The pull-down resistor draws current all the time. When the basic Class-A output is at AGND (for example, $V_{DD}/2$), there is 2.5 V + 3.6 V = 6.1 V on the resistor for an average current addition of 1.7 mA when the pull down helper is set for 1.0 mA. The design must be able to accommodate this additional current draw. To reduce power, the PWM can be disabled when the DAC output is not required to drive to the rail.

If the project has a low power or sleep mode and the buffer is to be turned off, the negative boost power must be turned off as well. This is done by turning off the PWM before the buffer is turned off so that excess negative current is not pulled from the buffer's GPIO protection diodes.

Driving closer to the rail than required by 9-bit resolution takes a little more current. While 10- and 11-bit DACs are not available as user modules, they can be created using the methods of Application Note AN2117, “DAC 11.” The limit on DACs is normally 9-bit, because this is the maximum resolution at which Cypress guarantees performance. While 10- and 11-bit DACs are possible, Cypress does not guarantee that they will be monotonic.

Collateral Estoppel or You Cannot Have It Both Ways

The output stage is symmetrical. If you add pull down current to drive the output closer to the *negative* rail, that current detracts from the buffer's ability to drive to the *positive* rail. If your design uses DACs and references of AGND/Vref = 1.6*Vbg ± 1.6*Vbg or AGND/Vref = Vbg ± Vbg, then this is not an issue. If, instead, you swing the output to *both* rails with a load greater than 0.5 mA, then the problem is best solved by an external rail-to-rail buffer.

Summary

With a PWM, one GPIO, and a few low cost discrete parts, the PSoC DACs drive much closer to either the V_{SS} or V_{DD} rail, but not both.

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**	848761	SEG	05/23/2007	New Application Note
*A	2675741	SEG	03/18/2009	Updated software version to PSoC Designer 5.0
*B	3187200	SEG	03/02/2011	Updated title, abstract and graphics.
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