Trace design guidelines for XENSIV™ current sensors

Considerations and recipes for external current rail design

About this document

Scope and purpose

This document provides guidelines for designing PCB traces for XENSIV™ current sensors with an external current rail (eCR). The document includes monocell sensing principles, trace design recipes for 1-layer, 2-layer, and 4-layer PCBs, and layout and system-level considerations to support engineers throughout the integration process.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems integrating magnetic current sensors into PCB-based power conversion or motor drive applications.

Keypoints

- **Three rail geometries** are covered; solid, strait, and S-bend; each offering different trade-offs between insertion resistance, power dissipation, bandwidth, and crosstalk
- **PCB stack parameters**, such as copper thickness, core thickness, and layer count directly determine the transfer factor, system sensitivity, and power dissipation. Doubling the copper thickness halves the power dissipation with negligible impact on sensitivity
- **Crosstalk in three-phase systems** can be managed by design (S-bend geometry, sufficient phase spacing) or by firmware-based compensation using a simulated or measured crosstalk matrix
- **Bandwidth depends on sensor-to-conductor displacement:** Minimizing the vertical gap and aligning the sensor toward the conductor edge at high frequencies maximizes usable bandwidth
- All case studies are based on the XENSIV™ TLx5572 TMR-based current sensor, simulated using the Infineon XENSIV™ current sensor simulation tool, with a 3 W dissipation limit as the design boundary

About this product family

Product family

Infineon's XENSIV™ current sensors deliver precise AC and DC current measurements with internal current rail (iCR) packages and up to several kiloamps with external current rail (eCR) packages.

Target applications

- Server power supply units (PSU)
- DC-DC converters
- On-board charging
- General purpose motor drive
- Photovoltaic

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1 Introduction

In the context of coreless current sensing, one of the primary challenges in integrating magnetic current sensors with an external current rail is achieving an optimal current rail design. This document serves for designing external current rails at the PCB level, offering a structured decision tree approach while addressing the following key variables: number of PCB layers, copper thickness, crosstalk, bandwidth requirements, and more.

The document is primarily divided into three core sections:

Design considerations for external current rails

Essential factors that impact current rail design for monocell sensors, providing a foundational understanding of the requirements and trade-offs involved.

Pre-defined trace designs and case studies

This section introduces case studies tailored to specific PCB types (1-layer, 2-layers, and 4-layers) to address diverse application requirements using the XENSIV™ TLx5572 TMR-based current sensor:

- **1-layer PCB:** Explores design possibilities and calculates system sensitivity based on the simulated transfer factor of the current rail
- **2-layer PCB:** Analyzes configurations with the sensor on the top layer and the current rail on the bottom layer, focusing on factors, such as copper thickness and power dissipation
- **4-layer PCB:** Investigates high-performance designs, such as 60 A full-scale, high-frequency applications, emphasizing crosstalk implications, and strategies for either mitigation or compensation

Layout and system considerations

Guidance on layout optimizations and broader system-level factors that influence the integration of current rails, such as sensor placement, parasitics, and mechanical constraints.

Explores the relationship between sensitivity and bandwidth with respect to the displacement between the sensor traces and the primary conductor. Considerations such as the impact of skin effect at high frequencies are also analyzed in detail.

Tailored to support integrators in selecting appropriate sensing structure designs for their applications while providing actionable advice for designing custom current rails used as sensing structures. Ultimately, the goal is to streamline the design process, ensure performance optimization, and address common application-specific challenges encountered in coreless current sensing systems.

Depending on the design of the external current rail, the XENSIV™ TLx5572 TMR-based current sensor can be utilized in systems handling currents ranging from tens to hundreds of amperes. For instance, 6-layer design is presented, refined for sensing a maximum current of ±165 A, as referred in [3].

2 General considerations

2.1 Monocell sensing principle

Monocell magnetic sensing involves placing a single sensing cell adjacent to a continuous, current-carrying copper conductor. This design allows the system to measure the local magnetic field without the need for ferromagnetic cores. Through careful PCB design, monocell sensing aims to maximize the magnetic signal from the intended conductor while minimizing the influence of other nearby conductors and switching elements in the system.

The monocell sensing principle offers the following key advantages:

- **Simplified conductor design:** A single, strait, wide copper segment can serve as the sensing structure, simplifying PCB routing and electromagnetic modeling
- **Low resistance:** A continuous, wide current path minimizes I^2R losses and self-heating, improving thermal performance and efficiency
- **Low inductance:** Avoiding the use of vias and multilayer current paths reduces parasitic inductance, thereby lowering switching overshoot and improving system stability
- **Strong Bx signal:** Aligning the sensor with the dominant magnetic field component near a strait conductor maximizes sensitivity and signal-to-noise ratio (SNR)
- **Top layer available for routing:** Placing the high-current path on a dedicated power layer eliminates congestion on the top PCB layer, allowing for short, clean routing of sensor and control signals
- **No inner-to-outer layer transitions using vias:** Unlike shunt-based designs, monocell sensing minimizes the need for vias in the current path, which reduces added resistance, inductance, and local magnetic field distortion
- **Cost-effective solution:** Monocell sensing is an economical approach for strait forward applications while still offering high accuracy and performance. Its competitiveness extends demanding segments like the automotive market

By leveraging these advantages, the monocell sensing principle is a highly flexible and efficient solution for modern PCB-based current measurement systems.

2.1.1 Crosstalk

In three-phase systems, three independent monocells are arranged to measure currents IU (Phase U), IV (Phase V), and IW (Phase W) without the use of ferromagnetic cores. The goal is to capture the local magnetic field from each phase while minimizing interference from neighboring phases and high-frequency switching nodes.

Crosstalk occurs when the magnetic field from Phase V or W influences the sensor intended for Phase U. This interference can add to or subtract from the local field being measured, introducing a proportional error. The severity of the error depends on key factors such as the physical spacing between current paths, their relative orientations, and the instantaneous currents in the other phases.

When integrating a magnetic current sensor with an external current rail into a three-phase current sensing system, two primary approaches to managing crosstalk can be considered:

Accept and compensate for crosstalk

Recognize the coupling between phases and implement firmware-based compensation strategies. This approach involves the following steps:

- Simulate the system to determine the current rail's crosstalk behavior, generating a corresponding crosstalk matrix that quantifies inter-phase interaction. Otherwise, for a more accurate implementation, measure the crosstalk matrix on a statistically relevant number of produced systems and use the average matrix for the compensation of all production systems
- Implement a compensation matrix in the microcontroller firmware that adjusts readings based on simulated or measured crosstalk data
- Sample all sensors simultaneously to ensure synchronization and accuracy in compensation

Note: *The "crosstalk matrix" is a mathematical representation of the coupling coefficients between each phase's sensor and the neighboring conductors. This matrix can be obtained from the Infineon's Current Sensor Simulation Tool.*

Reduce or eliminate crosstalk through design

Minimize or eliminate coupling between phases by making strategic design changes to the current rail. Techniques include:

- **S-Bend rail configuration:** Using an "S-shaped" conductor layout to cancel magnetic field contributions from neighboring phases by exploiting symmetry in the magnetic field lines
- **Sufficient spatial separation:** Increasing the physical distance between phases to reduce magnetic coupling. The required separation depends on factors, such as the operating current, conductor geometry, and switching frequency. Proper simulation during the design phase can help determine the optimal spacing for a given application

Note: *The "S-bend" rail configuration is particularly effective in high-density PCBs as it reduces field interference while maintaining compact layouts.*

By combining simulation and design optimization, system engineers can manage crosstalk effectively in three-phase systems. Selecting the appropriate approach depends on application requirements, precision needs, and system constraints.

The "S" shape current rail design is an effective strategy for mitigating crosstalk in three-phase systems. In this design, the sensor must be oriented at a 90° angle relative to its nominal case, ensuring that the sensing direction aligns with the magnetic field generated at the center of the "S" shape. This specific orientation ensures that the sensor is insensitive to magnetic fields in the yz-plane, thereby reducing the impact of a single phase's magnetic field on sensors associated with the other two phases.

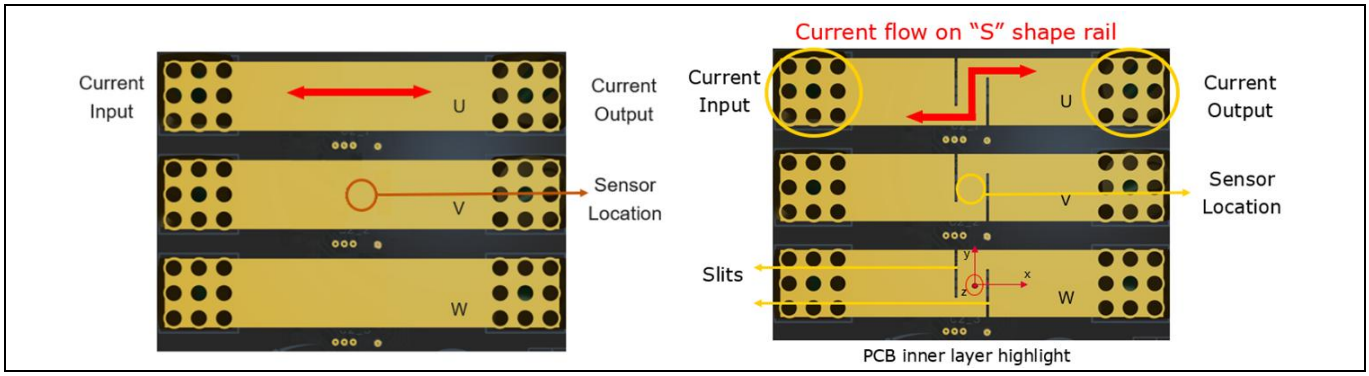


Figure 1 Crosstalk reduction technique

The magnitude of the magnetic field decreases proportionally to the square of the distance from the source conductor. For example, with an “S-bend” design, at a separation distance of 10 mm, crosstalk between phases are reduced to 0%. This value is negligible, particularly when compared to typical sensor error tolerances. Consequently, maintaining sufficient spacing between the current rails of different phases is a design parameter that can significantly contribute to crosstalk minimization.

While the "S-bend" design and spatial separation reduce crosstalk significantly, any residual coupling can be compensated systematically in software for the affected phase sensor. The compensation process involves:

- **Determining the crosstalk factor:** Using the Infineon’s Current Sensor Simulation Tool, derive the coupling coefficient (crosstalk matrix) between the source phase and the affected phase as a function of current rail geometry
- **Simultaneous sampling:** Simultaneously sample output signals from all three sensors to maintain synchronization across phases
- **Compensation calculation:** Subtract the readout current of the source phase scaled by the crosstalk factor from the affected phase sensor's output

This compensation ensures accurate current measurement despite minimal residual crosstalk effects. Proper implementation requires precise system characterization during the design phase.

2.1.2 Stray field sensitivity

Stray fields can significantly impact the performance of magnetic current sensors, especially in high-power applications where strong electromagnetic interference (EMI) is present. The primary sources of stray fields include: high di/dt switching nodes in power converters, DC-link current loops, gate driver switching currents, transformer, and inductor fringe fields.

These stray field sources create broadband, high-frequency magnetic disturbances that can couple into the sensors, particularly in applications with large copper areas, return planes, or poorly shielded assemblies. The result is an additional noise floor, duty-cycle-dependent signal ripple, and even apparent phase imbalance in multi-phase systems. At higher frequencies, induced eddy currents in nearby copper pours can redirect magnetic fields, causing frequency- and temperature-dependent variations in the sensor’s readings.

When assessing the impact of stray fields on sensor performance, particular attention must be given to the sensor’s placement and the surrounding environment. Following are the key considerations for minimizing the influence of stray fields:

- **Placement of cables inside the final assembly:** Power cables generate associated magnetic fields. When such cables are brought close to a monocell sensor, the resulting stray field influences the sensor output

- **Placement of different components at the PCB level:** Connectors or other materials containing ferromagnetic particles can become magnetized. If these are located close to the integrated sensor, they create offsets in the sensor readings
- **Placement of magnetic components near the sensor:** Components such as magnets, coils, or chokes can influence the sensor readings with their magnetic fields. These components can be included in the design, but their placement needs to be carefully considered to minimize their magnetic impact on the sensor

2.2 Trace design initial guidelines

- **Maximize spacing to other current paths:** Increase the centerline distance from neighboring conductors and reduce the length over which they run parallel to the sensor segment
- **Place the sensitive axis correctly:** Align the sensor with the tangential field of the target conductor and avoid orientations where fields from other conductors project strongly onto the same axis
- **Control local return currents and loop areas:** Keep high-di/dt loops physically distant, tightly couple forward and return paths, and prevent unrelated high-frequency returns from flowing underneath the sensing region
- **Maintain geometric symmetry:** Ensure the local environment around the monocell is uniform to improve common-mode rejection and simplify calibration
- **Avoid large copper pours directly beneath the sensor:** If complete avoidance is not possible, create cut-outs in the copper pours under the sensor area
- **Place connectors and harness transitions away from the sensor:** Avoid sharp turns, compressed loop areas, and bundled cables crossing the sensing region
- **Avoid magnetic materials near the sensor:** Ferromagnetic components and unintended shields can distort the local magnetic field and introduce temperature-dependent errors

2.3 Integration flow for external current rail

Figure 2 shows the integration flow of a current sensing solution with an external current rail.

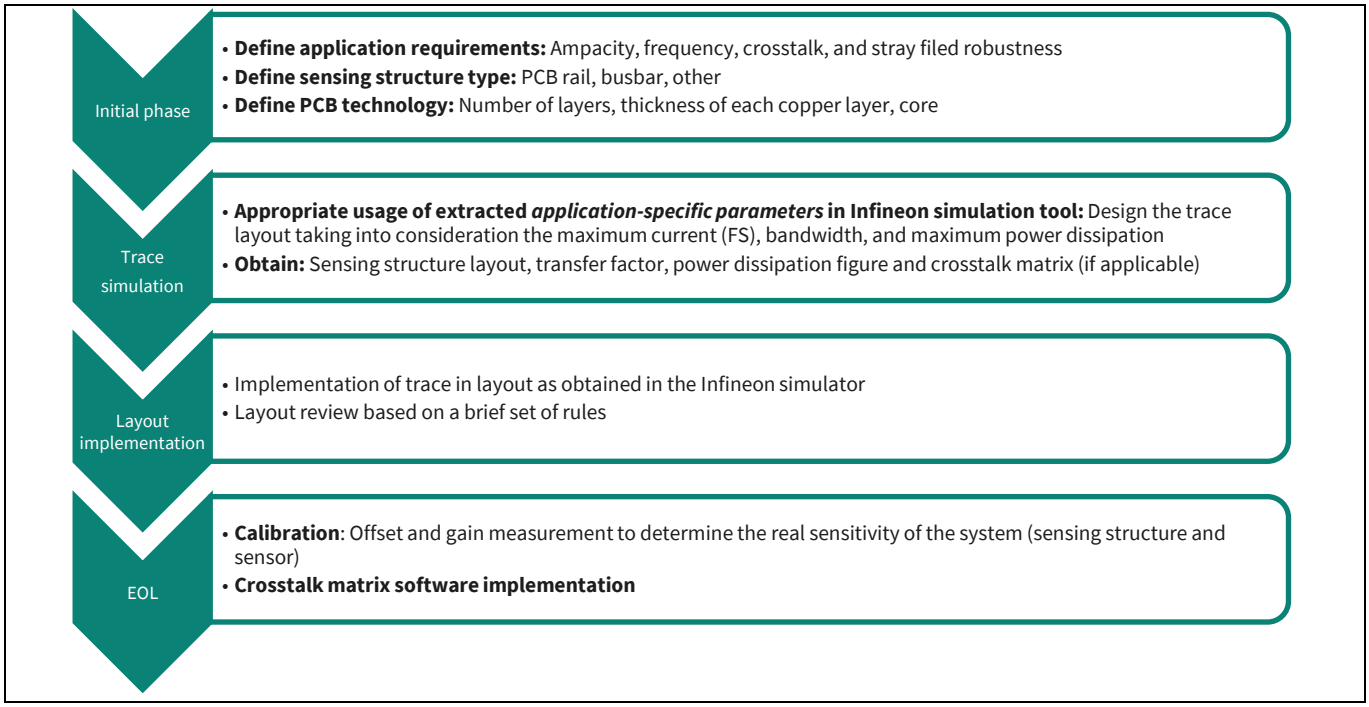


Figure 2 Integration flow for an external current rail

3 Recipes for trace design

The recipes for trace design are simulated with Infineon's online Current Sensor Simulation Tool.

From this tool, when selecting the "***PCB Design***" tab, there are three options for copper rail geometry: Solid, strait, and S-bend. The parameters of each structure are shown in Figure 3.

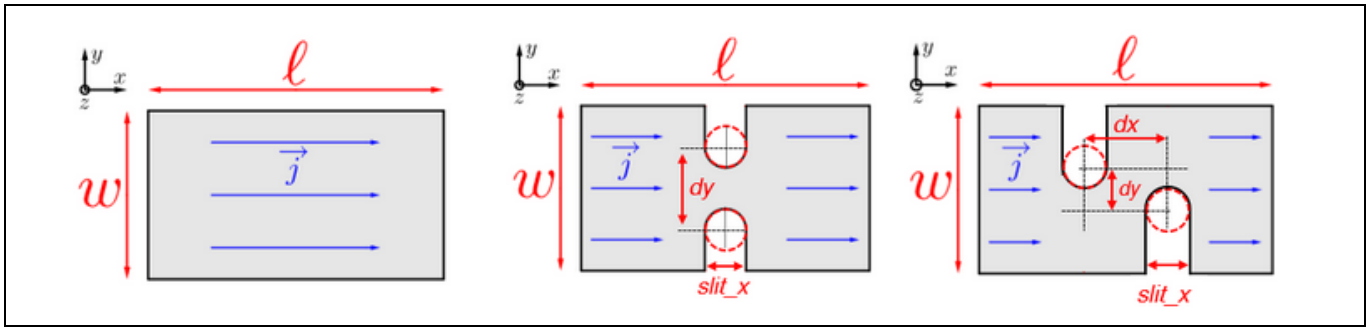


Figure 3 Current rail geometries: Solid, strait, and S-bend

In the case of strait and S-bend designs, observe a short area in which the current rail narrows. This leads to an increased local current density, therefore increased insertion resistance. The resulted temperature rise is dissipated on the rest of the copper rail. As a thumb rule, it is a good practice to design the traces having the power dissipation is below 3 W. This value is a good trade-off for most applications in terms of area-bandwidth-thermal dissipation.

The simulator outputs the resulting insertion resistance and based on this, it computes the estimated power dissipation at I_{RMS} as $P = I_{RMS}^2 \times$ Insertion resistance.

Note: Each recipe that is described in this chapter has a table with the parameters. This also contains details about orientation and displacement from the center of the rail.

This section includes three case studies, based on the available PCB type, tailored for specific applications.

- **Case study for 1-layer PCB: Exploring feasible design possibilities**
  - Calculate system sensitivity using the simulated transfer factor of the current rail
- **Case study for 2-layer PCB: Configuration with the sensor on the top layer and the current rail on the bottom layer**
  - Focus on parameters such as thickness, power dissipation, and current density
- **Case study for 4-layer PCB: 60 A full scale, high frequency application**
  - Examining crosstalk implications with strategies to either mitigate or compensate

For detailed information about the simulator and the pre-defined structures, refer application note [2].

Note: All case studies are based on integrating the XENSIV™ TLx5572 TMR-based current sensor.

Note: Some simulation results may slightly differ if re-simulated due to simulator updates.

3.1 Case study for 1-layer PCB

For applications with the constraint of having only the top-layer available for routing the external current rail, there is a solution to route it directly between the pins of the sensor.

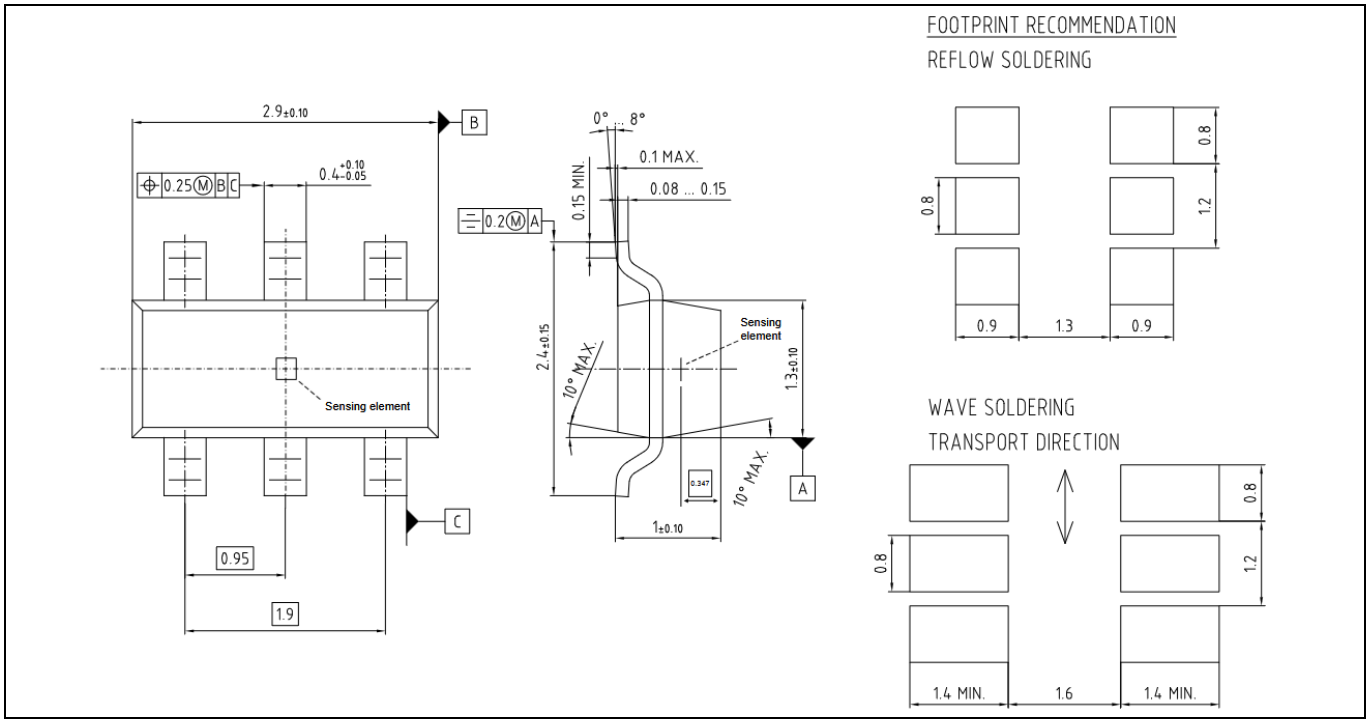


Figure 4 PG-SOT23-6-4 package outline

The XENSIV™ TLx5572 TMR-based current sensor has the PG-SOT23 package described in Figure 4. The distance between the solder pads is 1.3 mm, allowing space for a current rail with a maximum width of 1 mm, subject to the design rules of each integrator.

Table 1 Parameters for simulating a solid top-layer current rail

Parameter	Value
Geometry	Solid
L	10 mm
W	1 mm
Copper layer thickness	35 µm

The simulation shows a system transfer factor of 227.24 µT/A.

Table 2 Simulation results for 3.3 V supply

Sensitivity range	Specified sensitivity for each variant (mV/mT)	Calculated sensitivity of the system (mV/A)	Maximum current for FS (A)	Power dissipation at I_{RMS} (W)
S1: 25 mT	53.5	12.16	110.5	18.05
S2: 16 mT	85.5	19.43	69.14	7.07
S3: 12 mT	107	24.31	55.25	4.51
S4: 8 mT	172	39.09	34.37	1.75
S5: 6 mT	214	48.63	27.63	1.13
S6: 4 mT	340	77.26	17.39	0.45

Full scale (FS) current refers to the peak current flowing through the system, while power dissipation is computed at the estimated equivalent I_{RMS}.

To determine the “Calculated sensitivity of the system in mV/A”, the obtained transfer factor of 227.24 µT/A is multiplied by the specified sensitivity for each variant of the sensor.

Rationale example

With this configuration of the current rail, for a 3.3 V supply, the integrator can measure:

- **With S4 variant:** ±34.4 A FS, with a sensitivity of the system of 39 mV/A
- **With S5 variant:** ±27.6 A FS, with a sensitivity of the system of 48.6 mV/A
- **With S6 variant:** ±17.4 A FS, with a sensitivity of the system of 77.2 mV/A

Note: In this case, increasing the thickness of the copper layer from 35 µm to 70 µm reduces power dissipation without significantly influencing the transfer factor of the rail.

Table 3 shows the 5 V supply simulation results.

Table 3 Simulation results for 5V supply

Sensitivity range	Specified sensitivity for each variant (mV/mT)	Calculated sensitivity of the system (mV/A)	Maximum current for FS (A)	Power dissipation at I_{RMS} (W)
S1: 41 mT	53.5	12.16	177.67	46.65
S2: 25 mT	85.5	19.43	111.17	18.27
S3: 20 mT	107	24.31	88.84	11.66
S4: 13 mT	172	39.09	55.26	4.51
S5: 10 mT	214	48.63	44.42	2.92
S6: 6 mT	340	77.26	27.96	1.16

While keeping all the parameters as they are: solid geometry, length 10 mm and 35 µm and sweeping the width of the rail, the graph shown in Figure 5 is obtained.

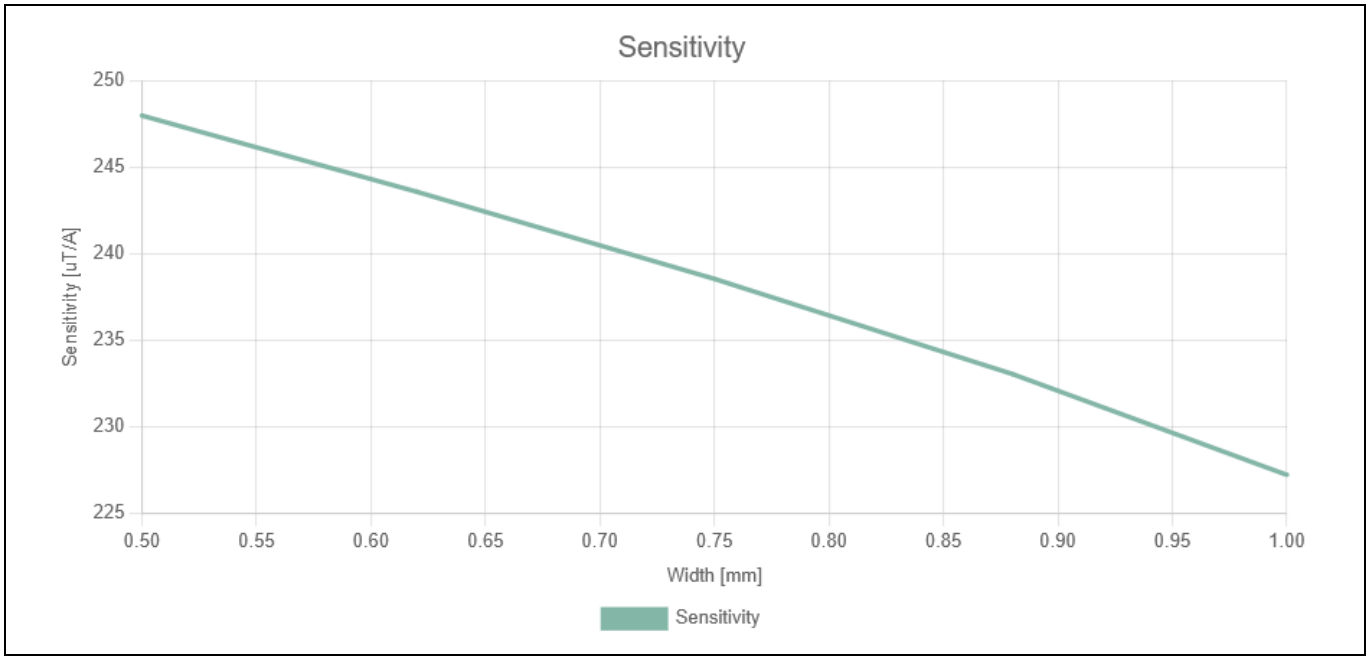


Figure 5 Width sweep for 1-layer trace design

3.2 Case study for 2-layer PCB

Section 3.1 has defined the transfer factor of the current rail and system sensitivity. This section shows how the thickness of the copper and the core of the PCB affects the power dissipation and the transfer factor of the current rail.

3.2.1 PCB layers thickness influence on rail parameters

Initial assumptions: 3.3 V supply, 2-layer PCB. TLx5572 sensor placed on the top layer, current rail designed on the bottom layer.

Table 4 Nominal simulation

Parameter	Value
Geometry	Solid
L	15 mm
W	5 mm
PCB Layer 1 thickness	35 µm
PCB Core thickness	180 µm
PCB Layer 2 thickness	35 µm

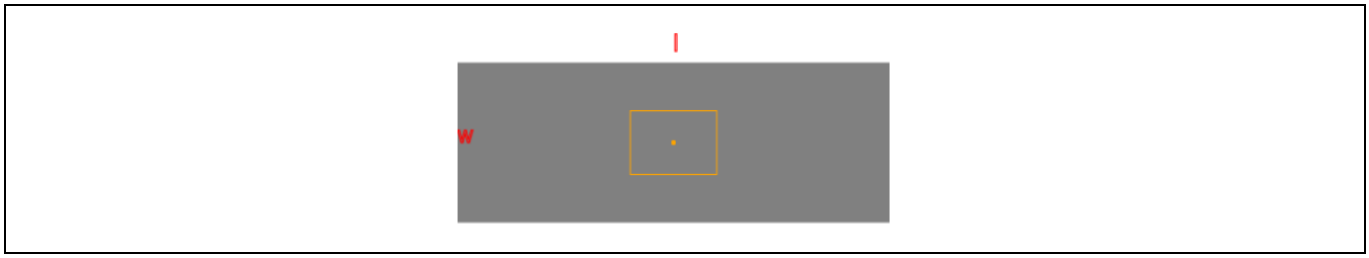


Figure 6 TLx5572 on top of the current rail

Table 5 Nominal simulation results for 3.3V supply; 35 µm thick copper rail

Sensitivity range	Specified sensitivity for each variant (mV/mT)	Calculated sensitivity of the system (mV/A)	Maximum current for FS (A)	Power dissipation at I_{RMS} (W)
S1: 25 mT	53.5	5.03	267.3	21.12
S2: 16 mT	85.5	8.03	167.26	8.27
S3: 12 mT	107	10.05	133.65	5.28
S4: 8 mT	172	16.16	83.14	2.04
S5: 6 mT	214	20.10	66.83	1.32
S6: 4 mT	340	31.94	42.06	0.52

Variants S1, S2, and S3 are excluded due to high power dissipation, as the rule of thumb is set at 3 W. By keeping every parameter unchanged, only the PCB Layer 2 thickness is updated to 70 µm.

Table 6 Nominal simulation results for 3.3V supply; 70 µm thick copper rail

Sensitivity range	Specified sensitivity for each variant (mV/mT)	Calculated sensitivity of the system (mV/A)	Maximum current for FS (A)	Power dissipation at I_{RMS} (W)
S1: 25 mT	53.5	5.00	268.77	10.68
S2: 16 mT	85.5	7.99	168.18	4.18
S3: 12 mT	107	10.00	134.38	2.67
S4: 8 mT	172	16.07	83.6	1.03
S5: 6 mT	214	19.99	67.19	0.67
S6: 4 mT	340	31.77	42.29	0.26

Doubling the thickness of the copper directly results in a halving of the power dissipated in the current rail, without dramatically influencing the transfer factor of the current rail.

Similarly, going back to the nominal simulation, the next step is to sweep the PCB core thickness to observe how distance affects the sensitivity. Keeping the L, W, and PCB copper thicknesses as in the nominal case, but sweeping the core thickness from 150 µm to 900 µm. Table 7 shows a graph of this dependency.

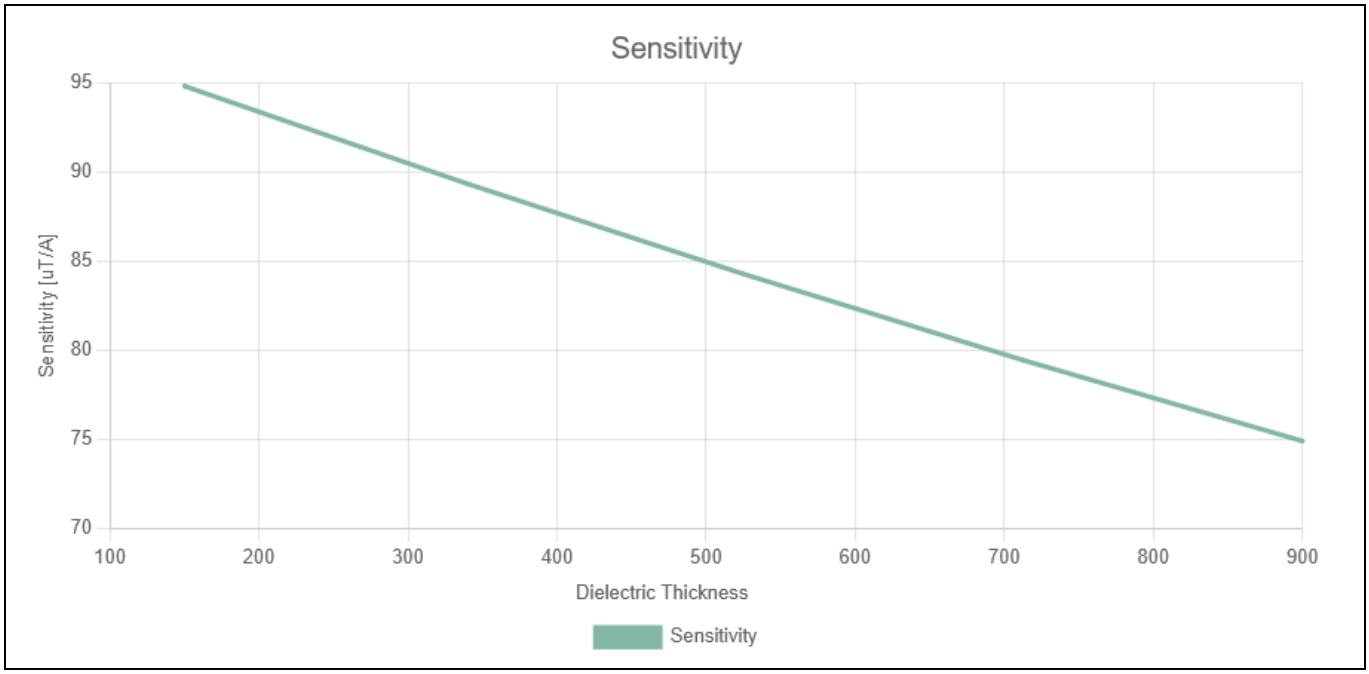


Figure 7 Impact of PCB core thickness on system sensitivity

3.2.2 Case study conclusion

- A system as described in Section 3.2.1, the nominal simulation, can satisfy three different ampacity requirements, by choosing the correct variant of the sensor:
  - **S4 variant:** ±83 A FS range, 16.15 mV/A calculated sensitivity
  - **S5 variant:** ±66.8 A FS range, 20 mV/A calculated sensitivity
  - **S6 variant:** ±42 A FS range, 32 mV/A calculated sensitivity
- Doubling the thickness of the copper directly results in halving the power dissipated at the current rail level
- Increasing the thickness of the PCB core, the distance between sensor and conductor decreases the sensitivity of the system, resulting in a larger full-scale current range

3.3 Case study for 4-layer PCB: 60 A, high frequency application

In this section, an application with a maximum current of 60 A is proposed, with a cut-off frequency requirement higher than 100 kHz. The requirement is to use a 4-layer PCB. The two inner layers and the bottom layer are used for routing. The copper thickness of inner layers is 35 µm, with a distance of 180 nm between them. The bottom layer has a 70 µm thickness.

3.3.1 S-bend configuration

Table 7 Parameters for S-bend geometry, 60 A, 100 kHz application

Parameter	Value
Geometry	S-bend
L	20 mm
W	9 mm
Slit_dx	5 mm
Slit_dy	0 mm
Slit_x	2 mm
X-offset	1.5 mm
Z-twist Y	90 deg

With these parameters, the resulted transfer factor for this sensing structure is 55.66 µT/A.

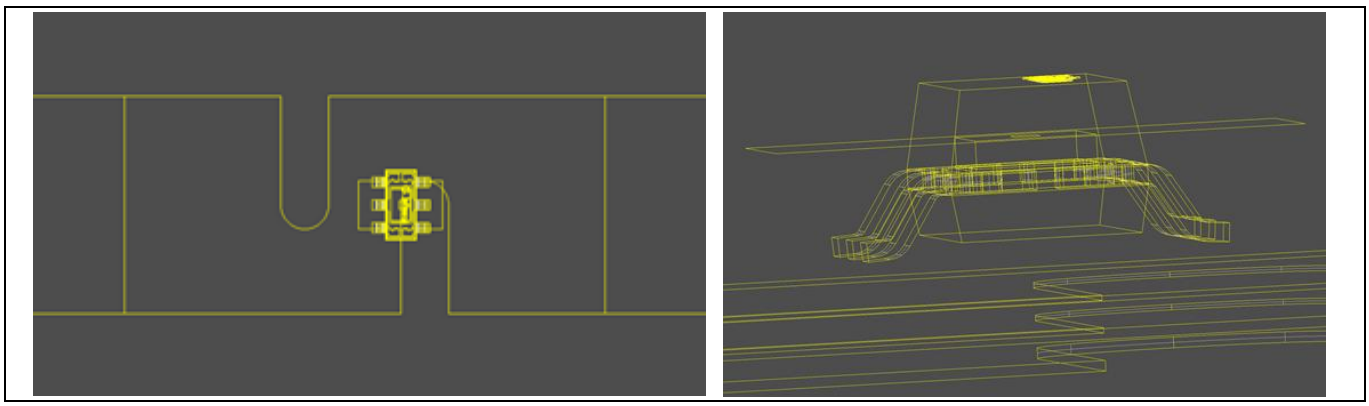


Figure 8 Resulted S-bend design

For XENSIV™ TLx5572 TMR-based current sensor, the S6 version has a sensitivity of 360 mV/mT. This, multiplied by the rail transfer factor of 55.66 µT/A gives a final sensitivity of the system of 20.037 mV/A, with a total power dissipation of 0.71 W.

The X-offset contributes to a better frequency response of the system. At high frequencies, the current density is higher around the edges of the copper rail due to skin effect. Displacing the sensing element towards the edge of the copper rail improves the bandwidth of the system.

The resulting maximum current for full scale is 67.05 A, with an insertion resistance of 316.281 µΩ. Resistance of an ideal solid busbar with height = 140.0 µm is 273.673 µΩ. Resistance of selected PCB stack with 'S-bend' current rail structure is 589.954 µΩ. Resistance increase with respect to ideal solid busbar (cost of insertion) is 115.57 percent or 316.281 µΩ.

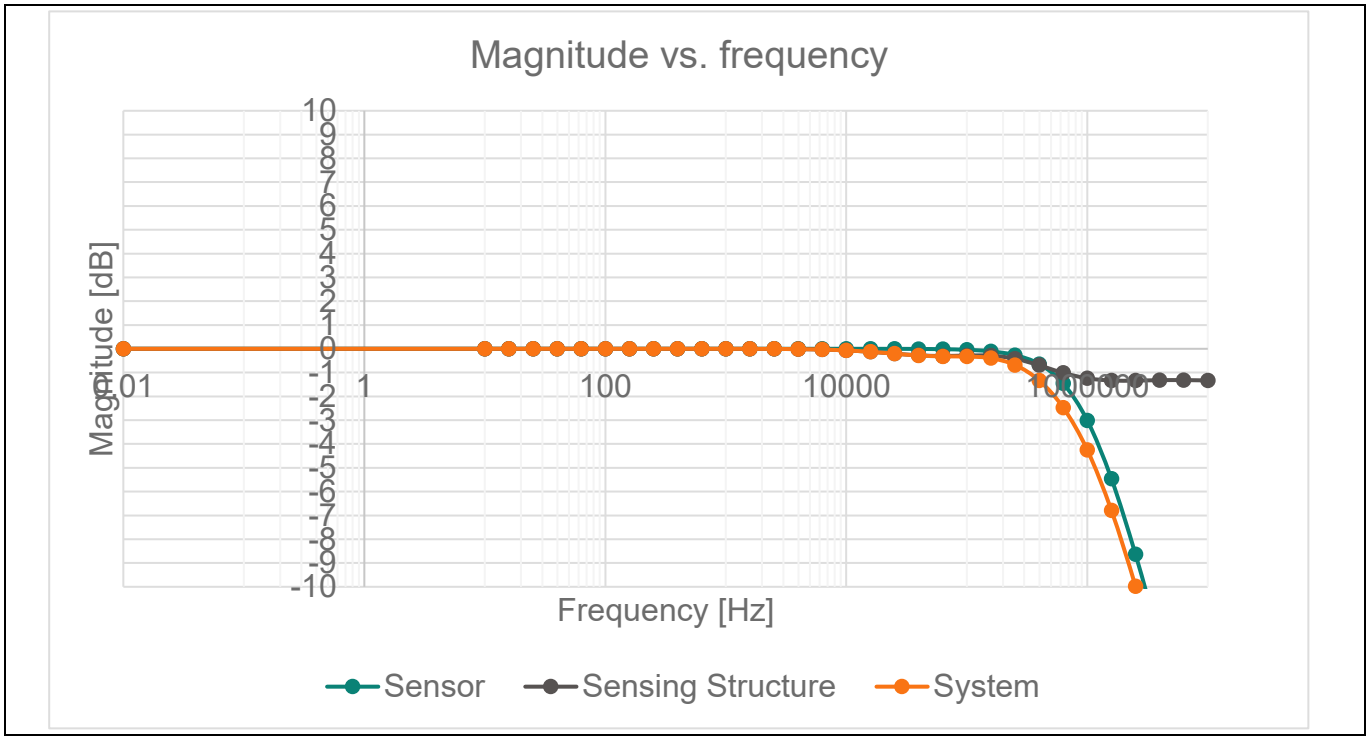


Figure 9 Frequency response for 60 A S-bend geometry

From the frequency response simulation, observe that the bandwidth of the system is higher than 500 kHz.

3.3.2 Strait configuration

Table 8 Parameters for strait geometry, 60 A, 100 kHz application

Parameter	Value
Geometry	Strait
L	20 mm
W	9 mm
Slit_dy	7 mm
Slit_x	1.5 mm
X-offset	0 mm
Y-offset	2.5 mm
Z-twist Y	0 deg

For this configuration, the resulted transfer factor is 56.75 µT/A.

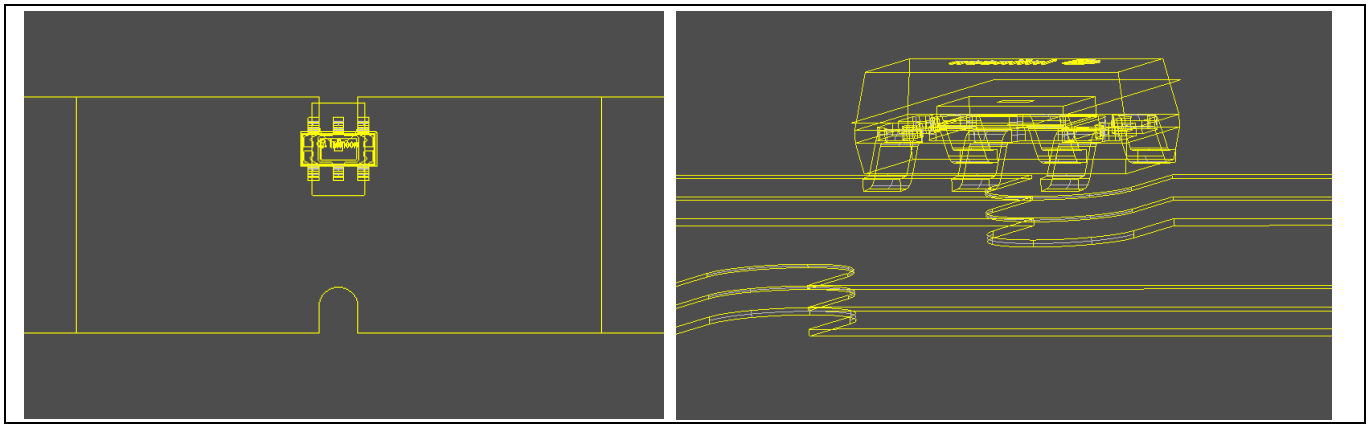


Figure 10 Resulted strait design

For XENSIV™ TLx5572 TMR-based current sensor, the S6 version has a sensitivity of 360 mV/mT. This, multiplied with the rail transfer factor of 56.75 µT/A gives the final sensitivity of the system of 20.429 mV/A, with a total power dissipation of 0.06 W.

The resulted maximum current for full scale is 65.76 A, with an insertion resistance of 25.923 µΩ. Resistance of an ideal solid busbar with height = 140.0 µm is 273.673 µΩ. Resistance of selected PCB stack with 'S-bend' current rail structure is 589.954 µΩ. Resistance Increase with respect to ideal solid busbar (cost of insertion) is 9.47 percent or 25.923 µΩ.

Since this design is clearly better-performing in terms of insertion resistance, the main disadvantage here is the crosstalk in the 3-phase system. The calculation was made with the assumption that there is 10 mm of spacing between the rails of each phase. To compensate for this effect, a crosstalk matrix is provided in Table 9.

Table 9 Crosstalk matrix (µT/A)

	Busbar left	**Busbar center**	**Busbar right**
Busbar left	56.75	0.45	0.07
Busbar center	1.17	56.75	0.45
Busbar right	0.12	1.17	56.75

Once all coefficients of the crosstalk compensation matrix are known, the user can calculate the corrected sensor output voltages [V_{O1}, V_{O2}, V_{O3}] starting from the measured current at the three phases [I_{PH1}, I_{PH2}, I_{PH3}].

Example: Coefficient a_{12} shows how much the current through the left rail affects the readings in the center rail.

$$\begin{bmatrix} V_{O1} \\ V_{O2} \\ V_{O3} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} X \begin{bmatrix} I_{PH1} \\ I_{PH2} \\ I_{PH3} \end{bmatrix}$$

Equation 1 Offset computation based on crosstalk matrix

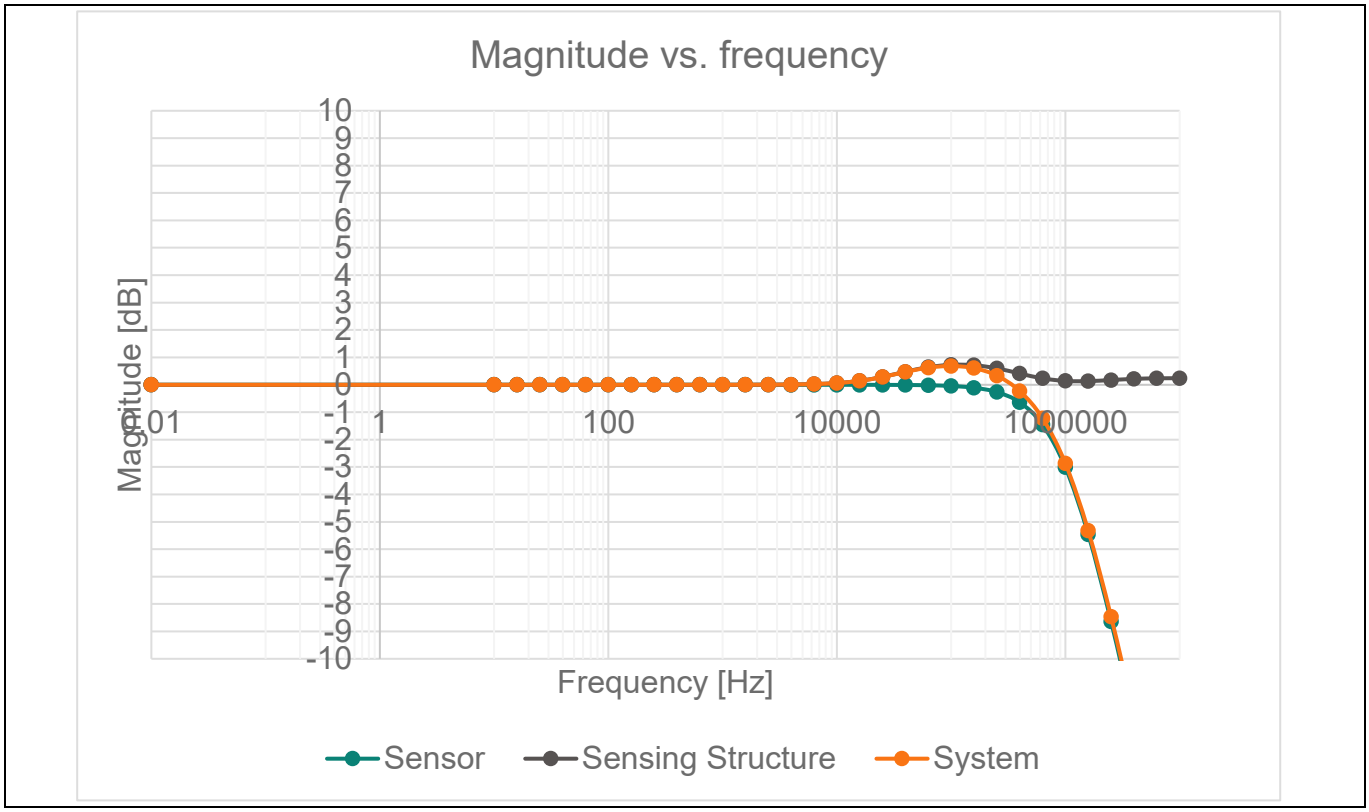


Figure 11 Frequency response for 60 A strait geometry

This design is optimized for frequency response. The bandwidth of the system is higher, almost 1 MHz.

3.3.3 Case study conclusion

The application requirements:

- 60 A full scale
- Measured-signal bandwidth greater than 100 kHz
- 4-layer PCB with the stack description shown in Figure 12

Solder Resist Top	0 µm	
Layer1	35 µm	
Dielectric 1	180 µm	
Layer 2	35 µm	☑ Contains Current Rail
Core	180 µm	
Layer 3	35 µm	☑ Contains Current Rail
Dielectric 2	180 µm	
Layer 4	70 µm	☑ Contains Current Rail
Solder Resist Bottom	0 µm	

Figure 12 Example layout

3 Recipes for trace design

Each design has its advantages and disadvantages, and every integrator is able to choose the right design for its application. In the studied case, both rails have similar dimensions and a suitable full-scale range and bandwidth. The decision is made based on the ability to implement crosstalk mitigation techniques.

- Choose strait design if the integrator can sample all three sensors at the same time and make the crosstalk-compensation calculations in the microcontroller code and benefit from the reduced power dissipation
- Choose S-bend design if the integrator desires minimum effort on the microcontroller-code development side and can tolerate the local hotspot. In this specific case the power dissipation is under 1 W, meaning that the S-bend configuration would not cause a significant heating at the PCB level

Table 10 Comparison between the strait and S-bend design

Parameter	Strait	S-bend
Full-scale	±65.8 A	±67 A
L/W	20 mm/9 mm	20 mm/9 mm
Bandwidth	~1 MHz	~800 kHz
Power dissipated	0.06 W	0.71 W
Insertion resistance	25.923 µΩ	316.281 µΩ
Crosstalk between phases	Up to 1.2%	Almost 0%
Parameter	Strait	S-bend

4 Layout and system considerations

In this section describes other factors to be considered when designing the copper current rail.

4.1 Bandwidth – a function of displacement

The sensor's usable bandwidth is directly influenced by the sensor-to-conductor displacement. As the separation increases, magnetic coupling decreases approximately proportional to 1/r. This reduction in magnetic signal strength, while the front-end/parasitic roll-offs and noise remain constant, leads to a drop in the SNR-limited bandwidth.

At higher frequencies, the skin effect and proximity effect can cause current to concentrate on the outer surfaces and edges of conductors, reshaping the magnetic field distribution. A sensor positioned at the center of a wide conductor may experience a perceived gain drop with increasing frequency, whereas a sensor placed closer to the edge may show less gain drop or even a slight increase.

To manage these effects, it is crucial to control and model both vertical (z-axis) and lateral displacement. Key considerations include: keeping the z-gap as small as possible, aligning the sensor cell with the dominant high-frequency current path, or averaging the measurement across the conductor's width to reduce sensitivity to skin-effect-related magnetic field changes.

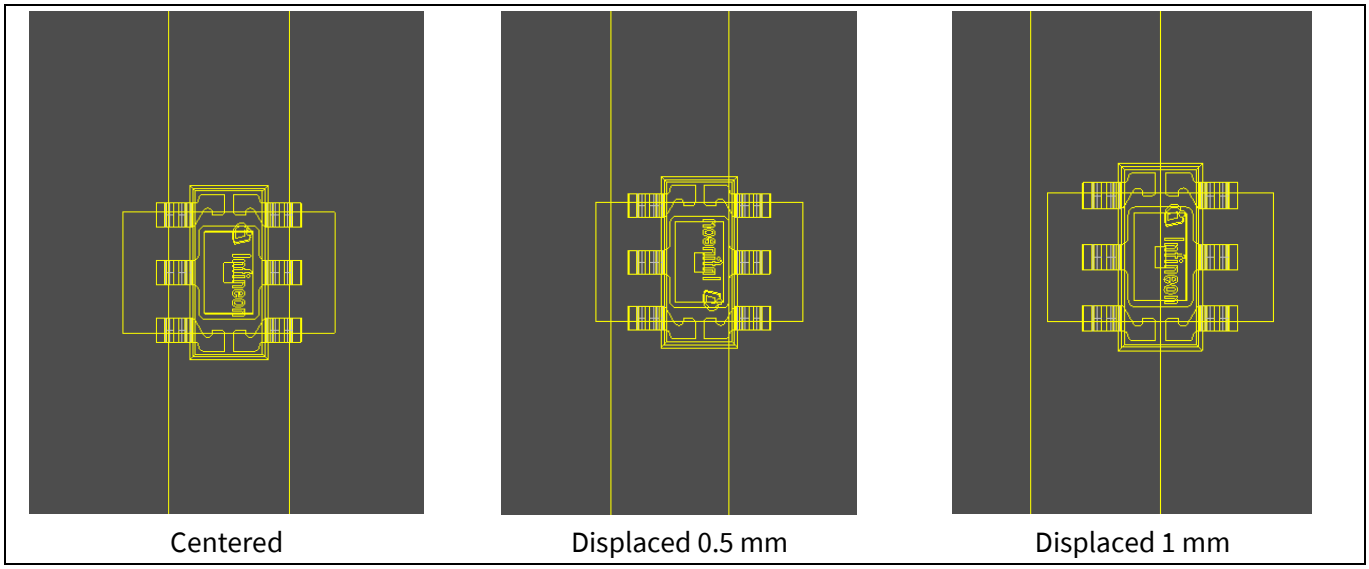


Figure 13 Case study setup

For demonstrating the bandwidth function of sensor displacement, a case study was performed:

Assume a solid geometry (see Figure 3) with l = 10 mm and w = 2 mm. The structure itself has a monocell field transfer factor of 126.79 µT/A. The proposed sensor is the XENSIV™ TLx5572 TMR-based current sensor, with a VDD of 3.3 V. Three simulations are made, with 3 different displacements for the sensor, relative to the copper trace: 0, 0.5, and 1 mm (see Figure 14).

Figure 14 shows the change in the system total sensitivity by varying only the displacement.

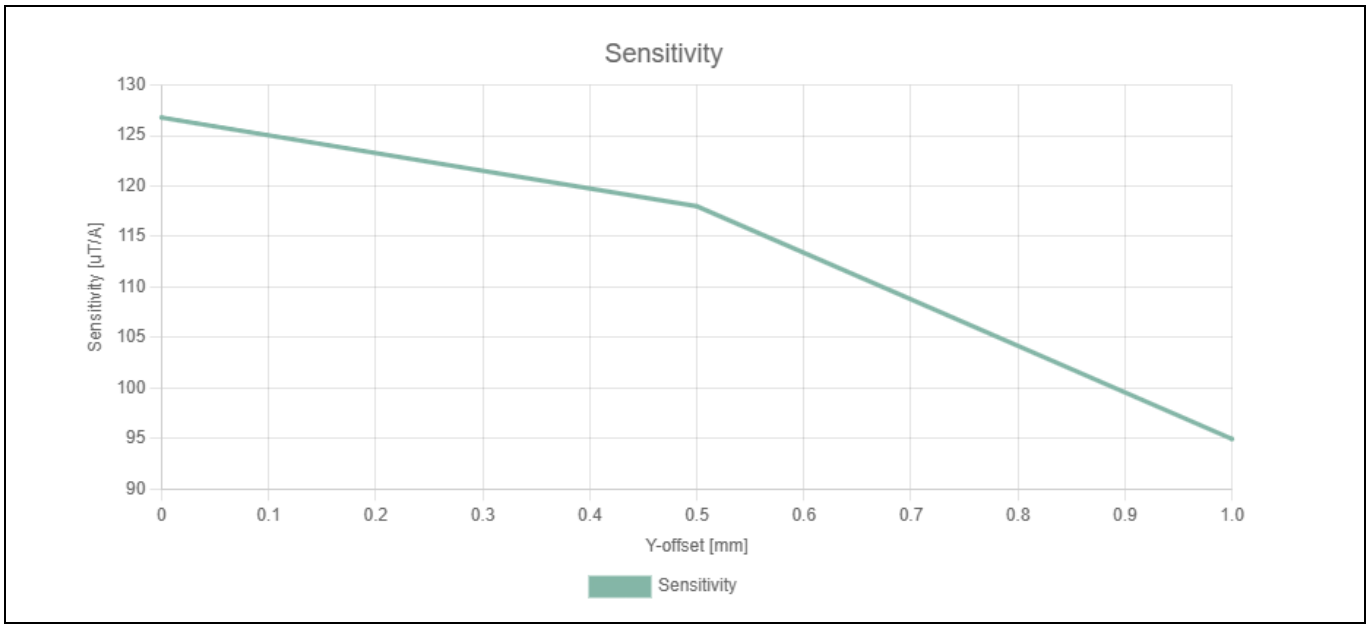


Figure 14 Sensitivity variation with displacement

Table 11, Table 12, and Table 13 contain the simulated and calculated values for each simulation positioning variant.

Table 11 Full scale options for 3.3 V supply; no displacement

Sensitivity range	Value (mV/mT)	Output voltage (mV/A)	Maximum current for FS (A)	Power dissipation at I_{RMS} (W)
B_FS1 = 24 mT	56.00	7.10	189.20	13.23
B_FS2 = 15 mT	90.00	11.41	117.72	5.12
B_FS3 = 12 mT	112.50	14.26	94.18	3.28
B_FS4 = 8 mT	180.00	22.82	58.86	1.28
B_FS5 = 6 mT	225.00	28.53	47.09	0.82
B_FS6 = 4 mT	360.00	45.65	29.43	0.32

Table 12 Full scale options for 3.3V supply; 0.5 mm displacement

Sensitivity range	Value (mV/mT)	Output voltage (mV/A)	Maximum current for FS (A)	Power dissipation at I_{RMS} (W)
B_FS1 = 24 mT	56.00	6.61	203.30	15.27
B_FS2 = 15 mT	90.00	10.62	126.50	5.91
B_FS3 = 12 mT	112.50	13.27	101.20	3.78
B_FS4 = 8 mT	180.00	21.24	63.25	1.48
B_FS5 = 6 mT	225.00	26.55	50.60	0.95
B_FS6 = 4 mT	360.00	42.48	31.62	0.37

Table 13 Full scale options for 3.3 V supply; 1 mm displacement

Sensitivity range	Value (mV/mT)	Output voltage (mV/A)	Maximum current for FS (A)	Power dissipation at I_{RMS} (W)
B_FS1 = 24 mT	56.00	5.32	252.68	23.59
B_FS2 = 15 mT	90.00	8.54	157.22	9.13
B_FS3 = 12 mT	112.50	10.68	125.78	5.85
B_FS4 = 8 mT	180.00	17.09	78.61	2.28
B_FS5 = 6 mT	225.00	21.36	62.89	1.46
B_FS6 = 4 mT	360.00	34.18	39.31	0.57

In frequency, observe how the amplification decreases with displacement at 1 MHz, it can be concluded that f_{-3dB} is increasing with displacement. Therefore, the bandwidth is higher at bigger values of displacement.

Table 14 System amplitude at 1 MHz

	No displacement	0.5 mm displacement	1 mm displacement
System amplitude at 1 MHz	–4.06 dB	–3.88 dB	–3.35 dB

4.2 Rules of thumb for layout design

In 3-phase systems:

- Position the traces as far as possible to minimize crosstalk between phases
- Strive for symmetry:
  - Route the sensors output traces symmetrically, ensuring equal trace lengths, an identical number of vias, and avoiding crossings over power paths
  - Design current rails to be identical and symmetrical relative to one another

Other

- Place the application PCB as far as possible from potential stray field generators, such as motors, chokes, inductors, and high-current conductors
- Keep forward and return current paths tightly coupled, particularly in areas away from the sensing region
- Avoid large copper pours or ground/supply planes near sensing traces to reduce the risk of eddy current interference
- If additional PCB space is available, oversize the length of the current-carrying trace to improve heat dissipation
- Place VDD decoupling capacitors as close as possible to the sensor to ensure stable power supply operation

Power conductors can be routed with sufficient spatial separation from magnetic sensors to minimize electromagnetic coupling. Avoid placing power wiring within the immediate sensing vicinity.

Position connectors at a minimum edge-to-edge distance of 15 mm from any sensor element, considering manufacturing and assembly tolerances. If it is not possible to meet the 15 mm separation requirement, ensure that connectors and adjacent hardware are made from non-ferromagnetic materials (with a relative permeability close to 1) to avoid field distortion and systematic hysteresis errors in the measurement chain.

4.3 Layout review checklist

For the XENSIV™ TLx5572 TMR-based current sensor, verify the following during the layout review:

- **Application circuit compliance:** Verify that the application circuit is implemented as recommended in the design documentation
- **Trace/busbar design:** Confirm that the trace or busbar geometry in the layout matches the dimensions and design parameters established through simulation
- **Proximity check for stray field sources:**
  - Inspect PCB-level proximity for potential stray field sources such as magnetic components for stray field sources at PCB level
  - Identify components like connectors with ferromagnetic particles, inductors, and transformers that are placed near the sensor. Move these components to a safe distance. If moving them is not feasible, perform a magnetic simulation to evaluate and mitigate their impact
- **Coupling checks:**
  - Ensure signal traces and power lines do not overlap to minimize unwanted electromagnetic coupling effects
  - Avoid power traces or planes directly underneath the sensor area. If unavoidable, create cut-outs directly under the sensor package, or at minimum, under the sensing element location. See Figure 3
  - Keep forward and return current paths tightly coupled and routed away from the sensing region to minimize interference
- **Symmetry checks for 3-phase systems:**
  - Route the output lines of the sensors symmetrically to the microcontroller, ensuring consistency in terms of the number of vias, trace lengths, and proximity to power rails
  - Design the current rails symmetrically (ideally identical), following the layout established during simulation for optimal balance

5 Related resources

- XENSIV™ current sensor family webpage
- XENSIV™ current sensors developer community
- XENSIV™ Current Sensor Simulation Tool

References

[1] Infineon Technologies AG: *XENSIV™ TLx5572 current sensors datasheet;* Available online

[2] Infineon Technologies AG: *XENSIV™ TLE4972, TLE4973 current sensors sensing structure design application note;* Available online

[3] Infineon Technologies AG: *XENSIV™ TLx5572 current sensors application note;* Available soon

Glossary

EMI
electromagnetic interference (EMI)

eCR
external current rail (eCR)

FS
full scale (FS)

iCR
internal current rail (iCR)

SNR
signal-to-noise ratio (SNR)

Revision history

Document revision	Date	Description of changes
1.00	2026-07-01	Initial release

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