AN1160

HOTLink® CY7B923/CY7B933 to HOTLink II™ Migration

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Associated Part Family: HOTLink IITM PHYs

Related Application Notes: AN014

This application note discusses how to migrate from HOTLink-based designs to HOTLink II™-based designs.

1 Introduction

HOTLink is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links (fiber, coax, twisted pair, and PCB trace). HOTLink II family devices are the second generation of HOTLink technology that offers enhanced levels of integration and faster data rates, while maintaining serial-link compatibility with HOTLink devices. HOTLink II also gives you the flexibility to have multiple channels on a single chip, thereby saving board space while increasing the data throughput.

This application note discusses how to migrate from HOTLink-based designs to HOTLink II-based designs. While most designs can be converted from HOTLink to HOTLink II, applications that use the device at signaling rates of less than 200 MBaud cannot be migrated. The scope of this application note is limited to device configuration, although some information on device operation is covered as necessary. The Quad HOTLink II Transceiver (CYP15G0401DXB) is used to illustrate how to migrate your design; one of the channels is used to show how to interface the HOTLink device to HOTLink II devices. A comparison of some of the features of HOTLink and HOTLink II are listed in Table 1.

2 HOTLink Device Configuration

2.1 Transmitter Configuration

2.1.1 Input Register[1]

The input register holds the data to be processed by the HOTLink transmitter. The CY7B923 input register is clocked by the CKW signal and loaded with the information on the D_{0-7}, SC/$\overline{D}$, and SVS pins. The HOTLink II input register supports different bit assignments based on whether the character is unencoded, encoded with two control bits, or encoded with three control bits. Table 2 lists HOTLink II input register bit assignments. These assignments are controlled by the TXMODE[1:0] 3-level select inputs[2], which allow one of the nine transmit modes to be chosen. The closest transmit modes to those supported by CY7B923 are the TX Mode 5 or TX Mode 8. In these modes, HOTLink II uses the encoded bit assignment without the SCSEL control input.

[1] CYP15G0402DXB supports the 10-bit unencoded mode only (encoder is bypassed), thus TXMODE[1:0] inputs are not available. CYP15G0403DXB supports only encoder-enabled or encoder-disabled mode, as controlled by the ENCBYP signal. Therefore, TXMODE and SCSEL signals are not available.

[2] 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of nonstandard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by a direct connection to V_{SS} (ground). The HIGH level is usually implemented by a direct connection to V_{CC}. When not connected or allowed to float, a 3-Level select input will self-bias to the MID level.

Table 1. HOTLink and HOTLink II Features Comparison[3]

HOTLink	HOTLink II
CY7B923 HOTLink Transmitter CY7B933 HOTLink Receiver	CYP15G0401DXB: Quad HOTLink II Transceiver CYP15G0201DXB: Dual HOTLink II Transceiver CYP15G0101DXB: Single HOTLink II Transceiver CYP15G0402DXB: Dual HOTLink II SERDES [4] CYP15G0403DXB: Quad HOTLink II Transceiver with Independent clocking
150 to 400 MBaud serial signaling rate	200 to 1500 MBaud serial signaling rate
Fibre Channel, ESCON®, DVB-ASI, and ATM compliant	Fibre Channel, Gigabit Ethernet, ESCON, FICON®, DVB-ASI, SMPTE-259M, SMPTE-292M, and ATM compliant
Synchronous TTL parallel I/O	Synchronous LVTTL parallel I/O
Not available	Selectable parity check/generate
Not available	Selectable multichannel bonding options
Not available	Selectable input/output clocking options
Not available	Per-channel Link Quality Indicator
Dual differential PECL-compatible serial inputs; external DC-restoration required	Dual differential PECL-compatible serial inputs per channel with internal DC-restoration
Triple differential PECL serial outputs; external bias resistors required	Dual differential PECL-compatible serial outputs per channel. No external bias resistors required and source matched to 50-Ω transmission lines
Single +5 V supply	Single +3.3 V supply

Table 2. HOTLink II Input Register Bit Assignments

Signal Name	Unencoded	Encoded	
		2-bit Control	3-bit Control
TXDx[0] (LSb)	DINx[0]	TXDx[0]	TXDx[0]
TXDx[1]	DINx[1]	TXDx[1]	TXDx[1]
TXDx[2]	DINx[2]	TXDx[2]	TXDx[2]
TXDx[3]	DINx[3]	TXDx[3]	TXDx[3]
TXDx[4]	DINx[4]	TXDx[4]	TXDx[4]
TXDx[5]	DINx[5]	TXDx[5]	TXDx[5]
TXDx[6]	DINx[6]	TXDx[6]	TXDx[6]
TXDx[7]	DINx[7]	TXDx[7]	TXDx[7]
TXCTx[0]	DINx[8]	TXCTx[0]	TXCTx[0]
TXCTx[1] (MSb)	DINx[9]	TXCTx[1]	TXCTx[1]
SCSEL	N/A	N/A	SCSEL

[3] The features listed in this table might not be available in all HOTLink II family devices. See each product data sheet for complete specifications.

[4] This device is obsolete.

Unlike the CY7B923 input register that can only be clocked synchronously to its reference clock, the input register on HOTLink II can be operated synchronously (TXCKSEL[5] = LOW) or asynchronously (TXCKSEL = MID or HIGH). When TXCKSEL = MID, the input register of each channel is clocked by its respective TXCLKx↑. When TXCKSEL = HIGH, TXCKLA↑ is used to clock the data into the input register for all channels.

2.1.2 Phase-Align Buffer

When the input registers are operated synchronously to the REFCLK (TXCKSEL = LOW), phase-align buffers are bypassed. When TXCKSEL ≠ LOW, phase-align buffers are used to absorb clock phase differences between the presently selected input clock and the internal character clock. Initialization of these phase-align buffers takes place when the $\overline{\text{TXRST}}$ input is sampled LOW by TXCLKA↑. Because CY7B923 operates only synchronously to its reference clock, it does not have a phase-align buffer.

2.1.3 Parity Support[6]

HOTLink II supports ODD parity checking while CY7B923 does not. Parity checking is controlled by the PARCTL input and can be set LOW to disable this feature. When parity checking is disabled, TXOPx inputs are ignored. If parity checking is enabled, TXPERx is asserted (HIGH) when a parity error is detected at the encoder.

2.1.4 Encoder[7]

When the encoder is enabled, characters to be transmitted are converted from data or special character codes to 10-bit transmission characters. CY7B923 uses two enable inputs ($\overline{\text{ENA}}$ and $\overline{\text{ENN}}$) to choose when the data is loaded into the input register. The SC/D input controls whether to encode a data or a special character. SVS can be used to send a violation code (C0.7).

In HOTLink II, TXCTx[1:0] and SCSEL are interpreted along with the associated TXDx[7:0] character to generate the specific 10-bit transmission character. In TX Mode 5 or TX Mode 8, however, SCSEL is not used. In these modes, TXCTx[1] can be used as the SC/D input and TXCTx[0] can be used as the $\overline{\text{ENA}}$ input. In some applications, the $\overline{\text{ENA}}$ input is sometimes set LOW permanently. This allows an even simpler configuration where TXCTx[0] can be connected to GND and TXCTx[1] used to select between encoding a data or a special character. HOTLink II does not have the Enable Next Parallel Data ($\overline{\text{ENN}}$ and the Send Violation Symbol (SVS) functions. A violation code can be sent by supplying a C0.7 data byte in the data bus and encoding it as a special character. Table 3 lists how the control signal interprets the data bits and what characters are generated by them.

Table 3. TX Mode Encoding Comparison

TXCTx[1]	TXCTx[0]	Characters Generated
0	0	Encoded data character
0	1	K28.5 fill character
1	0	Special character code
1	1	16-character Word Sync Sequence

Care needs to be taken when TXCTx[0] is used to replace $\overline{\text{ENA}}$. When TXCTx[1:0] = 11, a 16-character sequence of K28.5 characters, known as a Word Sync Sequence, is generated on the associated channel. When TX Mode 5 is selected, this character sequence cannot be stopped until all 16 characters have been generated. The content of the associated input registers is ignored for the duration of this 16-character sequence. When TX Mode 8 is selected, TXCTx[1:0] inputs must be sampled as '00' for the remaining 15 characters of the sequence. If, at any time a sample period exists where TXCTx[1:0] ≠ 00 is sampled after the Word Sync Sequence has started, the Word Sync Sequence is terminated, and a character representing the associated data and control bits is generated by the encoder.

[5] CYP15G0403DXB uses addressable latches for configuration. Therefore, logic mapping of the control signals may be different from that shown here. See the CYP15G0403DXB datasheet for details.

[6] Parity support is not available in CYP15G0403DXB.

[7] CYP15G0402DXB supports the 10-bit unencoded mode only (encoder is bypassed), thus TXMODE[1:0] inputs are not available. CYP15G0403DXB supports only encoder-enabled or encoder-disabled mode as controlled by the ENCBYP signal. Therefore, TXMODE and SCSEL are not available.

2.1.5 Transmit Modes[8, 9]

The operating mode of the HOTLink II transmit path is set through the TXMODE[1:0] inputs. These 3-level select inputs allow one of the nine transmit modes to be selected. CY7B923 selects the transmit modes through the MODE input. Table 4 lists comparable settings between the MODE pin in CY7B923 and TXMODE[1:0] in CYP15G0401DXB.

Table 4. Transmit Operating Modes

CY7B923	HOTLink II	Transmit Mode
MODE = L	TXMODE[1:0] = HH (TXMODE 8)	Encoder is enabled
MODE = H	TXMODE[1:0] = LL (TXMODE 0)	Encoder is bypassed

2.1.6 Serial Output Drivers

CY7B923 has three differential PECL serial outputs. Two of the serial outputs can be disabled by setting the FOTO input to HIGH. HOTLink II has two high-performance differential Current Mode Logic (CM) serial outputs to provide source-matched drivers for the transmission lines. Each serial driver can be enabled or disabled separately through the BOE[x] inputs, as controlled by the OELE latch-enabled signal.

2.1.7 Transmit PLL Clock Multiplier

CY7B923 takes a byte-rate reference clock, which is CKW, and multiplies it by 10 to create a bit-rate clock for driving the serial shifter. HOTLink II accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiplies that clock by 10 or 20 (as selected by TXRATE) to generate a bit-rate clock for use by the Transmit Shifter. Because CY7B923 operates up to a 400-MBaud signaling rate, both TXRATE and SPDSEL should be set LOW for HOTLink II to operate in this range and the REFCLK frequency should be between 20 MHz and 40 MHz. HOTLink II does not operate below a 200-MBaud signaling rate.

2.1.8 Built-In-Self-Test (BIST)

BIST can be used to validate both device and link operation. In CY7B923, the BIST function is enabled when $\overline{\text{BISTEN}}$ is LOW and either $\overline{\text{ENA}}$ or $\overline{\text{ENN}}$ is set LOW. When BIST is enabled, $\overline{\text{RP}}$ remains HIGH for all but the last byte of a test loop. $\overline{\text{RP}}$ pulses LOW one byte time per BIST loop.

In HOTLink II, BISTLE and BOE[x] inputs control enabling/disabling the BIST function. When BIST is enabled, BIST progress is presented on TXPERx outputs. After every BIST loop, the associated TXPERx signal will pulse HIGH for one transmit-character clock period to indicate a complete pass through the BIST sequence. When receive channels are clocked by a common clock (RXCKSEL ≠ MID), TXPERx pulses HIGH for 17 transmit-character clock periods.

2.2 Receiver Configuration

2.2.1 Serial Data Input

Both CY7B933 and each channel of the HOTLink II device have two pairs of differential line receivers that are selectable using the associated A/$\overline{\text{B}}$ input in CY7B933 or INSELx input in the HOTLink II device. Each serial input on the HOTLink II device provides internal DC restoration to the center of the receiver's common-mode range. Each receive channel of the HOTLink II device can be independently enabled and disabled through the BOE[7:0] inputs, as controlled by the RXLE[10] latch-enable signal.

HOTLink II also has a local loopback input (LPEN) that allows the serial transmit data to be routed internally back to the Clock and Data Recovery circuit associated with each channel. When LPEN is set LOW, the local loopback mode is disabled.

[8] CYP15G0402DXB supports the 10-bit unencoded mode only (encoder is bypassed), thus TXMODE[1:0] inputs are not available. CYP15G0403DXB supports only encoder-enabled or encoder-disabled mode as controlled by the ENCBYP signal. Therefore, TXMODE and SCSEL are not available.

[9] CYP15G0403DXB uses addressable latches for configuration. Therefore, the logic mapping of the control signals may be different from that shown here. See the CYP15G0403DXB datasheet for details.

[10] 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC}. When not connected or allowed to float, a 3-Level select input will self-bias to the MID level.

2.2.2 Signal Detect/Link Fault

The HOTLink II device uses the SDASEL input to set the trip point to detect a valid signal level. When SDASEL is set LOW, the valid signal level is set to 140-mV (p-p) differential, which is the closest valid signal level that HOTLink I can detect.

Each selected line-receiver is also simultaneously monitored to make sure that the received data stream has sufficient transition density and falls within the normal frequency range (±200 ppm). The status is presented on the $\overline{\text{LFIx}}$ (Link Fault Indicator) output associated with each receive channel. If one of the requirements is violated or the receiver is disabled, $\overline{\text{LFIx}}$ is asserted (LOW) to indicate that invalid signals are present. These functions are not available in CY7B933.

2.2.3 Clock and Data Recovery

The HOTLink II extraction of a bit-rate clock and recovery of data bits from each received serial stream is performed by a separate Clock/Data Recovery (CDR) block within each receive channel. The clock extraction function is performed by embedded PLLs that track the frequency of transitions in incoming bit streams and align the phase of their internal bit-rate clocks to transitions in selected serial data streams.

Each HOTLink II CDR accepts not only a full-character-rate (bit-rate ÷ 10) but also a half-character-rate (bit-rate ÷ 20) reference clock from the REFCLK input. This REFCLK input is used to ensure that the VCO is operating at the correct frequency, to improve PLL acquisition time, and to limit the unlocked frequency excursions when there is no input data present at the selected serial line receiver. Thus, setting RXRATE = LOW resembles CY7B933 that only accepts a full-character-rate reference clock from the REFCLK input.

2.2.4 Deserializer/Framer

Each CDR circuit extracts bits from the associated serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the framer logic checks the incoming bit stream for a unique pattern that defines the character boundaries. CY7B933 uses the K28.5 special character as a framing character, while HOTLink II allows selection of one of the three combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input. When FRAMCHAR is set HIGH, the framer logic selects K28.5 as its framing characters. The Framer on each HOTLink II channel operates in one of the three different modes as selected by the RFMODE[11] input. When RFMODE = LOW, the Low-Latency Framer is selected, which is similar to asserting the RF input in CY7B933 when framing is desired. When RFMODE = MID (open), the Cypress-mode Multi-Byte[12] Framing is selected. In CY7B933, this can be done by asserting the RF input HIGH for greater than 2048 clock cycles. The Alternate-mode Multi-Byte[12] Framing (RFMODE = HIGH) is not available in CY7B933. In addition, the HOTLink II Framer itself may be enabled or disabled through the RFEN input.

2.2.5 Decoder

The framed parallel output of each Deserializer Shifter is passed to the 10B/8B Decoder where, if the Decoder is enabled (DECMODE[11, 13] ≠ LOW in HOTLink II), it is transformed from a 10-bit transmission character back to the original data and special character codes. Table 5 lists the equivalent decoder configuration of CY7B933 and the HOTLink II device. When operating in channel bonding mode, the decoder must be enabled.

Table 5. Decoder Configuration

MODE (CY7B933)	DECMODE (HOTLink II)	Descriptions
HIGH	LOW	Decoder is bypassed
LOW	MID	Cypress decoder is enabled
N/A	HIGH	Alternate decoder is enabled

[11] CYP15G0403DXB uses addressable latches for configuration. Therefore, the logic mapping of the control signals may be different from that shown here. See the CYP15G0403DXB datasheet for details

[12] In Cypress-mode Multi-Byte framing, the framer logic requires a minimum of two K28.5 characters aligned on the same character boundary within a 5-character window to reframe.

[13] DECMODE, RXCKSEL, RXMODE[1:0], and Elasticity Buffer are not available in CYP15G0402DXB. RXSTx[2:0] outputs are replaced by COMDETx.

2.2.6 Elasticity Buffer[13]

Each receive channel in HOTLink II contains an Elasticity Buffer that is designed to support multiple clocking modes. These buffers allow data to be read using an Elasticity Buffer read clock that is asynchronous in both frequency and phase from the Elasticity Buffer write clock, or to use a read clock that is frequency-coherent but with an uncontrolled phase relative to the Elasticity Buffer write clock. These buffers are also used to align output data streams when multiple channels are bonded together.

CY7B933 does not have this feature and the receive path can only operate by using the recovered clock from received data streams. CKR outputs the character rate clock that is phase- and frequency-aligned to the incoming serial data stream. Likewise, when RXCKSEL[11, 13] in HOTLink II is set to MID (open), Elasticity Buffers are bypassed and the recovered clock for the respective channel is used to transfer data to output registers. In this mode, each RXCLKx± output follows the recovered clock for the respective channel, as selected by RXRATE.

2.2.7 Receive Modes and Channel Bonding

The operating mode of the receive path is set through the RXMODE[1:0][14, 15] inputs. These RXMODE[1:0] inputs are only interpreted when the decoder is enabled (DECMODE ≠ LOW). These modes determine the type (if any) of channel bonding and status reporting. See application note, AN014 - Channel Bonding with HOTLink II Transceiver for more information on channel bonding.

HOTLink II uses three bits (RXSTx[2:0]) for status reporting, whereas CY7B933 uses only two bits (RVS and SC/$\overline{D}$). While some information may be lost, RXSTx[0] can be mapped as SC/$\overline{D}$, and RXSTx[2] can be used to report error or violation events (RVS in CY7B933).

2.2.8 Output Register

CY7B933 presents an 11-signal output bus consisting of an 8-bit data bus ($Q_{0–7}$), a 2-bit status bus (SC/$\overline{D}$ and RVS), and a data output ready indicator ($\overline{RDY}$). In the encoder bypass mode, SC/$\overline{D}$, $D_{0–7}$, and RVS become D_a, D_{b-h}, and D_j respectively. On the other hand, each receive channel of HOTLink II presents a 12-signal output bus consisting of an 8-bit data bus (RXDx[7:0]), a 3-bit status bus (RXSTx[2:0]), and a parity bit (RXOPx). These bits are assigned as per Table 6.

Table 6. Output Register Bit Assignments[16]

Signal Name	DECMODE = LOW	DECMODE = MID or HIGH
RXSTx[2] (LSb)	COMDETx	RXSTx[2]
RXSTx[1]	DOUTx[0]	RXSTx[1]
RXSTx[0]	DOUTx[1]	RXSTx[0]
RXDx[0]	DOUTx[2]	RXDx[0]
RXDx[1]	DOUTx[3]	RXDx[1]
RXDx[2]	DOUTx[4]	RXDx[2]
RXDx[3]	DOUTx[5]	RXDx[3]
RXDx[4]	DOUTx[6]	RXDx[4]
RXDx[5]	DOUTx[7]	RXDx[5]
RXDx[6]	DOUTx[8]	RXDx[6]
RXDx[7] (MSb)	DOUTx[9]	RXDx[7]

[14] CYP15G0403DXB uses addressable latches for configuration. Therefore, the logic mapping of the control signals may be different from that shown here. See the CYP15G0403DXB datasheet for details.

[15] CYP15G0101DXB only has a single RXMODE pin to select between Receiver Character Status A or Status B.

[16] RXOPx outputs are also driven from the associated Output Register, but their interpretation is under the separate control of PARCTL.

2.2.9 Parity Generation[17]

HOTLink II supports ODD parity generation for each channel and the parity bit is presented at the RXOPx output. Parity generation is enabled through the PARCTL input. When PARCTL = LOW, parity checking is disabled, and the RXOPx outputs are all disabled. CY7B933 does not have parity support.

2.2.10 Built-In Self-Test (BIST)

BIST can be used to validate both device and link operation. In CY7B933, the BIST function is enabled when $\overline{\text{BISTEN}}$ is LOW, and $\overline{\text{RDY}}$ pulses HIGH for one character time per BIST loop. In HOTLink II, BISTLE and BOE[x] inputs control enabling/disabling the BIST function. RXSTx[2:0] outputs become the Receive BIST Status. When RXSTx[2] is HIGH, it indicates that the receiver has either not started comparing characters, or has not found the start-of-BIST character, or has found a mismatch in one or more of the decoded character bits. When RXSTx[2] = LOW and RXSTx[1] = HIGH, status bits indicate that the last character of the BIST sequence has been detected and is valid.

3 Interfacing CY7B923/CY7B933 to CYP15G0401DXB

HOTLink II devices, even though much more complex, can be configured in such a way as to operate like a CY7B923/CY7B933 device. The amount of external components required for the line interfaces is also reduced. Figure 1 shows an example of CYP15G0401DXB when configured similar to CY7B923/CY7B933 and illustrates how to design the line interfaces between CY7B923/CY7B933 and CYP15G0401DXB.

3.1 Device Configuration

CY7B923 is configured to operate in the encoded mode (MODE = LOW). A 20-MHz clock is used to create a 200-MBaud signaling rate. $\overline{\text{ENN}}$ is set HIGH and $\overline{\text{ENA}}$ is connected to GND to always enable the inputs bus. $\overline{\text{BISTEN}}$ is set HIGH to disable the BIST pattern generator. FOTO is connected to GND to always enable the serial outputs.

CY7B933 is also configured to operate in the encoded mode (MODE = LOW) with a 20-MHz clock used as an input to the REFCLK pin. RF is permanently set HIGH to enable multibyte framing. $\overline{\text{BISTEN}}$ is set HIGH to disable the BIST function. Table 7 lists the comparable HOTLink II pin configurations and provides an explanation of each pin's function.

3.2 Line Interface

The open-emitter structure of the CY7B923 PECL output can source current but cannot sink current. To allow the output to switch, some form of pull-down is required on the output. This pull-down usually takes the form of a resistive load; either to V_{EE} or V_{CC} – 2 V. The CYP15G0401DXB CML output driver construction does not require the pull-down resistor.

CYP15G0401DXB uses a 3.3-V power supply while CY7B923/CY7B933 uses a 5.0-V power supply. For configurations where different power supplies are used, some form of AC coupling becomes necessary. This can be performed with DC-blocking capacitors (or transformers). Because the line interfaces are AC-coupled, a DC-restoration network is required at the input of CY7B933. A termination network is also required at the input of CY7B933.

On the other hand, CYP15G0401DXB serial input has internal DC restoration, thus the only external components needed at the receiver are the termination resistor that is placed across the differential line, and the capacitors or transformers to AC-couple the line. Similar line interfaces can be used when interfacing CY7B923/CY7B933 to the remainder of HOTLink II family devices.

[17] Parity support is not available in CYP15G0403DXB.

4 Summary

The migration process from a HOTLink-based design to a HOTLink II-based design, as discussed above, is fairly simple. HOTLink II provides you with additional features and adds flexibility to have multiple channels on a single chip. The HOTLink II device configuration discussed in this application note is only one among other configurations that can be used. You should carefully choose the configuration that best suits your application needs. This application note can be used as both a reference and a guide to migrate your design.

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A Appendix

Figure 1. CY7B923/CY7B933 to CYP15G0401DXB Connections Schematic

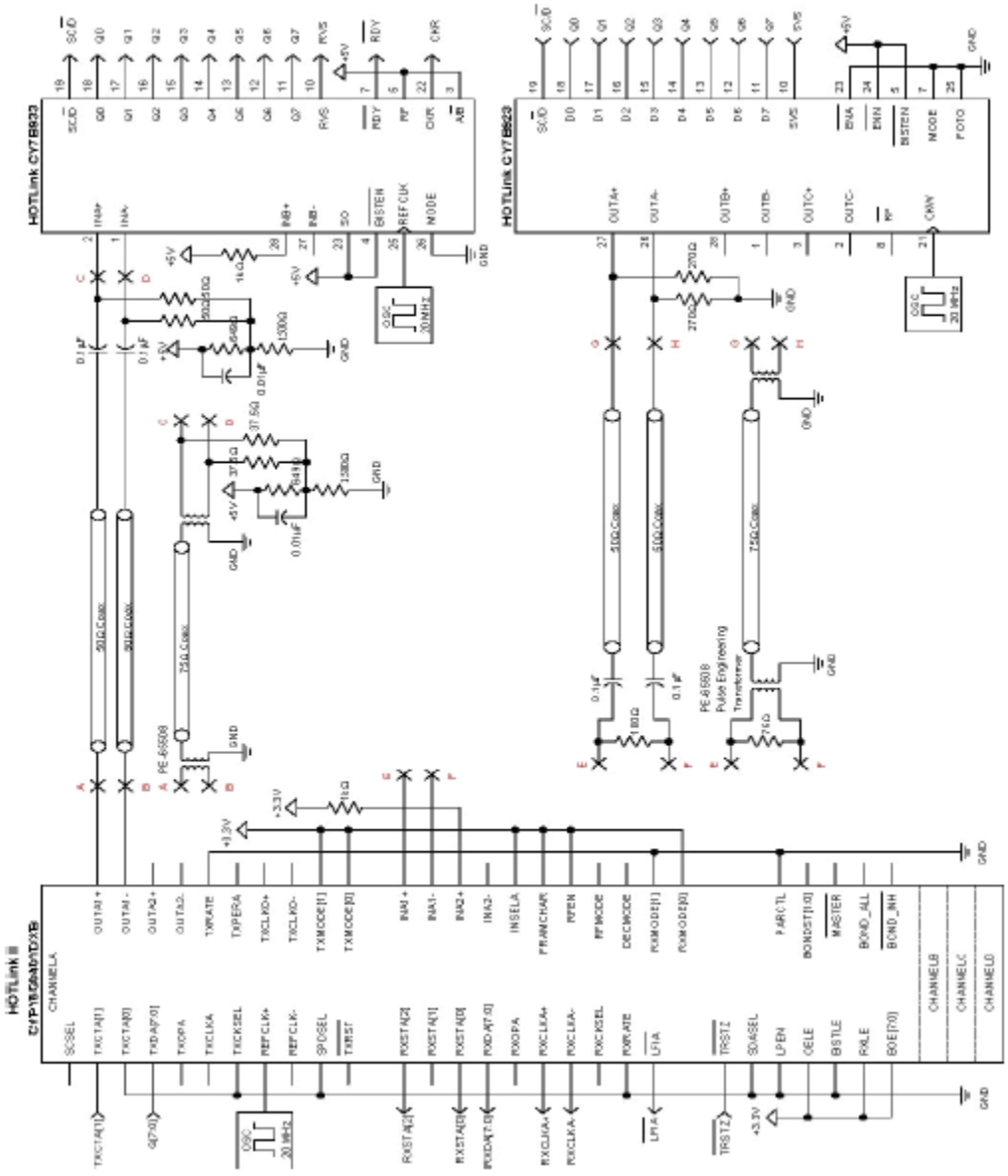

Table 7. CYP15G0401DXB Configuration

Signal Name	Type	Configuration	Function
TXPERx	LVTTL OUT	N/C	Optional output
TXCTx[1]	LVTTL IN	TXCTx[1]	Select between sending the encoded data or a K28.5 character
TXCTx[0]	LVTTL IN	LOW	Use TXCTx[1] only, as a transmit control signal
TXDx[7:0]	LVTTL IN	TXDx[7:0]	TX parallel data input
TXOPx	LVTTL IN	N/C	Not used when PARCTL = LOW
TXRST	LVTTL IN	N/C	Not used when TXCKSEL = LOW
SCSEL	LVTTL IN	N/C	Not used in TXMODE 8
TXCKSEL	3-Level Select IN	LOW	Use REFCLK to write data into the transmit input register
TXCLKO±	LVTTL OUT	N/C	Optional output
TXRATE	LVTTL IN	LOW	Use full-rate clock for the TX path
TXCLKx	LVTTL IN	N/C	Not used when TXCKSEL = LOW
TXMODE[1:0]	3-Level Select IN	HIGH, HIGH	Select TXMODE 8, Encoding Enabled (Interruptible)
RXDx[7:0]	LVTTL OUT	RXDx[7:0]	RX parallel data output
RXSTx[2:0]	LVTTL OUT	RXSTx[2:0]	RX status output
RXOPx	LVTTL OUT	N/C	Not used when the parity function is disabled
RXRATE	LVTTL IN	LOW	Use full-rate clock for the RX path
FRAMCHAR	3-Level Select IN	HIGH	Use the full K28.5 character as a framing character
RFEN	LVTTL IN	HIGH	Enable framing
RXMODE[1:0]	3-Level Select IN	LOW, HIGH	RX MODE 2, non-channel-bonding status B Mode
RXCLKx±	LVTTL OUT	RXCLKx±	RX clock output
RXCKSEL	3-Level Select IN	MID	Use recovered clock of the respective channel to transfer data to the receive output register
DECMODE	3-Level Select IN	MID	Use Cypress decoder table
RFMODE	3-Level Select IN	MID	Use multibyte framing
PARCTL	3-Level Select IN	LOW	Disable parity function
SPDSEL	3-Level Select IN	LOW	200–400 MBaud range is selected
REFCLK+[11]	LVTTL IN	REFCLK+	Reference clock 20 MHz
TRSTZ	LVPECL IN	TRSTZ	Device reset pin
OUTx1± OUTx2±	CML DIFF OUT	OUTx1± OUTx2±	Differential serial output
INx1± INx2±	LVPECL DIFF IN	INx1± INx2±	Differential serial input
INSELx	LVTTL IN	INSELx	Input select between INx1 or INx2
SDASEL	3-Level Select IN	LOW	Use 140-mV p-p differential to detect valid signal level
LPEN	LVTTL IN	LOW	Disable loop enable for normal operation
OELE	LVTTL IN	HIGH	TX channels latch enable
BISTLE	LVTTL IN	LOW	BIST latch enable

Signal Name	Type	Configuration	Function
RXLE	LVTTL IN	HIGH	RX channels latch enable
BOE[7:0]	LVTTL IN	HIGH	BOE, OELE, RXLE, BISTLE work together to turn ON/OFF the channels and BIST mode
LFIx	LVTTL OUT	LFIx	Link fault indicator (Optional output)
BONDST[1:0]	BIDIR	N/C	Not used in non-channel-bonding mode
MASTER	LVTTL IN	N/C	Not used in non-channel-bonding mode
BOND_ALL	BIDIR	N/C	Not used in non-channel-bonding mode
BOND_INH	LVTTL IN	N/C	Not used in non-channel-bonding mode

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**	1787906	SAAC	12/12/2007	New Spec
*A	3166071	SAAC	02/10/2011	Added abstract details. Added Document History Page. Updated as per template. No technical updates.
*B	4289782	YLIU	02/24/2014	Updated in new template. Completing Sunset Review.
*C	5284517	ELG	05/25/2016	Updated template

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