Optimization of output capacitors placement for best transient performance using TDA38640/641/740/725

40 A SVID/I2C synchronous buck regulator

About this document

Scope and purpose

This application note summarizes the placement of output capacitors and its impact to achieve the best transient performance using OptiMOS™ TDA38640 synchronous buck regulator targeted for CPU/SOC/AI applications. This document contains both theoretical and practical recommendations. This analysis is applicable to TDA38641/740/725 parts as well.

Intended audience

The intended audience for this document includes FAEs, customers, and application engineers who work on design and development of server boards related to Intel/AMD/custom ASIC/AI platforms point-of-load (POL) rails.

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1 Introduction

With the growing demand for easy-to-use and compact power solutions, there is a shift in the server industry to consider POLs for low-current rail (<35 A) applications in place of using two-phase multiphase solutions. This is further supported by the latest adoption of constant on-time (COT) architecture in POLs which provides the best transient performance critical for server applications. A quick introduction of the fast constant on-time (COT) control is available in Infineon's website [1].

The OptiMOS™ integrated point-of-load (iPOL) TDA38640 synchronous buck regulator is an easy-to-use, fully integrated and highly efficient 40 A synchronous buck regulator with both Intel SVID and I2C interfaces. The iPOL is optimized to convert a 12 V input supply to a voltage level required by high-performance microprocessors and DDR memory. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make the TDA38640 a small-footprint solution, providing highly efficient power delivery. The fast constant on-time (COT) control scheme simplifies design efforts and achieves fast control response. The device configuration can be easily defined using Infineon's XDP™ Designer GUI and is stored in the on-chip memory. XDP™ Designer can be downloaded from Infineon Developer Center launcher. Figure 1 shows the application circuit of TDA38640 synchronous buck regulator.

In general, POLs are expected to be placed at the point of the load. However, because of the increasing output power levels and higher slew rate requirements of the processors for the core rails, multiphase solutions take up more space and are placed closer to the CPU compared to other non-core rails regarding the board layout. These constraints have forced designers to place POL solutions 3 to 5 inches away from the load. This negatively impacts the load transient performance because of the parasitic impedances between the POL and the load.

This application note demonstrates and provides guidelines about placement of output capacitors to achieve the best transient results using the TDA38640 part to meet the Intel specifications. It uses Infineon-designed DB422 board based on Intel Birch Stream SP as a testing platform.

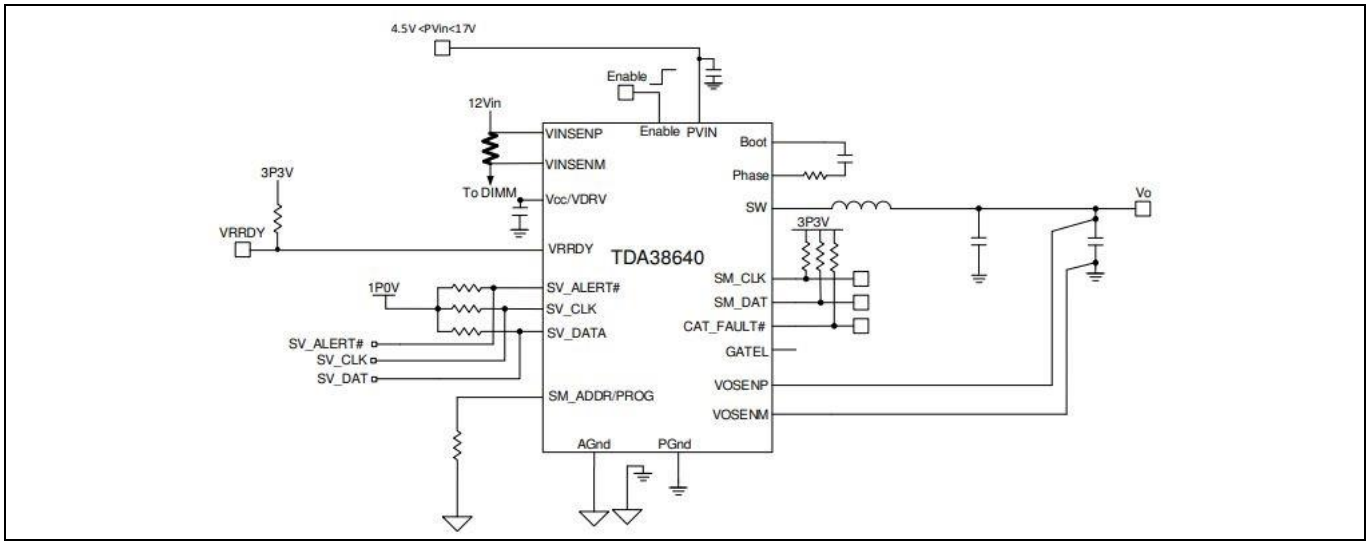

Figure 1 Application diagram of TDA38640

1.1 Features of TDA38640

- Single 5 V to 17 V application or wide input voltage range from 3.0 V to 17 V with external V_{cc}
- Output voltage range: 0.25 V to 3.04 V with external feedback resistor divider in SVID mode
- Enhanced fast COT engine stable with ceramic output capacitors and no external compensation
- Optional forced continuous conduction mode (CCM) and diode emulation for enhanced light load efficiency
- Programmable switching frequency from 400 kHz to 2 MHz in steps of 200 kHz, excluding 1600 kHz
- Monotonic startup with selectable soft-start time via SVID or PMBus commands and pre-bias startup
- Thermally compensated internal overcurrent protection with eight selectable settings
- I2C system interface for reporting of temperature, voltage, current, and power telemetry
- Single-image multiple-time programming (MTP) for the USER section
- Digitally programmable load-line without any external components
- 12 V input current sensing is supported without the need of an external interface circuit
- Operating temp: –40°C < T_j < 125°C
- Small size: 5 mm x 6 mm PQFN package
- Pb-free, Halogen-free, and RoHS2 compliant with exemption 7a

2 Load transient requirements

The VRs load transient requirements are very specific and vary from rail-to-rail and different CPUs/ASICs applications.

VRs providing power to these rails have to be designed to meet these transient specifications across a wide range of load repetitive frequencies in the range of 1 kHz to 1 MHz at different duty cycles in the range of 10% to 90%. VR alone cannot meet these transient requirements as the bandwidth of VR control loop is limited and usually around hundreds of kHz. This makes the role of output capacitors significant.

In general, different types of output capacitors are placed in parallel to these VRs. As the output characteristics of each type of capacitors frequency are different, the combination of various capacitors makes the output impedance minimum for a wide range of load repetitive frequencies that is a combination of MLCC and SP capacitors. The packages of these MLCC capacitors include 0805, 0603, and 0402 types. This combination of different types of capacitors on the output keeps the overall output impedance low in a frequency range of 1 kHz to 1 MHz to meet the transient specifications across a wider frequency range.

While selecting capacitors, consider the degradation of the output capacitance based on the DC bias characteristics of MLCC capacitors. In addition to the output capacitance, the PCB impedance affects the transient performance. This PCB impedance forms a secondary LC resonance from VR output to the actual load which negatively impact the transient performance.

A detailed analysis of impact of secondary LC filter on the transient performance has been presented in Section 3.

3 Secondary LC filter analysis

3.1 Literature study

This section provides a short literature background of IEEE paper "*Secondary LC filter analysis and design techniques for current-mode-controlled converters*" [2] that analyzes the impact of secondary LC filter for a buck converter. The point of interest for this application note would be the impact of secondary LC filter with respect to the capacitive loading. Two different capacitive loading conditions have been considered to understand the impact of secondary LC filter on the output impedance of the system. It analyzes the case of higher capacitance on the first stage LC filter and the other with higher capacitance on the output.

It states that the higher capacitance near the first stage LC filter would result in significant output impedance peaking at frequencies closer to the secondary filter resonance and recommends designing a system with higher capacitance at the second stage closer to the output. This reduction in impedance peaking with higher capacitance on output is attributed to the reduced quality factor providing damping to the secondary resonance.

3.2 Output impedance analysis

A typical buck converter output filter consists of the primary inductor (Lo) and primary capacitor (Co). Due to the parasitic inductor created by the long traces between the voltage regulator output and the actual load, there is a secondary inductor (Lo1). There is a secondary output capacitance (Co1) due to the capacitor bank close to the CPU/ASIC. There are two resonant frequencies formed by primary and secondary LC networks as shown in Figure 2. Assuming the main power inductor Lo >> Lo1 and setting the ESR of the capacitor to zero, Equation 1 for the primary resonant frequency and Equation 2 for the secondary resonant frequency is derived.

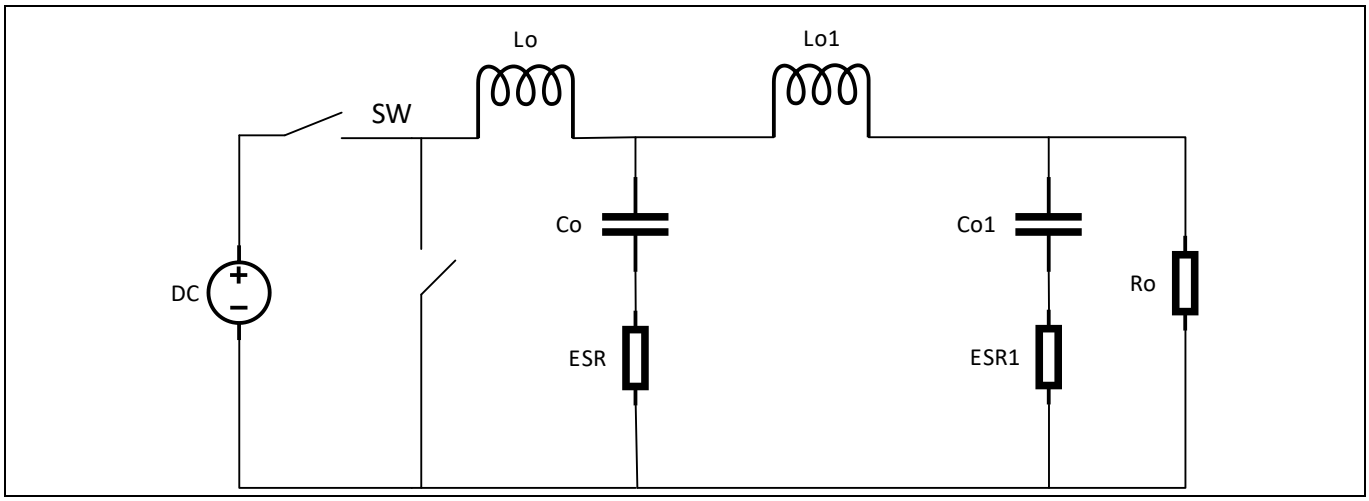

Figure 2 Buck converter with second LC filter

$$\omega p := \frac{1}{\sqrt{Lo \cdot (Co + Co1)}}$$

Equation 1 Primary resonant frequency

$$\omega s := \frac{1}{\sqrt{\left(Lo1 \cdot \frac{Co \cdot Co1}{Co + Co1}\right)}}$$

Equation 2 Secondary resonant frequency

3.3 High-frequency output impedance with Co>>Co1

The high-frequency output impedance of the secondary LC filter is shown in Equation 3. At high frequency, the primary inductor impedance is high and can be removed. The impact of the secondary LC filter is reflected in the second component of Equation 3 resulting in a third order system. The secondary resonance is dependent on Lo1 and Co1 values creating a dependency on the output capacitor loading.

$$Zos(s) := Ro \cdot \frac{(1 + Co \cdot ESR \cdot s)}{(1 + Co \cdot Ro \cdot s)} \cdot \frac{\left(1 + Lo1 \cdot \frac{s}{ESR1} + s \cdot Co1 \cdot (ESR + ESR1) + Lo1 \cdot Co1 \cdot s \cdot s\right)}{\left(1 + Lo1 \cdot \frac{s}{Ro} + s \cdot Co1 \cdot (ESR + ESR1) + Lo1 \cdot Co1 \cdot s \cdot s\right)}$$

Equation 3 High-frequency output impedance of secondary LC filter

Where,

Co = Capacitance close to the output VR

ESR = Primary capacitor ESR

Ro = Output load

Lo1 = secondary inductor

Co1 = Capacitor close to the load

ESR1 = Secondary capacitor ESR

Zp = High-frequency impedance of Co without secondary LC

Zs = High-frequency impedance of secondary LC filter

AR_i = Output impedance magnitude plot with PDN included in dB

Φ_i = Output impedance phase plot with PDN included in degrees

ARI_i = Output impedance magnitude plot with capacitors closer to the load in dB

ΦI_i = Output impedance phase plot with capacitors closer to the load in degrees

- When the capacitor of the secondary LC is much lower than the primary LC (Co >> Co1), output impedance peaking can occur at the secondary LC resonance. This is because of the second order filter impact created by secondary LC in the output impedance transfer function. This will affect the dynamic performance at high-frequency load repetition rate.

Secondary LC filter analysis

- The secondary filter LC resonance is sensitive to capacitive loading. Adding more capacitive load reduces the secondary resonance frequency, moving closer to the crossover frequency and can cause instability.
- The secondary LC filter also adds 180-degree phase shift. With Lo1 = 10 nH, Co= 496 µF, Co1 = 204 µF, the output impedance starts to peak in the range of 100–200 kHz.

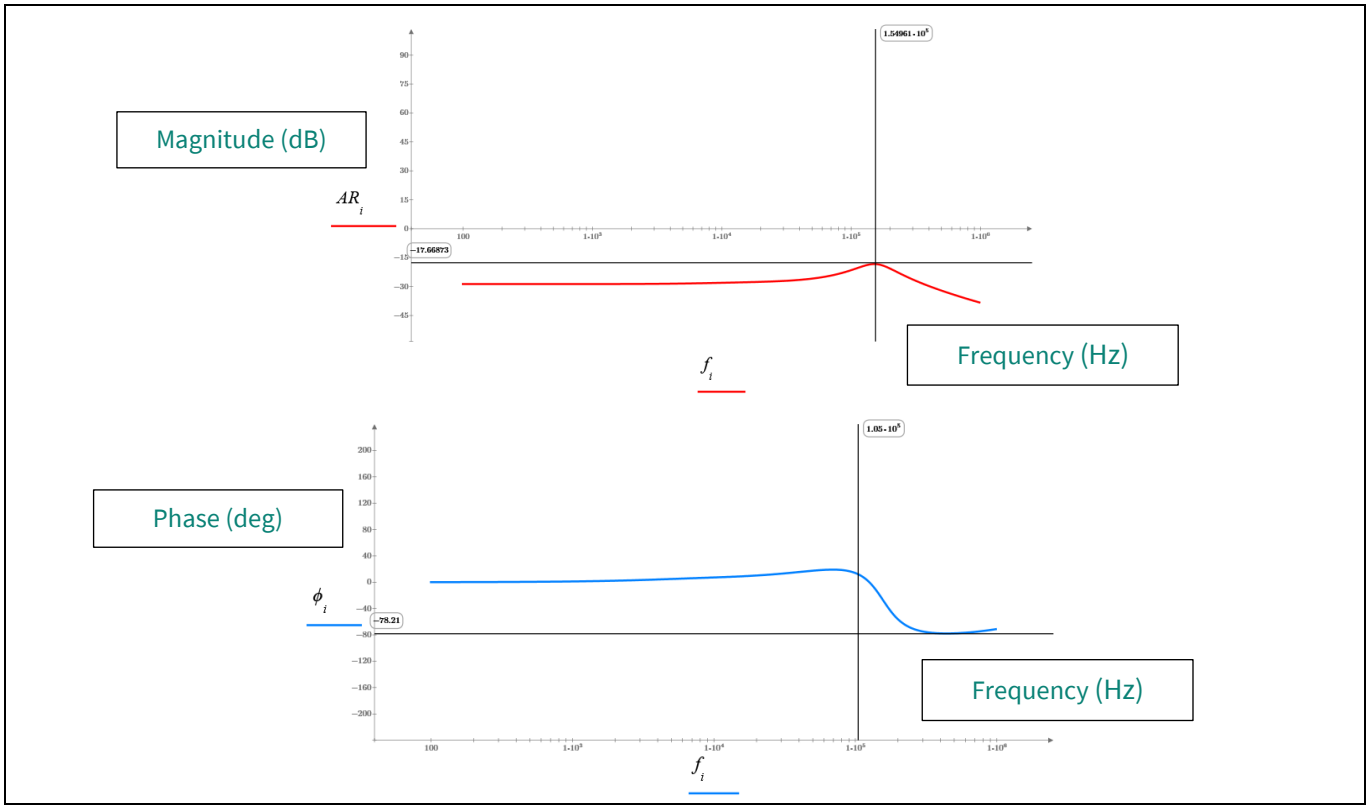

Figure 3 High-frequency output impedance of secondary LC filter with peak in the range of 100 kHz–200 kHz with Co>>Co1

3.4 High-frequency impedance with Co1>>Co

Equation 4 shows the high output impedance of the secondary LC with Co1>>Co.

$$Zo1(s) := Ro \cdot \frac{(1 + Co1 \cdot ESR1 \cdot s)}{(1 + Co1 \cdot Ro \cdot s)}$$

Equation 4 High output impedance of the secondary LC with Co1>>Co

The secondary LC does not affect the high-frequency output impedance in the case of Co1>>Co. This is the case with higher capacitance closer to the load than the VR. In other words, higher capacitance closer to the load will compensate the PDN impact effectively.

Secondary LC filter analysis

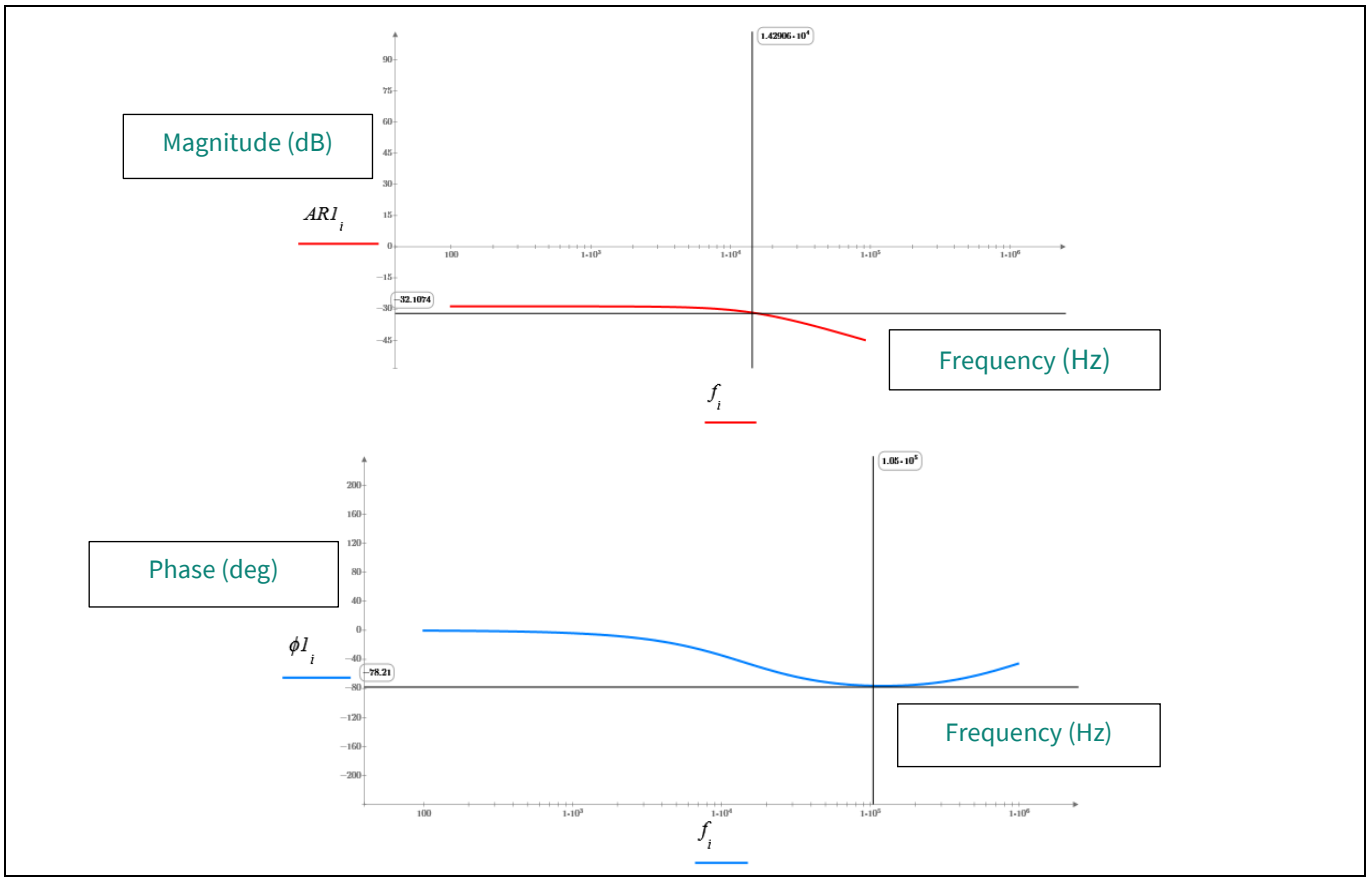

Figure 4 High-frequency impedance with Co1>>Co

4 Simulation and bench results with higher capacitance close to VR and actual load

This section demonstrates the SIMPLIS simulation and bench results of output voltage peak-peak variation during a transient event in two different cases. In the first case, a higher capacitance is used close to the VR and in the second case, a higher capacitance is used close to the load.

For obtaining the bench results, an Infineon-designed demo board DB422 is used. DB422 is designed for Birch Stream SP VR14 platform. An example of PVCCD_HV is considered for both simulation and bench testing.

4.1 Case 1: Higher capacitance close to VR

In this case, a 470 µF SP capacitor is placed close to the VR as shown in Figure 5 making Co >> Co1 as referred to Section 3.3.

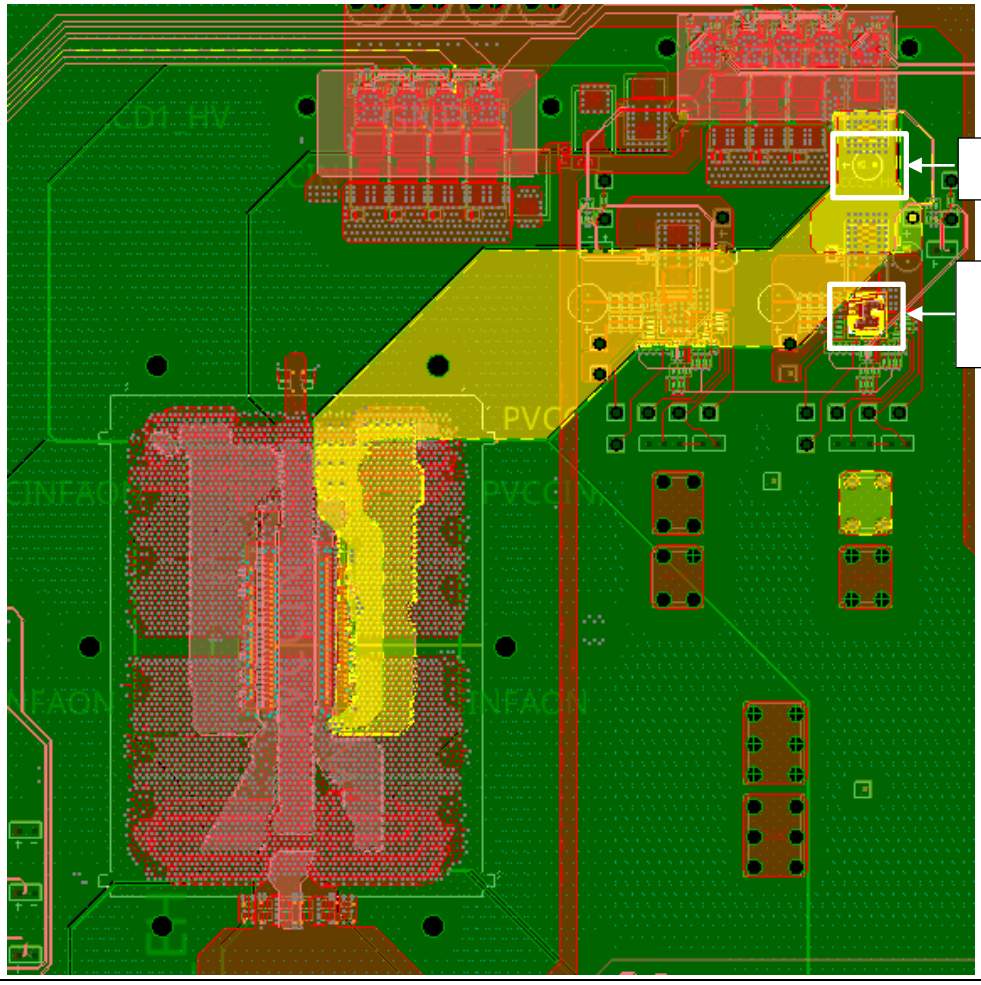

Figure 5 VR and SP capacitor placement on the test board for case 1

4.1.1 Case 1: Simulation analysis

Figure 6 shows the PDN network used for simulation. The parasitic inductances between different regions are extracted from DB422 layout and can be slightly different compared to the actual board parasitics. The output capacitors used are the same as used on the DB422 demo board. The ESR and ESL have been considered for all the MLCC and SP capacitors in the simulation based on the datasheet and capacitor manufacturer's design tools. DC bias characteristics are also considered for the MLCC capacitors.

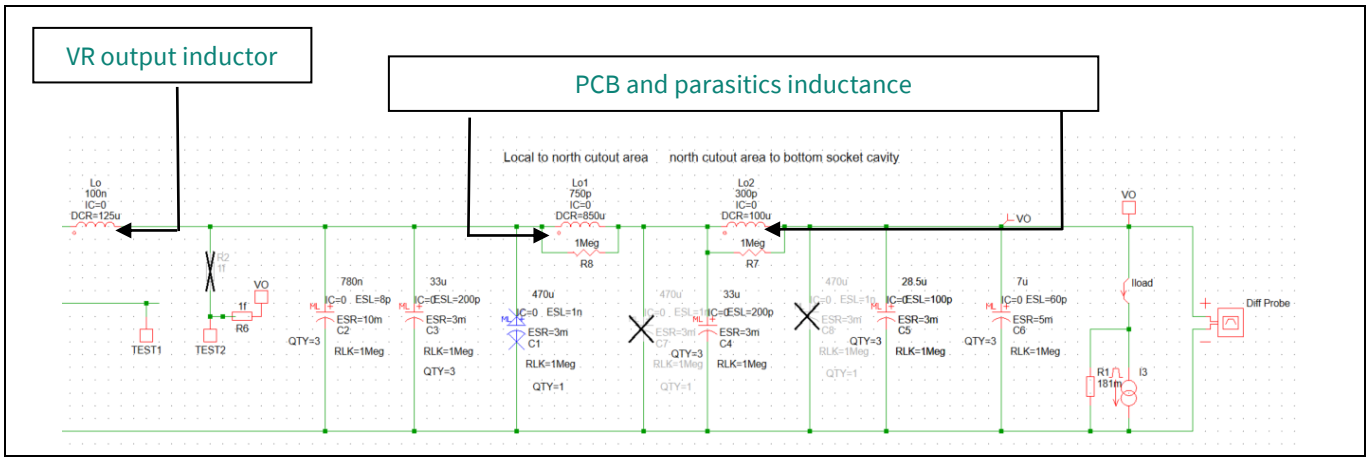

Figure 6 Simulation circuit with higher capacitance close to VR

4.1.1.1 Case 1: Simulation test setup and conditions

PVCCD_HV rail is taken as an example for the analysis.

Table 1 Case 1: Simulation test conditions

Parameter	Value	Unit
Output voltage	1.1	V
Switching frequency	1400	kHz
Load line	2.5	mΩ
Load rep rate frequency	230	kHz
Load rep rate duty cycle	20	%
Load step	6 to 27.5	A
Load slew rate	40	A/µs

Simulation and bench results with higher capacitance close to VR and actual load

Table 2 Case 1: Simulation test setup

Parameter	Value	Part number
Output inductance	100 nH (0.125 mΩ DCR)	L101247A-100L
Output capacitors close to VR	1 x 470 µF (2.5 V)	EEFGX0E471R
	3 x 1 µF (16 V, 0402, X6S)	GRM155C81C105KE11
	3 x 47 µF (4 V, 0805, X6S)	GRM21BC80G476ME15
Output capacitors close to the north cutout edge on the bottom	3 x 47 µF (4 V, 0805, X6S)	GRM21BC80G476ME15
Output capacitors close to the bottom socket cavity	3 x 47 µF (2.5 V, 0603, X6S)	GRM188C80E476ME05
	3 x 10 µF (6.3 V, 0402, X6S)	GRM155C80J106ME18

4.1.1.2 Case 1: Simulation results

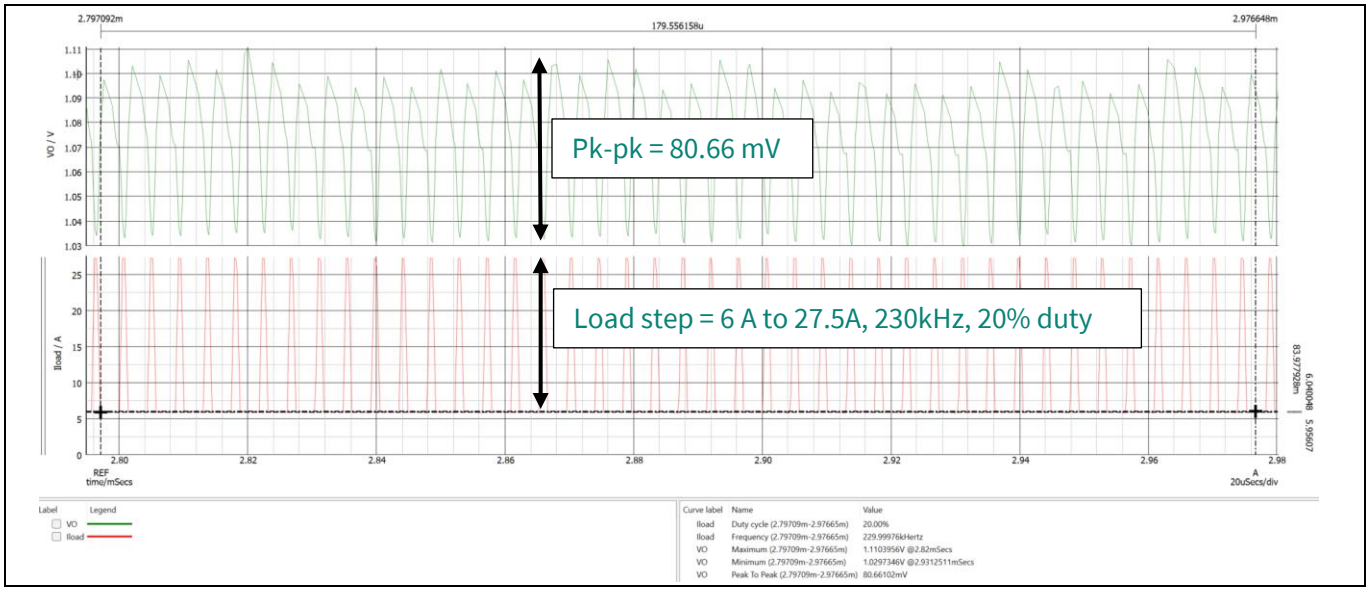

Figure 7 Transient simulation results with SP close to the VR

4.1.2 Case 1: Bench analysis

A 470 µF SP capacitor in this case is placed closer to the VR as shown in Table 3.

Table 3 L and C values for test case 1

Parameter	Value	Part number
Output inductance	100 nH (0.125 mΩ DCR)	L101247A-100L
Output capacitors close to the VR	1 x 470 µF (2.5 V)	EEFGX0E471R
	3 x 1 µF (16 V, 0402, X6S)	GRM155C81C105KE11
	2 x 47 µF (4 V, 0805, X6S)	GRM21BC80G476ME15
Output capacitors close to the north cutout edge on the bottom	3 x 47 µF (4 V, 0805, X6S)	GRM21BC80G476ME15
Output capacitors close to the bottom socket cavity	3 x 47 µF (2.5 V, 0603, X6S)	GRM188C80E476ME05
	4 x 10 µF (6.3 V, 0402, X6S)	GRM155C80J106ME18

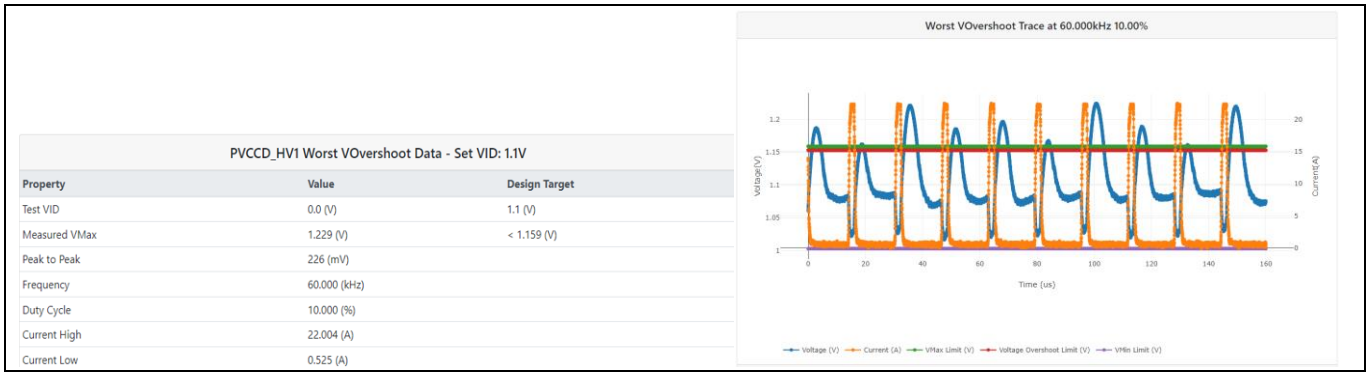

Figure 8 Worst case $V_{overshoot}$ for higher capacitance closer to VR

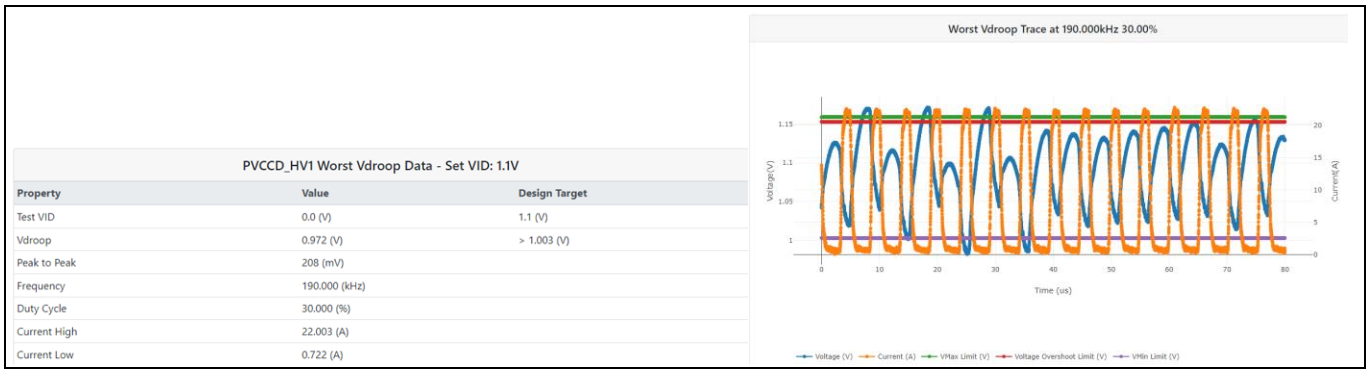

Figure 9 Worst case V_{droop} for higher capacitance closer to VR

4.2 Case 2: Higher capacitance close to the load

In this case, a 470 µF SP capacitor is placed close to the load as shown in Figure 10 making Co1 >> Co as referred to Section 3.4.

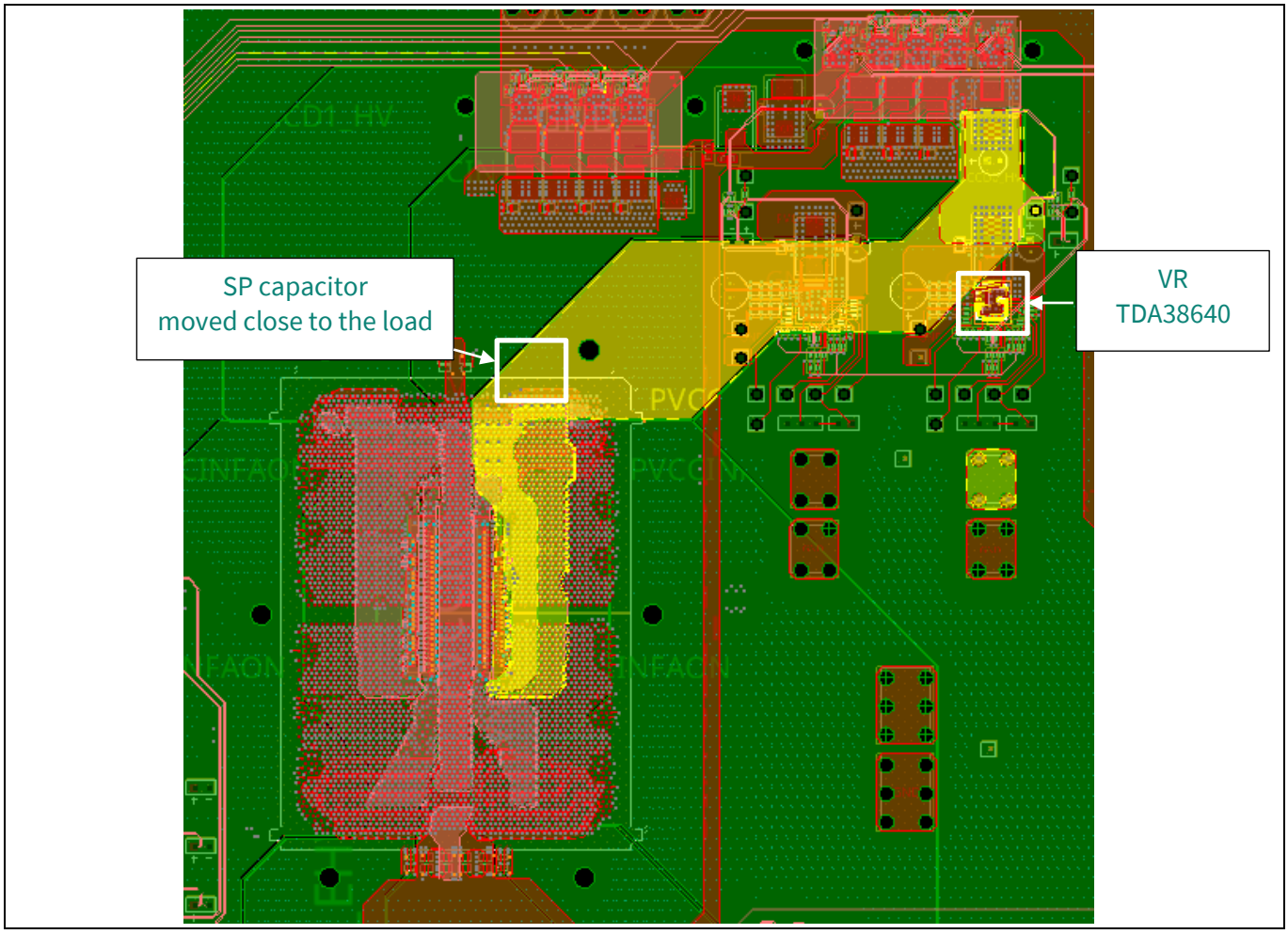

Figure 10 VR and SP capacitor placement on the test board for case 2

4.2.1 Case 2: Simulation analysis

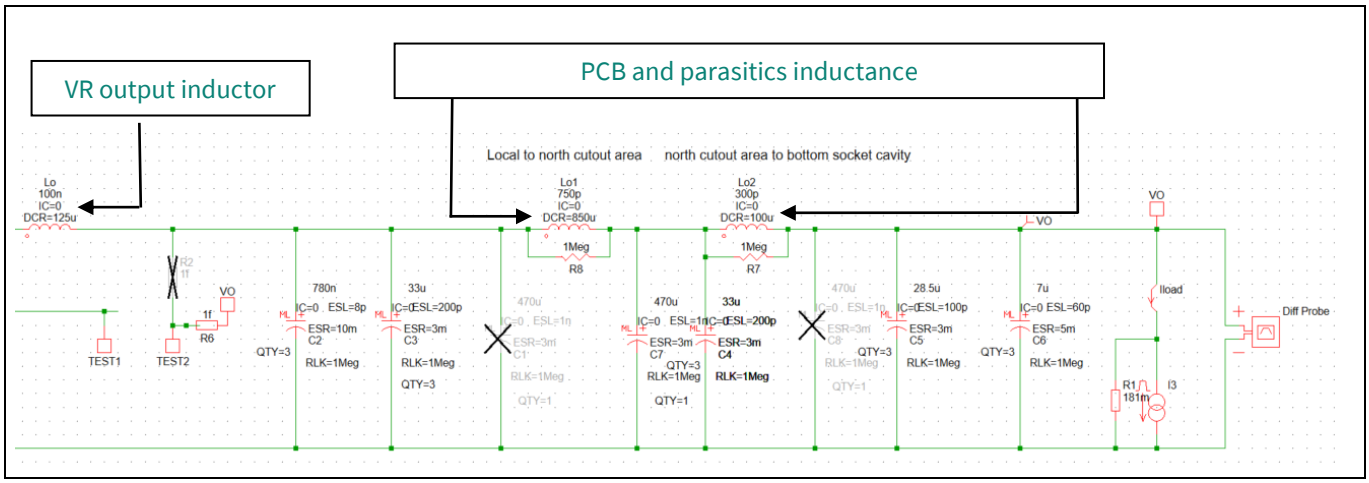

Figure 11 Case 2: Simulation circuit with higher capacitance close to the load

4.2.1.1 Case 2: Simulation test set up and conditions

PVCCD_HV rail is taken as an example for the analysis.

Table 4 Case 2: Simulation test conditions

Parameter	Value	Unit
Output voltage	1.1	V
Switching frequency	1400	kHz
Load line	2.5	mΩ
Load rep rate frequency	230	kHz
Load rep rate duty cycle	20	%
Load step	6 to 27.5	A
Load slew rate	40	A/µs

Table 5 Case 2: Simulation set up

Parameter	Value	Part number
Output inductance	100 nH (0.125 mΩ DCR)	L101247A-100L
Output capacitors close to VR	3 x 1 µF (16 V, 0402, X6S)	GRM155C81C105KE11
	3 x 47 µF (4 V, 0805, X6S)	GRM21BC80G476ME15
Output capacitors close to the north cutout edge on the bottom	3 x 47 µF (4 V, 0805, X6S)	GRM21BC80G476ME15
	1 x 470 µF (2.5 V)	EEFGX0E471R
Output capacitors close to the bottom socket cavity	3 x 47 µF (2.5 V, 0603, X6S)	GRM188C80E476ME05
	3 x 10 µF (6.3 V, 0402, X6S)	GRM155C80J106ME18

4.2.1.2 Case 2: Simulation results

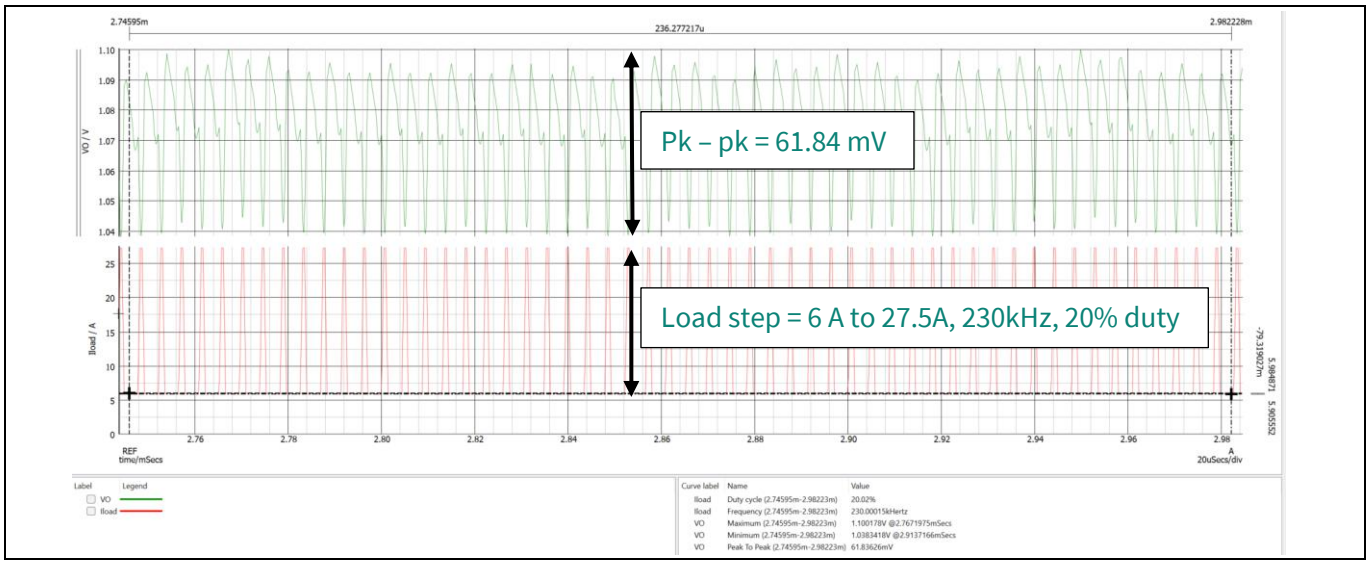

Figure 12 Transient results with SP close to the load

4.2.2 Case 2: Bench analysis

Table 6 L and C values for test case 2

Parameter	Value	Part number
Output inductance	100 nH (0.125 mΩ DCR)	L101247A-100L
Output capacitors close to the VR	3 x 1 µF (16 V, 0402, X6S)	GRM155C81C105KE11
	2 x 47 µF (4 V, 0805, X6S)	GRM21BC80G476ME15
Output capacitors close to the north cutout edge on the bottom	3 x 47 µF (4 V, 0805, X6S)	GRM21BC80G476ME15
	1 x 470 µF (2.5 V)	EEFGX0E471R
Output capacitors close to the bottom socket cavity	3 x 47 µF (2.5 V, 0603, X6S)	GRM188C80E476ME05
	4 x 10 µF (6.3 V, 0402, X6S)	GRM155C80J106ME18

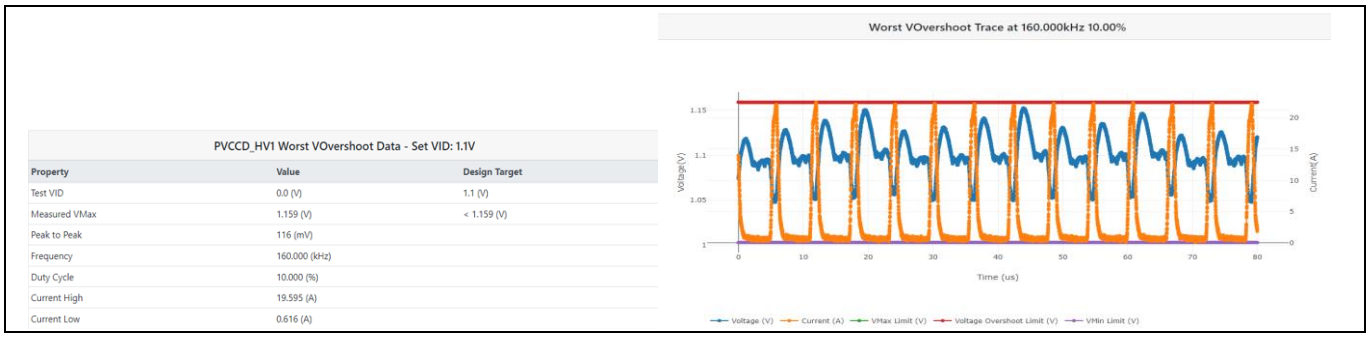

Figure 13 Worst case $V_{overshoot}$ for higher capacitance close to the load

Simulation and bench results with higher capacitance close to VR and actual load

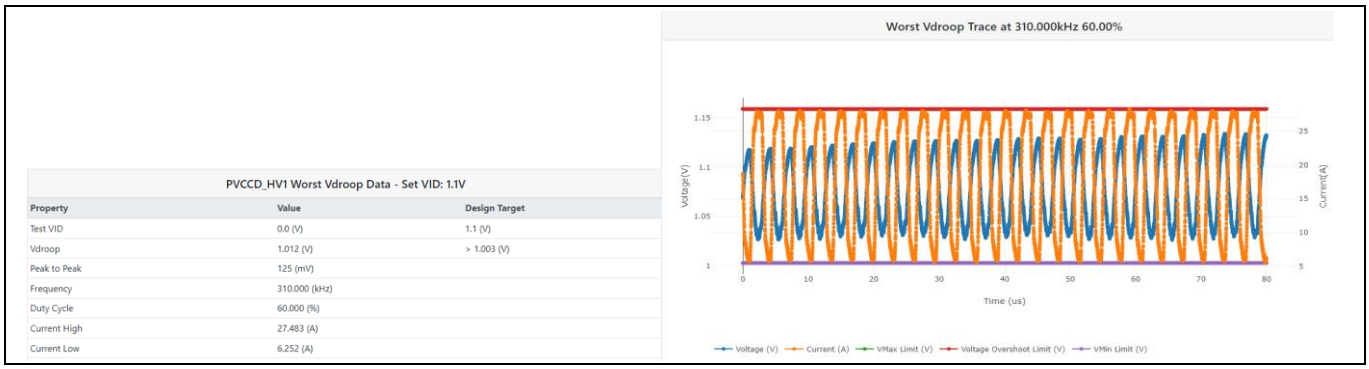

Figure 14 Worst case V_{droop} for higher capacitance close to the load

5 Summary

Table 7 Summary of transient performance

Capacitance	Simulation	Bench	Reason
VR local capacitance >> Capacitance close to the load (case 1)	V_{o_pkpk} = 80.66 mV	$V_{overshoot}$ (V) = 1.229 V $V_{undershoot}$ (V) = 0.972 V	The output impedance peaking occurs at high frequency due to the secondary resonance that affects the dynamic performance at high frequency repetitive load conditions.
Capacitance close to the load >> VR local capacitance (case 2)	V_{o_pkpk} = 61.84 mV	$V_{overshoot}$ (V) = 1.159 V $V_{undershoot}$ (V) = 1.012 V	The impact of secondary LC on the output impedance is eliminated because of a better damping resulting in reduced output impedance peaking at higher frequencies.

Observe that the transient performance has been improved by placing higher capacitance closer to the load than the VR. This would result in a faster transient response because of the reduced output impedance peaking and increased damping of the secondary resonance. A few MLCC capacitors in parallel placed close to the load would be the best choice considering space and cost of the system.

References

[1] Infineon Technologies AG: *Introduction of Fast COT*; Available online

[2] R. B. Ridley*: Secondary LC filter analysis and design techniques for current-mode-controlled converters* presented at IEEE power electronics conference October 1988; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2024-03-20	Initial release
V 1.1	2024-11-06	Simplified the application note with only two cases and added a literature study section

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