Configuring the HOTLink II™ CYP15G0403DXB Device for Multiple Protocols - AN067

AN067

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Associated Project: No
Associated Application Notes: None

Abstract

The HOTLink II™ family of physical layer (PHY) devices is a point-to-point or point-to-multipoint communications building block that provide serialization, deserialization, optional 8B/10B encoding/decoding and framing functions. CYP(V)15G0403DXB is a member of the HOTLink II family that has four independent transceivers that have separate reference clock inputs (Independent Clocking) for each channel. It can transport serial data at rates from 195 Mbps to 1.5 Gbps per channel and is compliant with communication standards such as Gigabit Ethernet (GbE), Fibre Channel, SMPTE 259M, SMPTE 292M, DVB-ASI and ESCON®. The only additional feature present in the CYV15G0403DXB compared to the CYP15G0403DXB is the ability to pass pathological pattern tests as defined in SMPTE EG34-1999.

Introduction

This application note focuses on configuring the CYP15G0403DXB for multiple protocols; specifically, Fibre Channel, ESCON, GbE and DVB-ASI. Configuration of CYP15G0403DXB for digital video transport (SMPTE 259M, SMPTE 292M and DVB-ASI) are covered in the application note entitled Configuring the HOTLink II CYP15G0403DXB device for Digital Video Transport.

The first section of this application note focuses on the benefits of independent clocking. The second section focuses on the specifics of configuring the CYP15G0403DXB for operation under different protocols.

Benefits of Independent Clocking

CYP15G0403DXB's independent clocking and independent configuration features can be used by customers in two types of applications:

1. Multiple protocols over different channels: Each channel can transmit and receive client traffic from a different protocol (different data rate). For example, Channel A passes GbE traffic, while Channel B passes Fibre Channel traffic. An example of this application is illustrated in Figure 1.
2. Multiple channels pass traffic from the same protocol but from different sources: Each channel can pass client traffic from the same protocol (same data rate), but the individual channels can be referenced by different clocks that need not be synchronous to each other, or in other words, the reference clocks for each channel can have a frequency offset with respect to each other. An example of this is illustrated in Figure 2 on page 2.

Configuration Interface

The CYP15G0403DXB has a configuration interface that consists of a 4-bit address bus (ADDR[3:0]) and an 8-bit data bus (DATA[7:0]). The address bus selects one of 16 latch-banks. Each latch-bank has eight latches. The block level description of the configuration interface is shown in Figure 3. The 4-bit address is decoded to enable one of the sixteen latch-banks. The enable signal for each latch-bank (or row) is indicated in Figure 3 as EN_x with the associated value of ADDR[3:0] to its right. The input $\overline{\text{WREN}}$ is the write enable signal for all latch-banks. When $\overline{\text{WREN}}$ is asserted, the values of DATA[7:0] are latched into the latch-bank selected by ADDR[3:0].

Figure 1. Example Of CYP15G0403DXB Transporting Traffic From Multiple Protocols

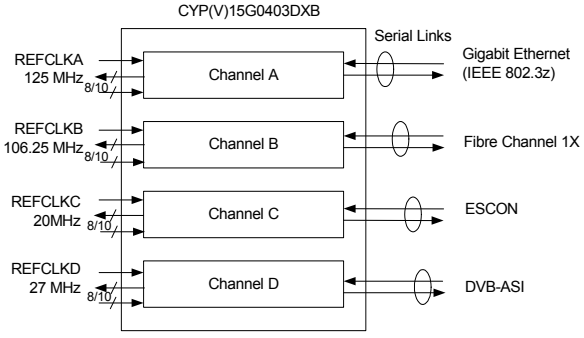


Figure 2. Example Of CYP15G0403DXB Transporting Data At Same Data Rate But Different Sources

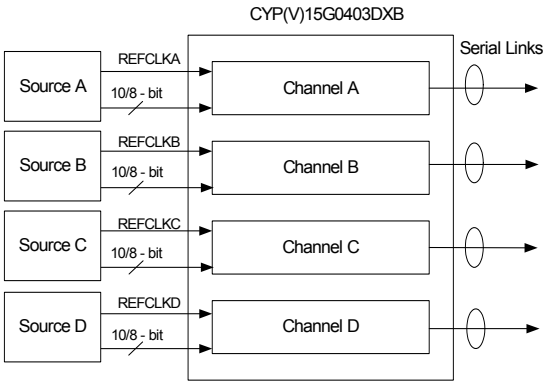
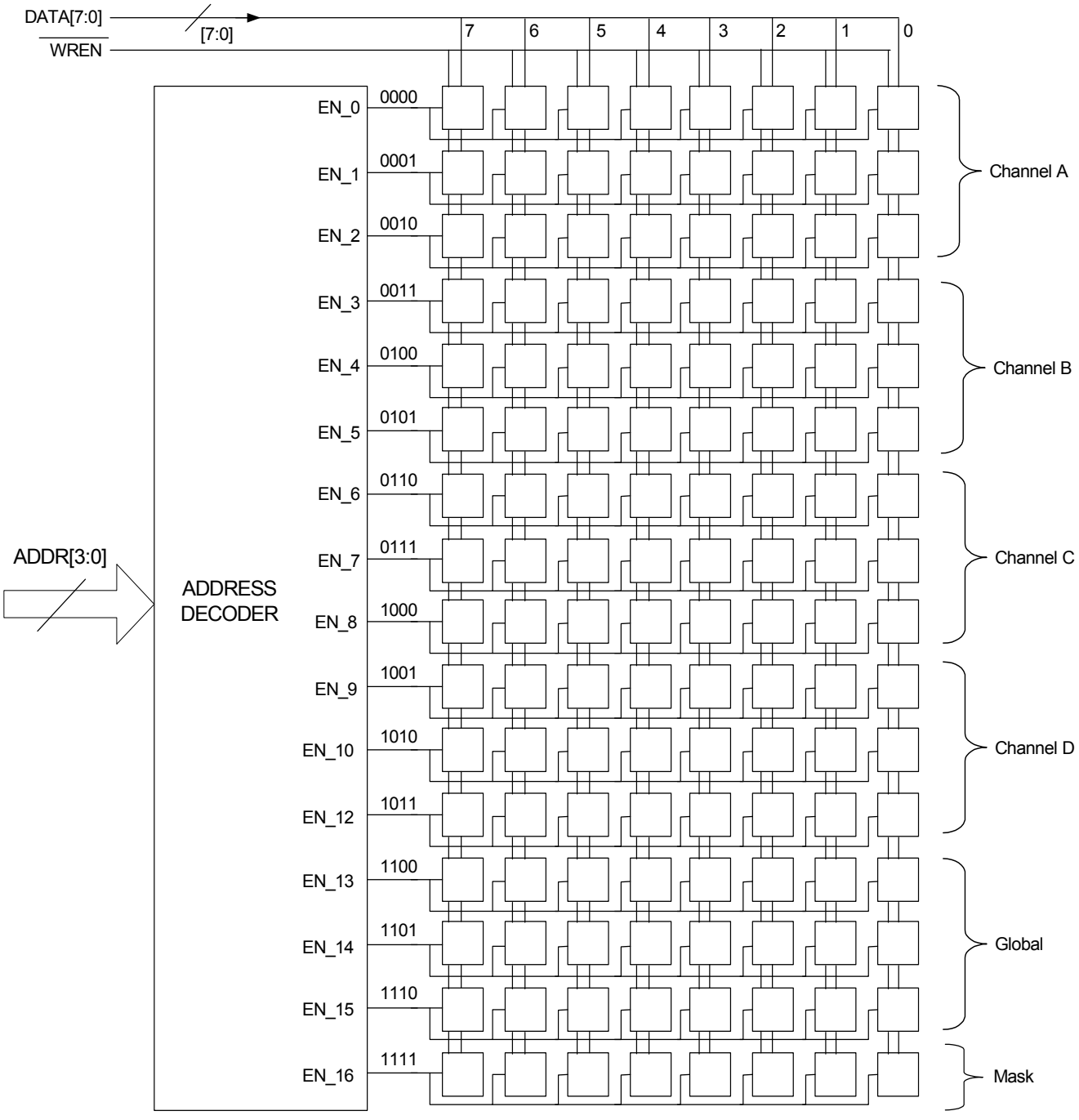


Figure 3. Block Diagram of the CYP15G0403DXB Configuration Interface



Organization of the Latch-Banks

The first set of three latch-banks (0, 1 and 2) control the settings of Channel A. The second set of three latch-banks (3, 4 and 5) control the settings of Channel B. Similarly, latch-banks 6, 7, 8 and 9, 10, 11 control the settings of Channel C and Channel D, respectively. The latch-banks 12, 13, 14 contain the Global configuration latches that can be used for controlling all channels globally. The last latch-bank, 15, is the Mask latch-bank used for bit-by-bit configuration. The mapping of the latches in each latch-bank is shown in Table 3 in APPENDIX A on page 12. The definitions of these configuration bits can be found in the data sheet.

Static Latches and Dynamic Latches

There are two types of latch banks: static (S) and dynamic (D). Each channel is configured by two static and one dynamic latch banks. The S-type controls those settings that normally do not change during the lifetime of an application, whereas the D-type controls the settings that could change during the application's lifetime. The first row of latches for each channel (address numbers 0, 3, 7 and 10) are the static receiver control latches. The second row of latches for each channel (address numbers 1, 4, 8 and 11) are the static transmitter control latches. The third row of latches for each channel (address numbers 2, 5, 9 and 12) are the dynamic control latches.

When to Use the Global Configuration Feature

The global configuration latch banks (12, 13 and 14) help limit the number of WRITE operations required when all channels in the device are to be configured with the same settings. The global update of the target latch banks will occur only when GLENx = 1 or associated FGLENx = 1. The initialization value of GLENx is 1, thereby allowing global configuration upon reset. The target latch banks for each global configuration latch bank are shown in Table 1. If all four channels are supposed to be configured with the same settings, writing to the global configuration latch banks will completely configure all four channels simultaneously.

Table 1. Global Configuration

Global Configuration Latch Bank	Target Latch Banks	Conditions for Global Configuration
12	0, 3, 6 and 9	Associated GLENx = 1 or FGLEN0 = 1
13	1, 4, 7 and 10	Associated GLENx = 1 or FGLEN1 = 1
14	2, 5, 8 and 11	Associated GLENx = 1 or FGLEN2 = 1

When to Use Bit-by-bit Configuration

The bit-by-bit configuration feature should be used whenever one or more bits in a particular latch bank need to be changed without altering the contents of the other bits in that latch bank. The mask vector in latch bank 15 is used for masking the latches whose contents should remain unaltered. The masking of bits that need to remain unaltered is done by setting the associated mask bit to '0'. After setting the desired mask bits, subsequent write operations to any other latch bank will alter the contents of the bits for which the associated mask bit is '1'. The initialize value of the mask vector is "11111111," thereby making its use optional on reset.

An example of where the bit-by-bit configuration feature is useful is in performing a phase-align reset. A phase-align reset should be performed on the transmit channel after configuring the transmit channel settings. The steps needed for performing a phase align reset on channel A, for example, without altering the contents of any other configuration bits are:

1. Set all bits in the mask vector latch bank to 0, except bit DATA[1]. This done by writing "00000010" to address 15.
2. Write the data "XXXXXX0X" to latch bank 2 (channel A) where 'X' stands for a "don't care" value. Note that the PABRSTx is a self-clearing latch. Therefore, there is no need to rewrite a '1' to complete the reset of the phase align buffer.

Configuration for Multiple Protocols

This section of the application note covers the requirements and settings to operate any channel of the CYP15G0403DXB HOTLink II device under a specific protocol. The protocols covered are Fibre Channel, ESCON (SBCON), GbE (IEEE 802.3z) and DVB-ASI.

Configuration for Fibre Channel

The HOTLink II family of devices support Fibre Channel operation at a data rate of 1.0625 GBaud.

Speed Settings

The operating data rate supported by HOTLink II for Fibre Channel is 1.0625 Gbps. For the operating data rate of 1.0625 Gbps, SPDSELx for the given channel should be HIGH.

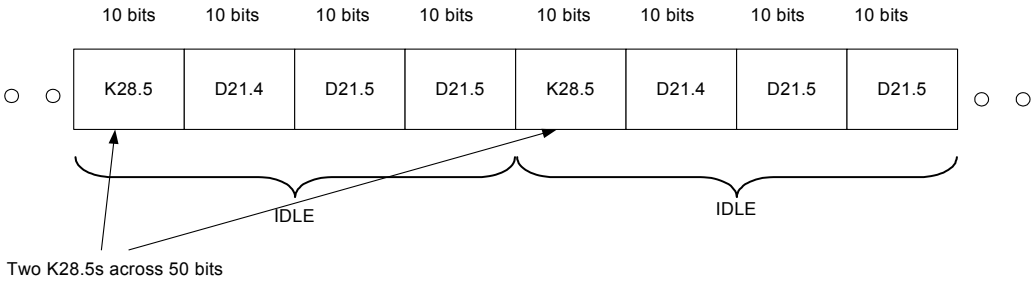
Reference Clock

As per Fibre Channel standard, the REFCLKx± for the given channel must have a frequency stability within ±100 ppm. It could be either a full-rate clock at 106.25 MHz or a half-rate clock at 53.125 MHz. When a half-rate clock (53.125 MHz) is used as the reference clock, TXRATEx for the associated channel should be set to '1'. When a full-rate clock (106.25 MHz) is used, TXRATEx for the associated channel should be set to '0'.

When a half-rate clock is used as the reference clock (TXRATEx = 1) and REFCLKx is selected as the transmit clock (TXCKSELx = 1), the transmit characters will be alternately latched into the input registers using the rising edges of REFCLKx+ and REFCLKx–.

The jitter from the reference clock should be low enough to ensure that the serial output from the HOTLink II device meets the Fibre Channel jitter specification.

Figure 4. IDLE Transmission in Fibre Channel Satisfying Cypress Mode MByte Framer Requirements



Transmit Clock

If TXCLKx is selected as the input clock to latch the parallel input data to the input register (TXCKSELx = '0'), the TXCLKx should be synchronous in frequency to REFCLKx. The phase align buffer must be reset after the presence of TXCLKx and after the TXPLL has locked to REFCLKx frequency.

8B/10B Encoder and 10B/8B Decoder

The HOTLink II transmitter block has an in-built 8B/10B encoder that should be enabled (ENCBYPx = 1) to map the raw 8-bit data characters to the corresponding 10-bit transmission character with the correct disparity as specified by Fibre Channel. The receiver block has an in-built 10B/8B decoder that should be enabled (DECBYPx = 1) to decode the received 10-bit transmission character to the corresponding 8-bit data character.

Framer

The recommended framer for Fibre Channel data reception is Cypress-mode Multi-Byte framer (RFMODEx[1:0] ="10"). In this framing mode, the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

All ordered sets and primitives in Fibre Channel have a K28.5 followed by three data characters (e.g., IDLE is K28.5 – D21.4 – D21.5 – D21.5). When ordered sets or idles are being transmitted, two instances of K28.5s will occur in successive ordered sets in identical 10-bit boundaries across 50 bits. When this is detected by the Cypress-mode Multi-Byte framer, the HOTLink II receiver frames the character boundaries correctly. An example of this is illustrated in Figure 4.

Although HOTLink II can be configured to frame to a single detection of a comma character, the Cypress-mode Multi-Byte framer to frame to two occurrences of K28.5 characters in a span of 50 bits is more reliable.

Framing Character

For the reasons mentioned in the previous section on Framer, the framing character should be set to K28.5 (FRAMCHARx = 1).

Receive Clock Source (Local Receiver Clock)

As required by the Fibre Channel specification, the received data should be clocked out of the output register to upstream logic using the recovered clock by selecting RXCKSELx = 0.

Receive Clocking Rate

As recommended in the Fibre Channel specification, the receive clocking rate could be set to half-rate clocking (RXRATEx = 1). RXCLKx+ and RXCLKx– will both be half-rate clocks operating at half the character rate. The received characters will be latched alternately on the rising edge of RXCLKx+ and RXCLKx–.

Configuration for ESCON (SBCON)

The HOTLink II device family of devices support ESCON (SBCON) operation at data rate of 200 MBaud.

Speed Settings

The operating data rate supported by the HOTLink II device for ESCON is 200 Mbps. For this data rate, the SPDSELx of the given channel should be LOW.

REFCLKx±

The REFCLKx± of the given channel must be supplied by a stable source. It must be a full-rate clock (TXRATEx = 0) at a frequency of 20 MHz. Half-rate operation at this speed range is not supported by HOTLink II.

The jitter from the reference clock should be low enough to ensure that the serial output from the HOTLink II device meets the ESCON jitter specification.

Transmit Clock

If TXCLKx is selected as the input clock to latch in the parallel input data (TXCKSELx = ‘0’), TXCLKx should be synchronous in frequency with REFCLKx. The phase align buffer must be reset after the presence of TXCLKx and after the TXPLL has locked to frequency of REFCLKx.

8B/10B Encoder and 10B/8B Decoder

The HOTLink II transmitter block has an built-in 8B/10B encoder that should be enabled (ENCBYPx = 1) to map the raw 8-bit data characters to the corresponding 10-bit transmission character with the correct disparity as specified by ESCON. The receiver block has an built-in 10B/8B decoder that should be enabled (DECBYPx = 1) to decode the received 10-bit transmission character to the corresponding 8-bit data character.

Framer

The recommended framer for ESCON data reception is the Cypress-mode Multi-Byte framer (RFMODEx[1:0] = ”10”). In this framing mode, the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

The K28.5 special character is defined by ESCON as the idle character that will also be used to establish character alignment. According to the ESCON specification, a link-level facility should transmit at least four consecutive idle characters in between two frames. Moreover, all Sequence Functions in ESCON contain a K28.5 character followed by a single data character. Therefore, the Cypress-mode Multi-Byte framer will establish framing whenever IDLEs are transmitted or when Sequence Functions are transmitted.

Avoiding the use of the low-latency single-byte framer for ESCON data reception is recommended because it could misframe to alias framing characters.

Framing Character

For the reasons mentioned in the previous section on Framer, the framing character should be set to K28.5 (FRAMCHARx = 1).

Receive Clock Source (Local Receiver Clock)

As required by the ESCON specification, the received data should be clocked out of the output register to upstream logic using the recovered clock by selecting RXCKSELx = 0.

Receive Clocking Rate

The receive clocking rate should be set to full-rate clocking (RXRATEx = ’0’).

Configuration for GbE (IEEE STD 802.3z)

The HOTLink II family of devices supports TBI mapping of GbE (IEEE STD 802.3Z) operations at a data rate of 1.25 GBaud. With additional glue logic, the HOTLink II device can support GMII mapping of GbE. For more details on implementing GMII mapping of GbE using HOTLink II, refer to the application note entitled Using HOTLink II for Gigabit Ethernet.

Speed Settings

HOTLink II can operate at the GbE data rate of 1.25 GBaud. For the operating data rate of 1.25 GBaud, SPDSELx should be HIGH.

Reference Clock

As per GbE standard, the REFCLKx± must have a frequency stability within ±100 ppm. It could be either a full-rate clock at 125 MHz or a half-rate clock at 62.5 MHz. When a half-rate clock (62.5 MHz) is used as the reference clock, TXRATEx for the associated channel should be set to ‘1’. When a full-rate clock (125 MHz) is used, TXRATEx for the associated channel should be set to ‘0’.

The jitter from the reference clock should be low enough to ensure that the serial output from the HOTLink II device meets the GbE jitter specification.

Transmit Clock

If TXCLKx is selected as the input clock to latch in the parallel input data (TXCKSELx = ‘0’), it should be synchronous in frequency to REFCLKx. The phase align buffer must be reset after the presence of valid TXCLKx and after the TXPLL has locked to REFCLKx frequency.

8B/10B Encoder and 10B/8B Decoder

For TBI mapping, the 8B/10B encoder and the 10B/8B decoder must be bypassed (ENCBYPx = 0, DECBYPx = 0). The raw 10-bit data provided in the parallel inputs is serialized and transmitted through the serial outputs. The received serial data is deserialized as raw 10-bit data.

Framer

If the upstream link layer device has a built-in framer, the HOTLink II framer is optional.

If the framing function of HOTLink II is utilized, the recommended framer for GbE data reception is the Cypress-mode Multi-Byte framer (RFMODEx[1:0] = ”10”). In this framing mode, the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

In GbE, K28.5s are sent as part of I1, I2, C1, and C2 ordered sets. The IDLE ordered sets, I1 and I2, contain a K28.5 followed by one data character. Hence, when IDLE ordered sets are transmitted, the K28.5s are spaced across 30 bits in two successive occurrences of the ordered set. An example is illustrated in Figure 5 on page 7. The CONFIGURATION ordered sets, C1 and C2, contain a K28.5 followed by three data characters. Therefore, when CONFIGURATION ordered sets are transmitted, the K28.5s are spaced across 50 bits in two successive occurrences of the ordered set. In both

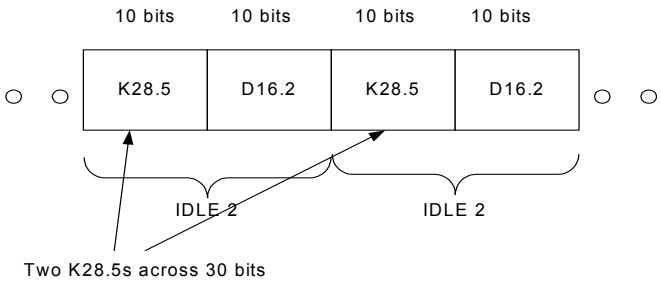
cases, they meet the Cypress Mode Multi-Byte framer requirements.

Although the HOTLink II receiver can be configured to frame to a single detection of a comma character, using the Cypress Mode Multi-Byte framer is more reliable.

Framing Character

For the reasons mentioned in the previous section on Framer, the framing character should be set to K28.5 (FRAMCHARx = 1).

Figure 5. IDLE2 Transmission in Gigabit Ethernet satisfying Cypress Mode Multi-Byte Framer requirements



Receive Clock Source (Local Receiver Clock)

The received data should be clocked to upstream logic using the recovered clock by selecting RXCKSELx = 0.

Receive Clocking Rate

The receive clocking rate should be set to half-rate clocking (RXRATEx = ’1’) for TBI mapping. RXCLKx+ and RXCLKx– will both be clocks operating at half the character rate. The received characters should be latched alternately on the rising edges of RXCLKx+ and RXCLKx–. One of these clocks is used to latch the odd numbered code groups. The other clock is used to latch the even numbered code group.

Lock to Reference

The LCK_REF function specified by TBI mapping of GbE can be accomplished by ULCx signal. When ULCx is asserted, the RXPLL locks to the local reference clock (REFCLKx±).

Configuration for DVB-ASI

The HOTLink II family of devices support DVB-ASI operation at a transmission rate of 270 MBaud.

Speed Settings

The operating data rate supported by HOTLink II for DVB-ASI is 270 Mbps. For this data rate, the SPDSELx for the given channel should be LOW.

Reference clock

As per DVB-ASI standard [Reference 5], REFCLKx± for the given channel must have a frequency stability within ±100 ppm. It should be a full-rate clock at 27 MHz. Half-rate REFCLKx± is not allowed for this speed range. Therefore, TXRATEx must be set to 0.

The jitter from the reference clock should be low enough to ensure that the serial output from the HOTLink II device meets the DVB-ASI Jitter specification. It is recommended to use a stable source as the reference clock.

Transmit Clock

If TXCLKx is selected as the input clock to latch the parallel input data into the input register (TXCKSELx = ‘0’), TXCLKx should be synchronous in frequency to REFCLKx. The phase align buffer must be reset after the presence of data, after the presence of TXCLKx, and after the TXPLL has locked to the REFCLKx frequency.

8B/10B Encoder and 10B/8B Decoder

The HOTLink II transmitter block has a built-in 8B/10B encoder that should be enabled (ENCBYPx = 1) to map the raw 8-bit data characters to the corresponding 10-bit transmission character with the correct disparity as specified by DVB-ASI. The receiver block has a built-in 10B/8B decoder that should be enabled (DECBYPx = 1) to decode the received 10-bit transmission character to the corresponding 8-bit data character.

Framer

The recommended framer for DVB-ASI data reception is the Cypress-mode Multi-Byte framer (RFMODEx[1:0] = ”10”). In this framing mode, the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

All transport packets in DVB-ASI must be preceded by two successive K28.5 characters. When this is detected by the Cypress-mode Multi-Byte framer, it meets the framer requirements for the HOTLink II receiver to frame to the correct character boundaries.

Framing Character

For the reasons mentioned in the previous section on Framer, the framing character should be set to K28.5 (FRAMCHARx = 1).

Receive Clock Source (Local Receiver Clock)

The received data can be clocked out of the output register to upstream logic either using the recovered clock (RXCKSELx = 0) or the local reference clock REFCLKx± (RXCKSELx = 1).

When REFCLKx± is used as the output clock for the output register, the data is read out of the elasticity buffer which inserts or deletes K28.5 characters from the transport stream to accommodate for the frequency differences between the incoming stream and the local reference clock. Therefore, sufficient K28.5 characters should be interspersed within the transport stream when RXCKSELx selects REFCLKx± as the output clock.

Receive Clocking Rate

The receive clocking rate must be set to full-rate clocking (RXRATEx = 0). The received characters will be latched every rising edge of RXCLKx+ or every falling edge of RXCLKx–.

Summary

The Independent Clocking feature of CYP15G0403DXB can be used in applications that need to transport protocols at different data rates as well as applications that need to transmit data from different reference clock domains. The flexible configuration interface allows both global and independent configuration. The configuration interface can be used to configure a particular channel to any particular communication protocol (Fibre Channel, ESCON, GbE or DVB-ASI). The settings of all control latches and control signals for the four protocols are tabulated in Table 2.

References

1. Fibre Channel—Physical and Signaling Interface, Rev 4.3, 1994.
2. Single-Byte Command Code Sets CONnection Architecture, Rev 2.3, 1996.
3. IEEE STD 802.3‰ —2002, IEEE Computer Society, 2002.
4. Independent Clock Quad HOTLink II (TM) Transceiver data sheet, 38-02065, Cypress Semiconductor Corporation.
5. Cabled Distribution Systems for Television, Sound and Interactive Multimedia Signals, Part 9: Interfaces for CATV/SMATV Headends and Similar Professional Equipment for DVB/MPEG-2 Transport Streams, European Standard EN 50083–9:March 1997.

Table 2. Recommended Configuration for Different Protocols

Control Latch / Control Signal	Fibre Channel (1.0625 GBaud)	ESCON (200 MBaud)	Gigabit Ethernet–TBI (1.25 GBaud)	DVB–ASI (270 MBaud)
RFMODEx[1:0]	“10”: Selects Cypress-mode Multi-Byte framer.	“10”: Selects Cypress-mode Multi-Byte framer.	“10”: Selects Cypress-mode Multi-Byte framer.	“10”: Selects Cypress-mode Multi-Byte framer.
FRAMCHARx	1: Selects K28.5 as framing character.	1: Selects K28.5 as framing character.	1: Selects K28.5 as framing character.	1: Selects K28.5 as framing character.
DECMODEx	User-selectable 1: Selects Cypress Decoding Mode for special characters 0: Selects Alternate Decoding Mode for special characters	User-selectable 1: Selects Cypress Decoding Mode for special characters 0: Selects Alternate Decoding Mode for special characters	1: to bypass10B/8B decoder in the receiver block	User-selectable 1: Selects Cypress Decoding Mode for special characters 0: Selects Alternate Decoding Mode for special characters
DECBYPx	1: Enables 10B/8B decoder in the receiver block.	1: Enables 10B/8B decoder in the receiver block.	0: Bypasses10B/8B decoder in the receiver block.	1: Enables 10B/8B Decoder in the receiver block.

Table 2. Recommended Configuration for Different Protocols (Continued)

Control Latch / Control Signal	Fibre Channel (1.0625 GBaud)	ESCON (200 MBaud)	Gigabit Ethernet–TBI (1.25 GBaud)	DVB–ASI (270 MBaud)
RXCKSELx	0: Selects recovered clock to clock output register	0: Selects recovered clock to clock output register	0: Selects recovered clock to clock output register	User-selectable 0: Selects recovered clock to clock output register 1: Selects REFCLKx± to clock output register, with insertion/deletion of K28.5 characters to absorb the frequency difference between incoming serial data and REFCLKx±
RXRATEx	1: RXCLKx+ and RXCLKx– are complementary clocks operating at half the character rate.	0: RXCLKx+ and RXCLKx– are full-rate complementary clocks operating at the character rate.	1: RXCLKx+ and RXCLKx– are complementary clocks operating at half the character rate.	0: RXCLKx+ and RXCLKx– are full-rate complementary clocks operating at the character rate.
SDASEL1x[1:0]	User-selectable “00”: Analog signal detector disabled “01”: Typical p-p differential voltage threshold level is 140 mV “10”: Typical p-p differential voltage threshold level is 280 mV “11”: Typical p-p differential voltage threshold level is 420 mV	User-selectable “00”: Analog signal detector disabled “01”: Typical p-p differential voltage threshold level is 140 mV “10”: Typical p-p differential voltage threshold level is 280 mV “11”: Typical p-p differential voltage threshold level is 420 mV	User-selectable “00”: Analog signal detector disabled “01”: Typical p-p differential voltage threshold level is 140 mV “10”: Typical p-p differential voltage threshold level is 280 mV “11”: Typical p-p differential voltage threshold level is 420 mV	User-selectable “00”: Analog signal detector disabled “01”: Typical p-p differential voltage threshold level is 140 mV “10”: Typical p-p differential voltage threshold level is 280 mV “11”: Typical p-p differential voltage threshold level is 420 mV
SDASEL2x[1:0]	User-selectable “00”: Analog signal detector disabled “01”: Typical p-p differential voltage threshold level is 140 mV “10”: Typical p-p differential voltage threshold level is 280 mV “11”: Typical p-p differential voltage threshold level is 420 mV	User-selectable “00”: Analog signal detector disabled “01”: Typical p-p differential voltage threshold level is 140 mV “10”: Typical p-p differential voltage threshold level is 280 mV “11”: Typical p-p differential voltage threshold level is 420 mV	User-selectable “00”: Analog signal detector disabled “01”: Typical p-p differential voltage threshold level is 140 mV “10”: Typical p-p differential voltage threshold level is 280 mV “11”: Typical p-p differential voltage threshold level is 420 mV	User-selectable. “00”: Analog signal detector disabled “01”: Typical p-p differential voltage threshold level is 140 mV “10”: Typical p-p differential voltage threshold level is 280 mV “11”: Typical p-p differential voltage threshold level is 420 mV
ENCBYPx	1: Enables 8B/10B encoder in transmitter block	1: Enables 8B/10B encoder in transmitter block	0: bypasses 8B/10B encoder in transmitter block	1: Enables 8B/10B Encoder in transmitter block

Table 2. Recommended Configuration for Different Protocols (Continued)

Control Latch / Control Signal	Fibre Channel (1.0625 GBaud)	ESCON (200 MBaud)	Gigabit Ethernet–TBI (1.25 GBaud)	DVB–ASI (270 MBaud)
TXCKSELx	User-selectable. 0: Recommended. Selects TXCLKx to clock input register. Use TXCLKx synchronous to REFCLKx± to clock input registers. 1: Selects REFCLKx to clock input register	User-selectable. 0: Recommended. Selects TXCLKx to clock input register. Use TXCLKx synchronous to REFCLKx± to clock input registers. 1: Selects REFCLKx to clock input register	User-selectable. 0: Recommended. Selects TXCLKx to clock input register. Use TXCLKx synchronous to REFCLKx± to clock input registers. 1: Selects REFCLKx to clock input register	User-selectable. 0: Recommended. Selects TXCLKx to clock input register. Use TXCLKx synchronous to REFCLKx± to clock input registers. 1: Selects REFCLKx to clock input register
TXRATEx	User-selectable 0: 106.25-MHz source must be used as reference clock 1: 53.125-MHz source must be used as reference clock	0: A full-rate reference clock at 20 MHz must be provided	User-selectable 0: 125 MHz source must be used as reference clock 1: 62.5 MHz source must be used as reference clock	0: A full-rate reference clock at 27 MHz must be provided as REFCLKx±
RFENx	Could be left as 1 if recommendations for RFMODEx[1:0] are followed. This will keep the framer continuously enabled, making reframing possible whenever there is loss of framing.	Could be left as 1 if recommendations for RFMODEx[1:0] are followed. This will keep the framer continuously enabled, making reframing possible whenever there is loss of framing.	Could be left as 1 if recommendations for RFMODEx[1:0] are followed. This will keep the framer continuously enabled, making reframing possible whenever there is loss of framing. Could be set to 0, if upstream device has a built-in framer.	Could be left as 1 if recommendations for RFMODEx[1:0] are followed. This will keep the framer continuously enabled, making reframing possible whenever there is loss of framing.
RXPLLPDx	1: Enables CDR PLL in the receiver block Set to 0 only when the receive block of the channel is not used	1: Enables CDR PLL in the receiver block Set to 0 only when the receive block of the channel is not used	1: Enables the CDR PLL in the receiver block Set to 0 only when the receive block of the channel is not used	1: Enables CDR PLL in the receiver block. Set to 0 only when the receive block of the channel is not used
RXBISTx	1: Receiver BIST function is disabled	1: Receiver BIST function is disabled	1: Receiver BIST function is disabled	1: Receiver BIST function is disabled
TXBISTx	1: Transmitter BIST function is disabled	1: Transmitter BIST function is disabled	1: Transmitter BIST function is disabled	1: Transmitter BIST function is disabled
OE1x	User-selectable. 0: Disables Serial Output Buffer OUT1x± 1: Enables Serial Output Buffer OUT1x±	User-selectable. 0: Disables Serial Output Buffer OUT1x± 1: Enables Serial Output Buffer OUT1x±	User-selectable. 0: Disables Serial Output Buffer OUT1x± 1: Enables Serial Output Buffer OUT1x±	User-selectable. 0: Disables Serial Output Buffer OUT1x± 1: Enables Serial Output Buffer OUT1x±
OE2x	User-selectable 0: Disables Serial Output Buffer OUT2x± 1: Enables Serial Output Buffer OUT2x±	User-selectable 0: Disables Serial Output Buffer OUT2x± 1: Enables Serial Output Buffer OUT2x±	User-selectable 0: Disables Serial Output Buffer OUT2x± 1: Enables Serial Output Buffer OUT2x±	User-selectable 0: Disables Serial Output Buffer OUT2x± 1: Enables Serial Output Buffer OUT2x±

Table 2. Recommended Configuration for Different Protocols (Continued)

Control Latch / Control Signal	Fibre Channel (1.0625 GBaud)	ESCON (200 MBaud)	Gigabit Ethernet–TBI (1.25 GBaud)	DVB–ASI (270 MBaud)
PABRSTx	If TXCLKx± is used as input clock, this latch should be rewritten with a 0 after the completion of device configuration, after the presence of TXCLKx and after the TXPLL has locked to the REFCLKx± input frequency.	If TXCLKx± is used as input clock, this latch should be rewritten with a 0 after the completion of device configuration, after the presence of TXCLKx and after the TXPLL has locked to the REFCLKx± input frequency.	If TXCLKx± is used as input clock, this latch should be rewritten with a 0 after the completion of device configuration, after the presence of TXCLKx and after the TXPLL has locked to the REFCLKx± input frequency.	If TXCLKx± is used as input clock, this latch should be rewritten with a 0 after the completion of device configuration, after the presence of TXCLKx and after the TXPLL has locked to the REFCLKx± input frequency.
LDTDEN	User-selectable HIGH: Range Controller, Transition Density Detector and Signal Level Detector are enabled to determine if RXPLL tracks REFCLKx± LOW: Only Range Controller is used to determine if RXPLL tracks REFCLKx±	User-selectable HIGH: Range Controller, Transition Density Detector and Signal Level Detector are enabled to determine if RXPLL tracks REFCLKx± LOW: Only Range Controller is used to determine if RXPLL tracks REFCLKx±	User-selectable HIGH: Range Controller, Transition Density Detector and Signal Level Detector are enabled to determine if RXPLL tracks REFCLKx± LOW: Only Range Controller is used to determine if RXPLL tracks REFCLKx±	User-selectable HIGH: Range Controller, Transition Density Detector and Signal Level Detector are enabled to determine if RXPLL tracks REFCLKx± LOW: Only Range Controller is used to determine if RXPLL tracks REFCLKx±
ULCx	When LOW, RXCLKx± follows reference clock. Connect to optical module signal detect function. When HIGH, RXCLKx± follows clock selected by RXCKSELx	When LOW, RXCLKx± follows reference clock. Connect to optical module signal detect function. When HIGH, RXCLKx± follows clock selected by RXCKSELx	When LOW, RXCLKx± follows reference clock. Connect to optical module signal detect function. When HIGH, RXCLKx± follows clock selected by RXCKSELx	User-selectable LOW: RXCLKx± follows reference clock. Assert this input when there is no serial data present at the serial inputs. HIGH: RXCLKx± follows clock selected by RXCKSELx
SPDSELx	HIGH. Use strong pull-up resistor (e.g., 100 ohms). Do not provide LVTTL or LVCMOS stimulus.	LOW. Use strong pull-down resistor (e.g., 100 ohms). Do not provide LVTTL or LVCMOS stimulus.	HIGH. Use strong pull-up resistor (e.g., 100 ohms). Do not provide LVTTL or LVCMOS stimulus.	LOW. Use strong pull-down resistor (like 100 ohms). Do not provide LVTTL or LVCMOS stimulus.
INSELx	User-selectable HIGH: IN1x± is selected as input buffer for the associated receive channel LOW: IN2x± is selected as input buffer for the associated receive channel	User-selectable HIGH: IN1x± is selected as input buffer for the associated receive channel LOW: IN2x± is selected as input buffer for the associated receive channel	User-selectable HIGH: IN1x± is selected as input buffer for the associated receive channel LOW: IN2x± is selected as input buffer for the associated receive channel	User-selectable HIGH: IN1x± is selected as input buffer for the associated receive channel LOW: IN2x± is selected as input buffer for the associated receive channel
LPENx	LOW. Setting to HIGH will route the serialized output of the associated channel internally to the Clock and Data Recovery circuit of the same channel.	LOW. Setting to HIGH will route the serialized output of the associated channel internally to the Clock and Data Recovery circuit of the same channel.	LOW. Setting to HIGH will route the serialized output of the associated channel internally to the Clock and Data Recovery circuit of the same channel.	LOW. Setting to HIGH will route the serialized output of the associated channel internally to the Clock and Data Recovery circuit of the same channel.

Appendix A

Table 3. Device Control Latch Configuration Table

ADDR	Channel	Type	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Reset Value
0 (0000b)	A	S	RFMODE A[1]	RFMODE A[0]	FRAMCHAR A	DECMODE A	DECBYP A	RXCKSEL A	RXRATE A	GLEN0	10111111
1 (0001b)	A	S	SDASEL2 A[1]	SDASEL2 A[0]	SDASEL1 A[1]	SDASEL1 A[0]	ENCBYP A	TXCKSEL A	TXRATE A	GLEN1	10101101
2 (0010b)	A	D	RFEN A	RXPLLPD A	RXBIST A	TXBIST A	OE2 A	OE1 A	PABRST A	GLEN2	10110011
3 (0011b)	B	S	RFMODE B[1]	RFMODE B[0]	FRAMCHAR B	DECMODE B	DECBYP B	RXCKSEL B	RXRATE B	GLEN3	10111111
4 (0100b)	B	S	SDASEL2 B[1]	SDASEL2 B[0]	SDASEL1 B[1]	SDASEL1 B[0]	ENCBYP B	TXCKSEL B	TXRATE B	GLEN4	10101101
5 (0101b)	B	D	RFEN B	RXPLLPD B	RXBIST B	TXBIST B	OE2 B	OE1 B	PABRST B	GLEN5	10110011
6 (0110b)	C	S	RFMODE C[1]	RFMODE C[0]	FRAMCHAR C	DECMODE C	DECBYP C	RXCKSEL C	RXRATE C	GLEN6	10111111
7 (0111b)	C	S	SDASEL2 C[1]	SDASEL2 C[0]	SDASEL1 C[1]	SDASEL1 C[0]	ENCBYP C	TXCKSEL C	TXRATE C	GLEN7	10101101
8 (1000b)	C	D	RFEN C	RXPLLPD C	RXBIST C	TXBIST C	OE2 C	OE1 C	PABRST C	GLEN8	10110011
9 (1001b)	D	S	RFMODE D[1]	RFMODE D[0]	FRAMCHAR D	DECMODE D	DECBYP D	RXCKSEL D	RXRATE D	GLEN9	10111111
10 (1010b)	D	S	SDASEL2 D[1]	SDASEL2 D[0]	SDASEL1 D[1]	SDASEL1 D[0]	ENCBYP D	TXCKSEL D	TXRATE D	GLEN10	10101101
11 (1011b)	D	D	RFEN D	RXPLLPD D	RXBIST D	TXBIST D	OE2 D	OE1 D	PABRST D	GLEN11	10110011
12 (1100b)	GLOBAL	S	RFMODE GL[1]	RFMODE GL[0]	FRAMCHAR GL	DECMODE GL	DECBYP GL	RXCKSEL GL	RXRATE GL	FGLEN0	N/A
13 (1101b)	GLOBAL	S	SDASEL2 GL[1]	SDASEL2 GL[0]	SDASEL1GL [1]	SDASEL1 GL[0]	ENCBP GL	TXCKSEL GL	TXRATE GL	FGLEN1	N/A
14 (1110b)	GLOBAL	D	RFEN GL	RXPLLP GL	RXBIST GL	TXBIST GL	OE2 GL	OE1 GL	PABRST GL	FGLEN2	N/A
15 (1111b)	ALL MASK	D	D7	D6	D5	D4	D3	D2	D1	D0	11111111

Document History

Document Title: Configuring the HOTLink II™ CYP15G0403DXB Device for Multiple Protocols - AN067
Document Number: 001-15079

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1012620	NVNS	04/24/2007	Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date Please post in the web- overwrite the existing AN067 file
*A	3246334	NVNS	05/04/2011	Updated in new template.
*B	4384645	NVNS	05/20/2014	No technical updates. Completing Sunset Review.

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