Power Consumption of HOTLink II™ Family of Devices - AN027

AN027

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Abstract

The HOTLink II™ family of physical layer (PHY) devices is a point-to-point or point-to-multipoint communications building block that provide serialization, deserialization, 8B/10B encoding/decoding and framing functions. It can transport serial data at rates between 195 Mbps and 1.5 Gbps per channel and are compatible with communication standards such as Gigabit Ethernet (GbE), Fibre Channel, SMPTE-259M, SMPTE-292M, DVB-ASI and ESCON®.

Introduction

HOTLink II is a highly configurable device with numerous power down options and power saving mechanisms. The power of the device increases with number of channels (transmit or receive) enabled, operating frequency and power supply voltage. The purpose of this application note is to illustrate the power consumed by any device in the family for a given operating frequency and configuration. Apart from illustrating the power consumption for different devices, the application note also discusses the instructions for the Cypress HOTLink II™ Power Estimation Graphical User Interface (GUI). The GUI can be downloaded from http://www.cypress.com/design under Software & Drivers. The file must be opened using MS-Excel software. A screenshot of the GUI is shown Figure 6 on page 7.

The next few sections will cover the following topics:

- Power-saving Features of HOTLink II
- CYP(V)15G0401DXB Power Consumption
- CYP(V)15G0402DXB Power Consumption
- CYP(V)15G0101DXB Power Consumption
- CYP(V)15G0201DXB Power Consumption
- Instruction guide for HOTLink II power estimation GUI.

Power-Saving Features

The ability to power down unused blocks of the HOTLink II to a low current consumption state offers the power savings to the user. The following blocks of the device can be selectively powered down by configuring certain control inputs:

1. Primary and/or secondary serial output buffers (OUTx1± and OUTx2±)
2. Receive channel PLLs (Channel A, B, C and/or D).

Table 1. BOE Signals for Enabling Serial Outputs

BOE Input	CYP(V)15G0401DXB		CYP(V)15G0402DXB		CYP(V)15G0201DXB		CYP(V)15G0101DXB	
	Output Controlled (OELE)	Receive PLL Channel Enable (RXLE)	Output Controlled (OELE)	Receive PLL Channel Enable (RXLE)	Output Controlled (OELE)	Receive PLL Channel Enable (RXLE)	Output Controlled (OELE)	Receive PLL Channel Enable (RXLE)
BOE[7]	OUTD2±							
BOE[6]	OUTD1±	Receive D	OUTD±	Receive D				
BOE[5]	OUTC2±							
BOE[4]	OUTC1±	Receive C	OUTC±	Receive C				

Table 1. BOE Signals for Enabling Serial Outputs (Continued)

BOE Input	CYP(V)15G0401DXB		CYP(V)15G0402DXB		CYP(V)15G0201DXB		CYP(V)15G0101DXB	
	Output Controlled (OELE)	Receive PLL Channel Enable (RXLE)	Output Controlled (OELE)	Receive PLL Channel Enable (RXLE)	Output Controlled (OELE)	Receive PLL Channel Enable (RXLE)	Output Controlled (OELE)	Receive PLL Channel Enable (RXLE)
BOE[3]	OUTB2±				OUTB2±			
BOE[2]	OUTB1±	Receive B	OUTB±	Receive B	OUTB1±	Receive B		
BOE[1]	OUTA2±				OUTA2±		OUTA2±	
BOE[0]	OUTA1±	Receive A	OUTA±	Receive A	OUTA1±	Receive A	OUTA1±	Receive A

Disabling and Enabling Serial Output Buffers

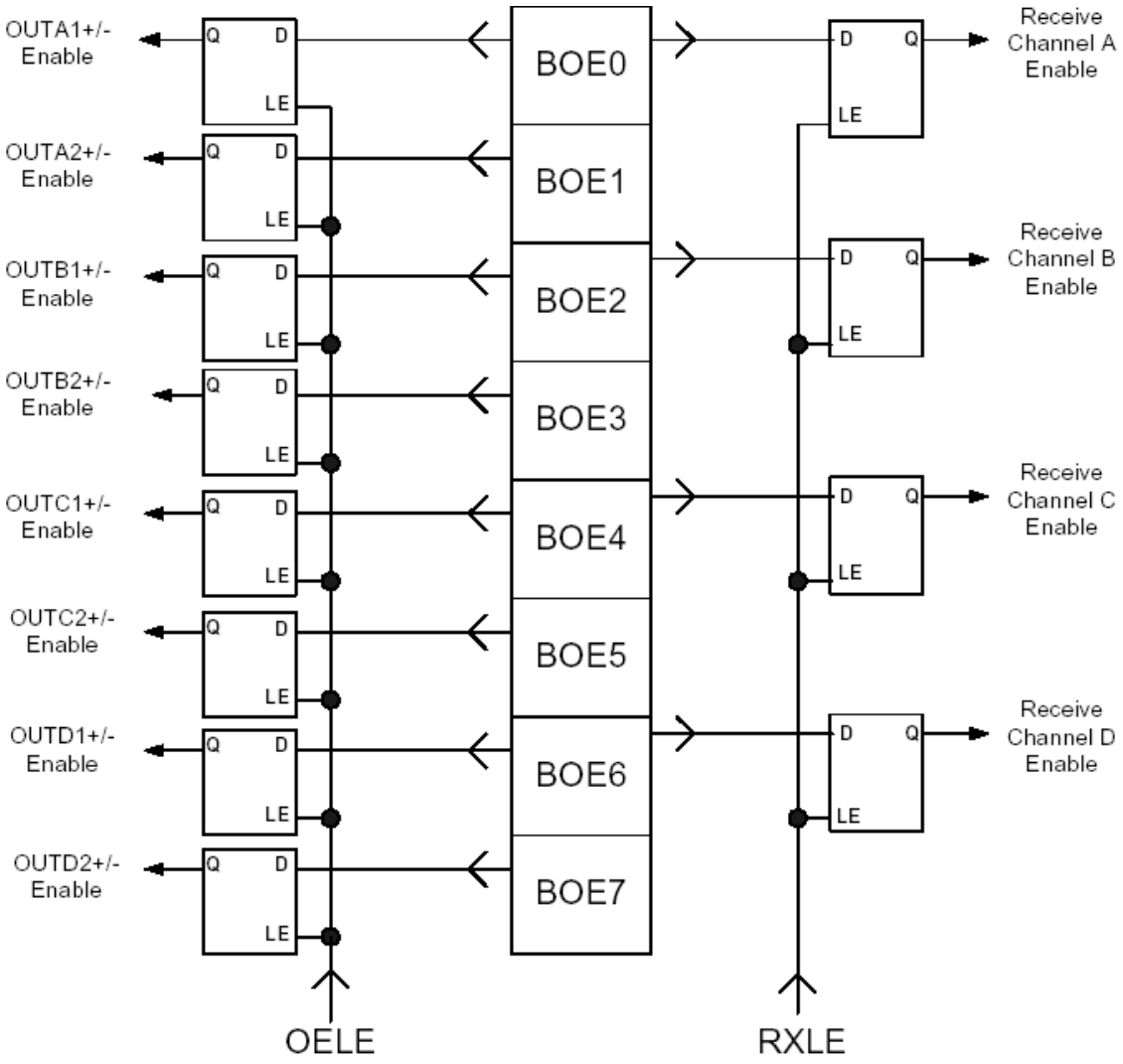
All members of the HOTLink II family, not including CYP(V)15G0402DXB, have two pairs of differential serial output buffers for each transmit channel. One or both output pairs can be used to deliver the serial output differential data.The serial output buffers can be powered up by enabling the Output Enable Latches (OELE = HIGH) and providing a HIGH at the associated BOEx as specified in Table 1 on page 1 and illustrated in Figure 1 on page 3. The serial output buffers can be powered down by enabling the Output Enable Latches (OELE = HIGH) and providing a LOW at the associated BOEx. To power down all the logic in a transmit channel, disable both output buffers (OUTx1± and OUTx2±) associated with the given channel.

Disabling and Enabling Receive Channel PLLs

The receive channel PLLs can be powered up by enabling the receive channel enable latches (RXLE = HIGH) and providing a HIGH at the associated BOEx as specified in Table 1 on page 1 and illustrated in Figure 1 on page 3. The receive channel PLLs can be powered down by enabling the receive channel enable latches (RXLE = HIGH) and providing a LOW at the associated BOEx.

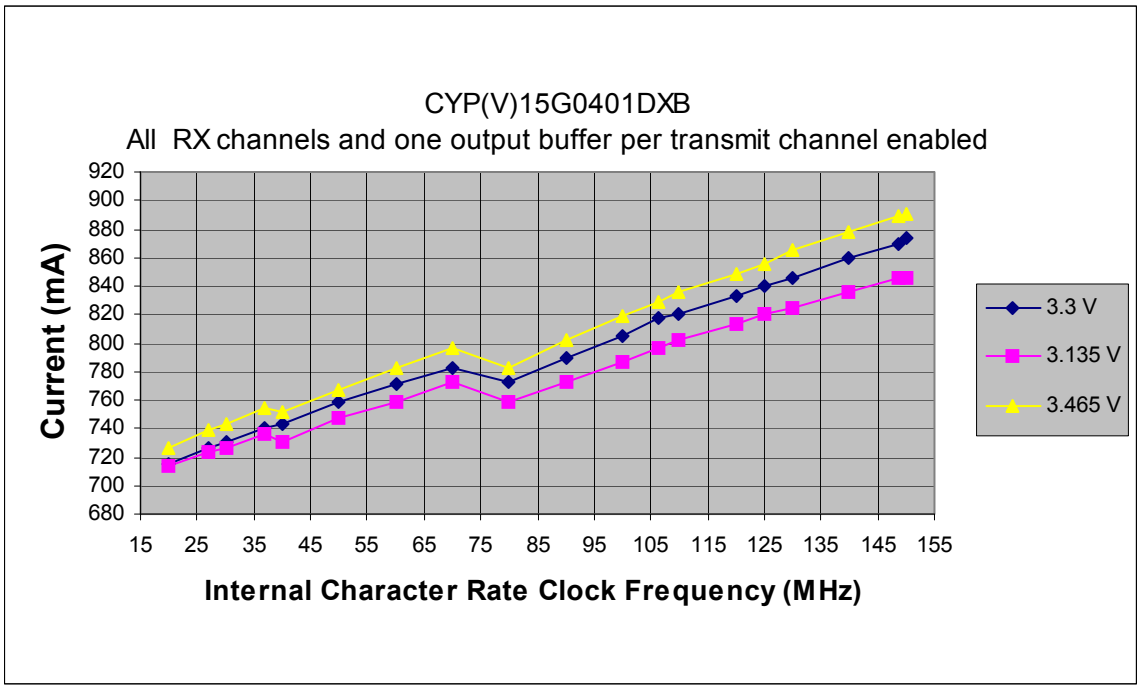
Figure 1 on page 3 depicts the structure of the latches associated with OELE and RXLE. The illustration in Figure 1 on page 3 applies to CYP(V)15G0401DXB, but can also be applied to CYP(V)15G0201DXB and CYP(V)15G0101DXB with appropriately reduced number of channels and BOEs.

Figure 1. Structure of OELE and RXLE Latches for CYP(V)15G0401DXB



Power Consumption of HOTLink II Devices

Figure 2. Power Consumed by CYP(V)15G0401DXB When All Channels are Enabled



This section of the application note describes the power consumption measurements performed for the HOTLink II family. All measurements were performed with all channels enabled at room temperature with parallel outputs unloaded. The power consumption when fewer channels are enabled can be obtained from the “Cypress HOTLink II™ Power Estimation” GUI.

CYP(V)15G0401DXB Power Consumption

The power consumption of CYP(V)15G0401DXB when all four channels are enabled is shown in Figure 2. This data represents the total power consumed when all receive channels (A, B, C and D) and one output buffer per transmit channel (OUTx1±) are enabled, the serial data consists of an alternating “1010..” pattern and the RXCKSEL setting is LOW.

CYP(V)15G0402DXB Power Consumption

The power consumption of CYP(V)15G0402DXB when all four channels are enabled is shown in Figure 3 on page 5. This data represents the total power consumed when all receive channels (A, B, C and D) and output buffers (OUTx±) are enabled, the serial data consists of an alternating “1010..” pattern. This data is estimated from the basic set of measurements performed for CYP(V)15G0401DXB.

CYP(V)15G0101DXB Power Consumption

The power consumption of CYP(V)15G0101DXB when all channels are enabled is shown in Figure 4 on page 5. This data represents the total power consumed when the receive channel and one output buffer in the transmit channel (OUT1±) are enabled, the serial data consists of an alternating “1010..” pattern and the RXCKSEL setting is MID.

CYP(V)15G0201DXB Power Consumption

The power consumption of CYP(V)15G0201DXB when both channels are enabled is shown in Figure 5 on page 6. This data represents the total power consumed when both receive channels (A and B) and one output buffer in each transmit channel (OUTx1±) are enabled, the serial data consists of an alternating “1010..” pattern and the RXCKSEL setting is MID. This data is estimated from the basic sets of measurements performed for CYP(V)15G0101DXB and CYP(V)15G0401DXB.

Figure 3. Power Consumed by CYP(V)15G0402DXB When All Channels are Enabled

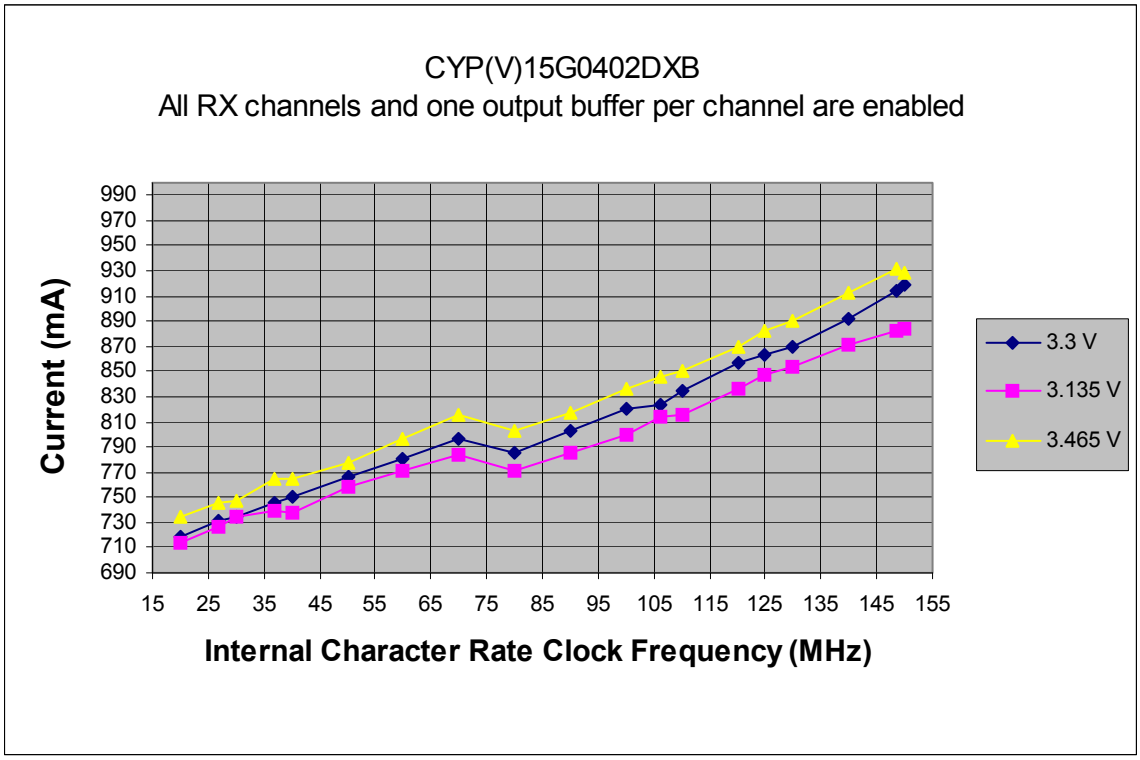


Figure 4. Power Consumed by CYP(V)15G0101DXB When All Channels are Enabled

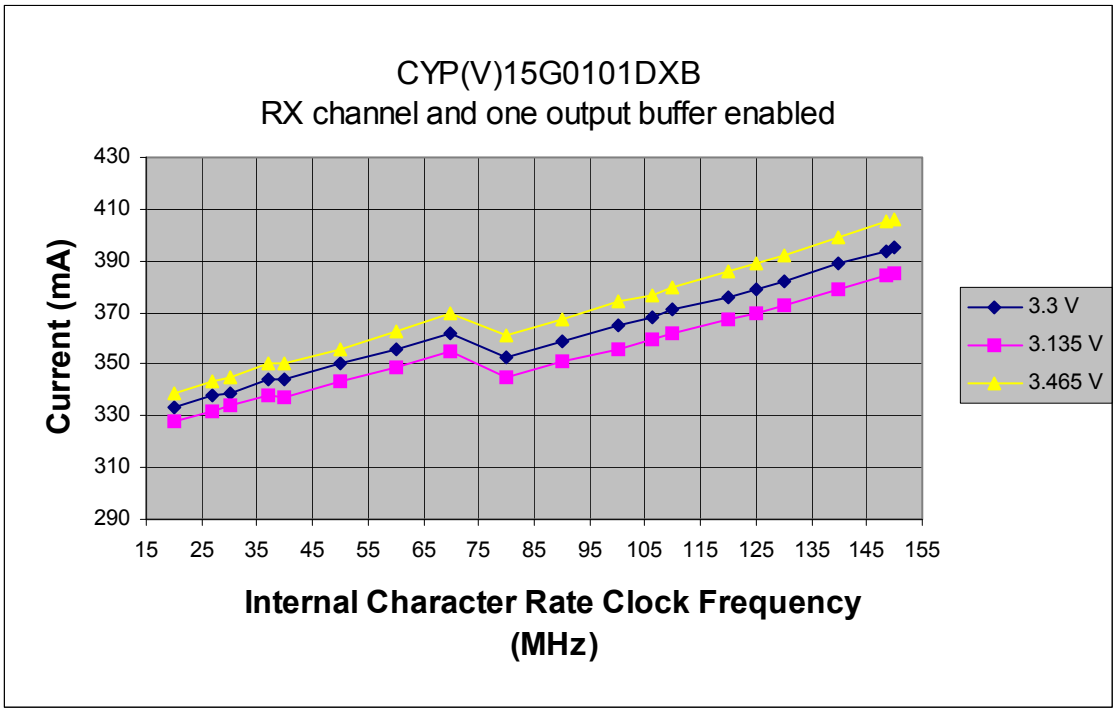
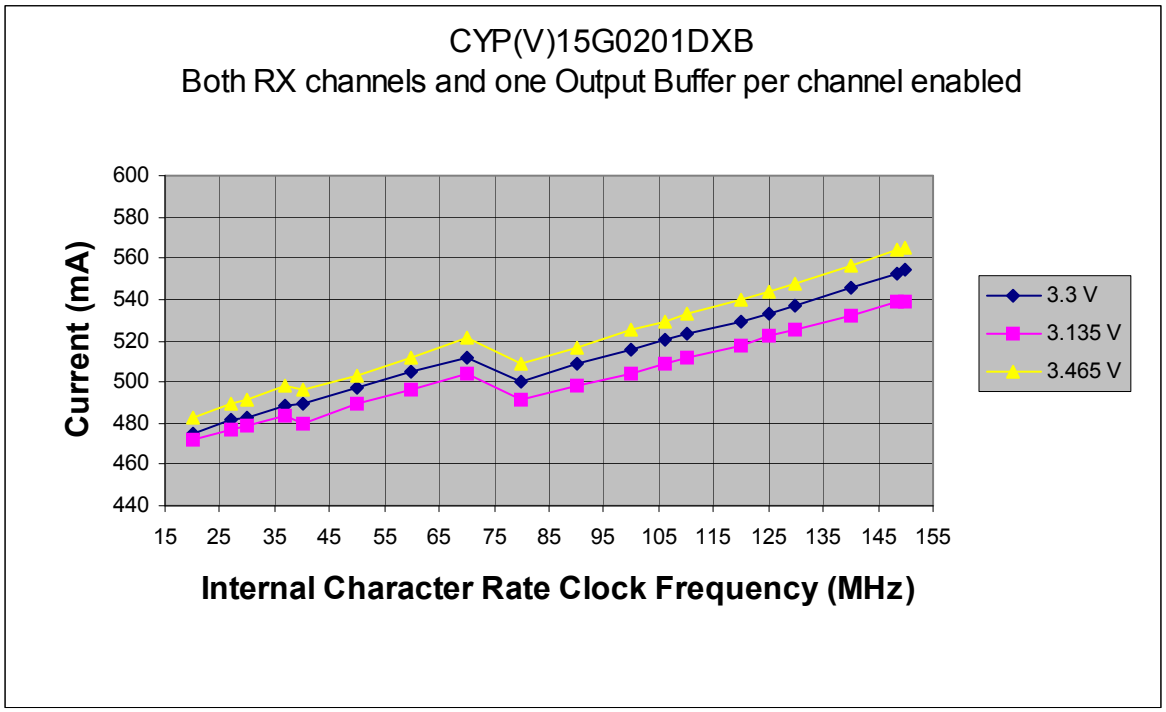


Figure 5. Power Consumed by CYP(V)15G0201DXB When Both Channels are Enabled



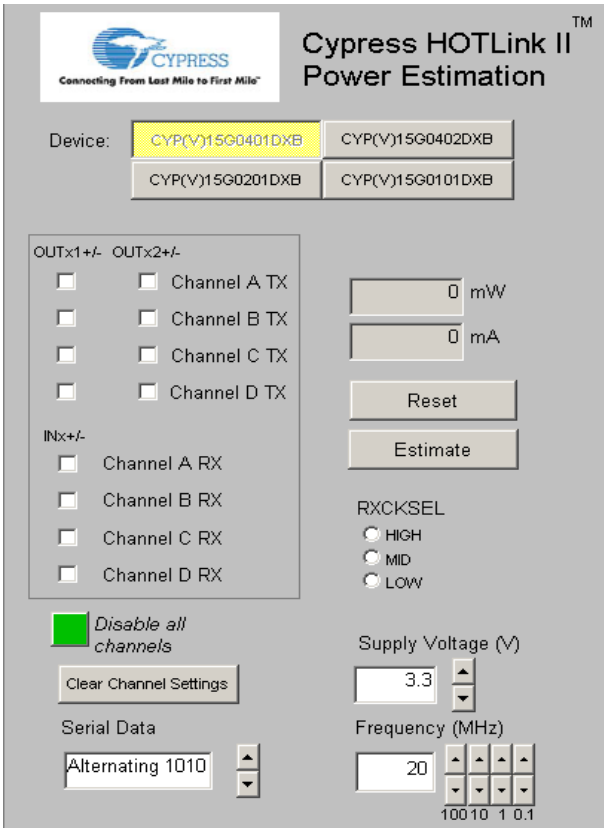
Instruction Guide for Using Power Estimator

This section of the application note focuses on the features of the Cypress HOTLink II™ Power Estimation GUI and provides instructions on how to use it.

After opening the downloaded file, when prompted, select “Enable Macros” to enable the GUI Functions. A screenshot of the GUI is shown in Figure 6 on page 7.

All power numbers are estimated from a basic set of measurements performed for CYP(V)15G0401DXB and/or CYP(V)15G0101DXB at room temperature with parallel outputs unloaded. The estimated measurements were found to be within ±5% of bench measurements.

Figure 6. Screenshot of the Power Estimation GUI



Selecting the Device

One of the four devices in the HOTLink II family can be selected by clicking on the buttons for device selection in the top of the GUI.

Selecting the Output Buffers that are Enabled

Once the device is selected, select the output buffers that will be enabled in the application. This is done by placing a check mark in the desired check box next to the appropriate output buffer. Note that CYP(V)15G0402DXB does not support a second pair of output buffers per channel, so these options will not appear. Also note that CYP(V)15G0201DXB and CYP(V)15G0101DXB have only two and one transmit channels, respectively.

Selecting the Receive Channels that are Enabled

The receive channels are enabled by placing check marks in the check boxes provided for them.

Disabling All Channels

The green colored button named “Disable all channels” is used to calculate the power of the device when all channels are disabled. All transmit and receive channel enable settings will be disabled when this button is pressed once. One more mouse click will again allow the user to select the desired channels.

Clearing Channel Settings

When this button is clicked, all check boxes are cleared.

Serial Data

This selection box is used to obtain a power estimate for two possible types of serial data:

1. Alternating 1010.

In this case, the data at the serial inputs and outputs is a repetitive clock like pattern of ‘1’ followed by ‘0’.

2. PRBS data.

In this case the data at the serial inputs and outputs is a repetitive pattern of serial data that corresponds to the HOTLink BIST pattern fed from another HOTLink II device.

The power in the PRBS case will be higher since the parallel outputs will be switching at a fast rate.

The selection of the option for type of serial data is made by using the scroll arrows near the “Serial Data” selection box.

RXCKSEL Setting

The RXCKSEL setting determines which clock is used to clock the output character in each channel. The RXCKSEL setting also determines which clock outputs are enabled or disabled. Hence, the power consumption will vary depending on the number of active receive channels and the RXCKSEL setting.

RXCKSEL Setting for CYP(V)15G0401DXB

When RXCKSEL is MID, the output character in each channel is clocked out using the recovered character rate clock in the corresponding channel. In this case RXCLKx± (x = A, B, C or D) in each channel outputs a clock signal that follows the recovered clock of the corresponding channel. In this mode, the RXCLKx± is disabled whenever the channel is disabled.

When RXCKSEL is LOW, the output characters on all channels are clocked out using a buffered version of the local REFCLK. In this case, RXCLKA± and RXCLKC± present a buffered version of the REFCLK with different delays. RXCLKB+ and RXCLKD+ will act as control inputs. RXCLKB– and RXCLKD– are in High Z state. In this mode RXCLKA± and RXCLKC± present a buffered version of REFCLK irrespective of any channel being enabled or disabled.

When RXCKSEL is HIGH, output characters from all channels are clocked by the selected recovered clock. This selection is made using the RXCLKB+ and RXCLKD+ signals as inputs. These selected clocks are always output on

RXCLKA± and RXCLKC±. RXCLKB- and RXCLKD– are in High Z state.

RXCKSEL Setting for CYP(V)15G0402DXB

There is no RXCKSEL setting for CYP(V)15G0402DXB. The output character in each channel is clocked out using the recovered character rate clock in the corresponding channel. RXCLKx± (x = A, B, C or D) in each channel outputs a clock signal that follows the recovered clock of the corresponding channel. RXCLKx± is disabled whenever the channel is disabled.

RXCKSEL Setting for CYP(V)15G0201DXB

When RXCKSEL is MID, the output character in each channel is clocked out using the recovered character rate clock in the corresponding channel. In this case RXCLKx± (x = A or B) in each channel outputs a clock signal that follows the recovered clock of the corresponding channel. In this mode, the RXCLKx± is disabled whenever the channel is disabled.

When RXCKSEL is LOW, the output characters on both channels are clocked out using a buffered version of the local REFCLK. In this case, RXCLKA± and RXCLKC+ present a buffered version of REFCLK with different delays. RXCLKB+ acts as a control input. RXCLKB– is in High Z state. In this mode, RXCLKA± and RXCLKC+ present a buffered version of REFCLK irrespective of any channel being enabled or disabled.

When RXCKSEL is HIGH, output characters for both channels are clocked by the recovered clock as selected by the RXCLKB+ input. This selection is made using the RXCLKB+ as input. This selected clock is output on RXCLKA± and RXCLKC+. RXCLKB– is in High Z state.

RXCKSEL Setting for CYP(V)15G0101DXB

When RXCKSEL is MID, the output character in the receive channel is clocked out using the recovered character rate clock. RXCLKA± outputs a clock signal that follows the recovered clock. In this mode, the RXCLKA± is disabled whenever the receive channel is disabled.

When RXCKSEL is LOW, the output characters are clocked out using a buffered version of the local REFCLK. In this case, RXCLKA± and RXCLKC+ present a buffered version of the REFCLK with different delays. In this mode, irrespective of receive channel being enabled or disabled RXCLKA± and RXCLKC+ present a buffered version of REFCLK.

RXCKSEL being HIGH is an invalid option for CYP(V)15G0101DXB.

Supply Voltage

The power supply voltage can be selected as either 3.135 V (3.3 V – 5%), 3.3 V or 3.465 V (3.3 V + 5%) by using the scrolling arrows next to the “Supply Voltage” selection box.

Frequency

The operating frequency can be either manually typed in or selected using the scroll bars next to the “Frequency” entry box. The operating frequency is the frequency of the internal character rate clock, in other words, it is the divide-by-10 frequency of the serial data rate. It will be same as the REFCLK frequency if TXRATE = LOW and twice REFCLK frequency if TXRATE = HIGH.

Estimation of Power

Once all the selections have been made, an estimate of the power consumed can be obtained by clicking on the “Estimate” button. The current drawn is displayed in milliAmperes (mA). The power consumed (supply voltage × current) is also displayed in milliwatts (mW).

Summary

The power saving mechanisms of the HOTLink II family of devices are discussed. The power consumption characteristics of the CYP(V)15G0401DXB, CYP(V)15G0402DXB, CYP(V)15G0201DXB and CYP(V)15G0101DXB are illustrated. The instructions for the HOTLink II power estimation GUI are also provided.

For additional support, please contact Cypress Support at http://www.cypress.com/support or call Cypress Applications Support USA at 1-800-541-4736.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1009380	NVNS	04/23/2007	Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date Please post in the web- overwrite the existing AN027 file
*A	3248216	NVNS	05/04/2011	Updated in new template.
*B	4384630	NVNS	05/20/2014	No technical updates. Completing Sunset Review.

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