AIROC™ CYW20706 Bluetooth® & Bluetooth® LE system on chip hardware design guidelines

About this document

Scope and purpose

This document provides guidance on how to design your hwardware with CYW20706.

Intended audience

This document is intended for hardware engineers creating PCB layout designs with CYW20706.

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1 Introduction

This document provides basic guidelines on the layout for the CYW20706. This document is divided into the following sections.

- Basic layout guidelines which include the board stackup and impedance control requirements
- Component placements and recommended parts for critical components
- Routing guidelines and the recommended trace width for various power traces

2 Basic layout guidelines

Most Bluetooth® devices use four-layer boards to minimize thickness. Components are placed on the top layer; the top layer will also have the signal fanout from the CYW20706 chip. The second layer is a solid ground fill, power traces are routed on the third layer, and lastly, the digital signals as well as additional power traces that couldn't be routed on the third layer can be routed on the bottom layer.

For RF traces, use a 50-ohm transmission line to minimize mismatch losses and reflections, and therefore maximize the power transferred to the load. There are two types of transmission lines: microstrip and stripline. The reference design uses the microstrip design.

Transmission lines require a proper geometry. Some parameters are highly dependent on the dielectric material, trace width, vertical distance to the ground plane, and a solid ground plane as the reference. Different height and width solutions perform differently.

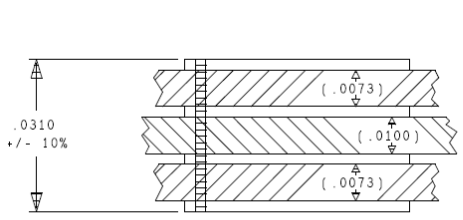
For the microstrip layer and its reference ground layer selections, two things should be considered:

- Thinner traces have higher insertion loss – PCB fabrication requires adequate trace width for reliability and repeatability. Heights between the microstrip and ground should be maintained per the stack up shown in Figure 1 to maintain 50-ohm impedance control.
- For microstrip lines, avoid sharp corners; use a smooth radius to change directions. The coplanar ground follows the contour of these traces with a clearance of two to three-line widths (2 W to 3 W). Connect the outer layer to the reference ground plane using vias so that they surround the microstrip trace.

The microstrip used in this reference design is on Layer 1 with a trace width of 12.5 mils. The reference ground is Layer 2.

This reference design uses a four-layer PCB with a stackup as shown in Figure 1:

- Layer 1: Components and main signal layer
- Layer 2: Solid ground layer
- Layer 3: Power signal layer
- Layer 4: Digital signal layer. Additional power signals that could not be routed on Layer 3 can be routed here as well. However, ensure that they do not overlap any of the power signals on Layer 3.



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER	CPW SPACE	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER	CPW SPACE
L01 - TOP	0.5 OZ	50	.0125	2	-----	---	.-----/.-----	---	-----
L02 - PLANE	0.5 OZ	--	-----	---	-----	---	----	---	-----
L03 - PLANE	0.5 OZ	--	-----	---	-----	---	----	---	-----
L04 - BOTTOM	0.5 OZ	--	.-----	---	-----	---	.-----/.-----	---	-----

STACK-UP (DIMENSIONS IN INCHES)

Figure 1 Typical board stackup used for CYW20706

3 Component placement

As a rule, follow the receive signal flow from the antenna to the antenna-matching and filter circuits, then to the low-noise amplifier (LNA) chip input. Keep radio front end (RF), power management unit (PMU), and baseband (BB) decoupling capacitors as close to the CYW20706 pins as possible.

3.1 Bypass capacitor placement

The following schematic design shows the PMU and the RF front end section. When making determinations about the part placements on the PCB, the following requirements must be met:

- VBAT input(Pin D1) must have a 2.2-µF (C8) capacitor placed as close to the pin as possible.
- VPA_BT input(Pin E1) must have a 2.2-µF (C9) capacitor placed as close to the pin as possible.
- VDDC_LDO1P2(Pin F1) must have a 1-µF (C10) capacitor placed as close to the pin as possible.
- VDDPA, which consist of VOUT_BTVDD2P5 (Pin E2) and BT_PAVDD2P5 (Pin A1), must have a 2.2-uF (C11) and a 10-pF(C12) capacitors placed as close to the pins respectively.
- BT_PLLVDD1P2 (Pin A3), BT_IFVDD1P2(Pin B4), BT_LNAVDD1P2 (Pin B1) and BT_VCOVDD1P2 (Pin C1) must have a 1-uF capacitor (C13, C14, C15, C16) placed as close to the pins respectively. If board space is limited, Pin A3 and Pin B4 share one 1-uF capacitor, Pin B1 and Pin C1 share one 1-uF capacitor.

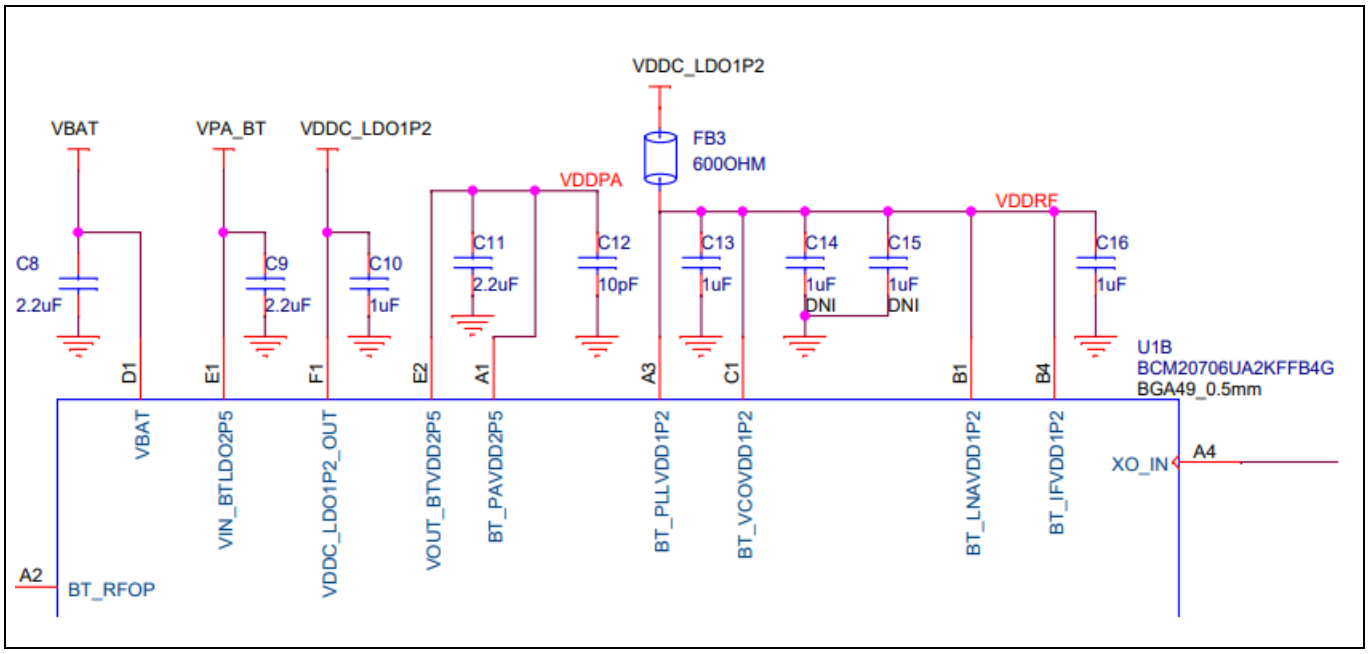


Figure 2 Bypass capacitors in the PMU and RF front end area

In the baseband area, the following component placement must also be met:

- BT_OTP_VDD3P3V (Pin G1) must have 1-µF capacitor placed as close to the pin as possible.
- BT_VDDC-1 (Pin G6) and BT_VDDC-2 (Pin B8) have a 1-µF capacitor for each pin, and they must be placed as close to the pin as possible.
- BT_VDDO (Pin G5) must have a 0.1-µF capacitor placed as close to the pin as possible.

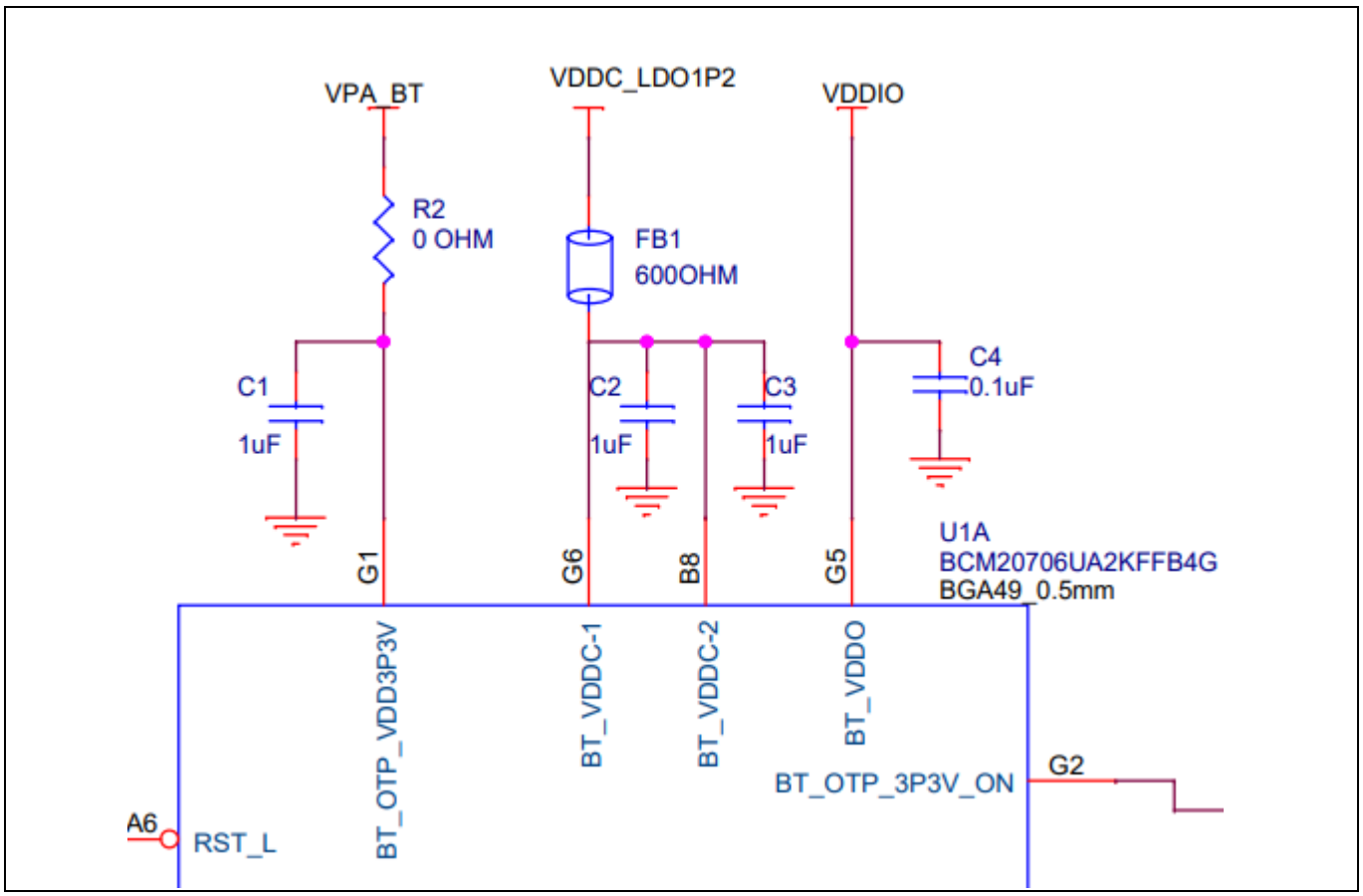


Figure 3 Bypass capacitor in the baseband area

3.2 Antenna placement

Keep the antenna connection to the device as short as possible. Maintain a solid ground near the antenna and adequate ground clearance for the layers beneath the antenna.

In the reference design, the antenna is on the top layer on the left of the board next to the CYW20706 chip.

For more details on PCB antennas, see AN91445 - Antenna design and RF layout guidelines. For the associated Gerber file, click https://www.infineon.com/dgdl/Infineon-AN91445_Antenna_Design_Guide-ApplicationNotes-v09_00-EN.zip?fileId=8ac78c8c7cdc391c017d073e1c866233s.

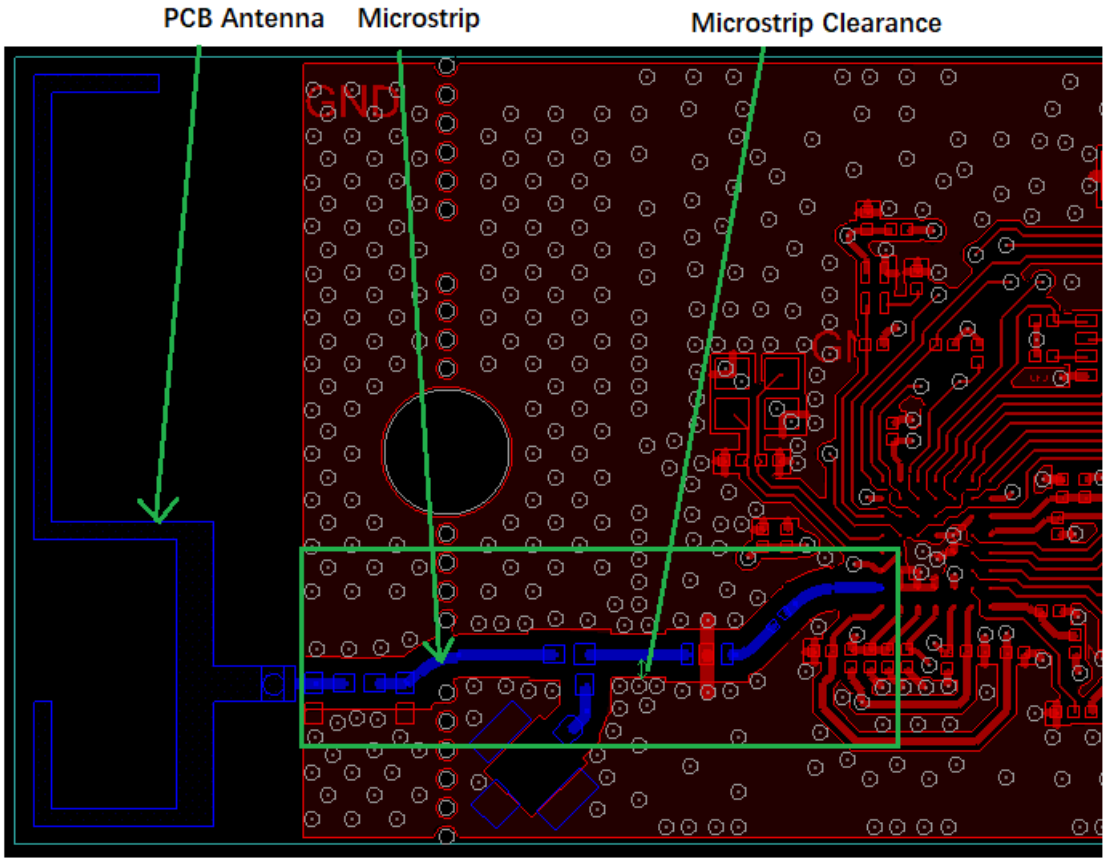


Figure 4 Antenna placement and microstrip clearance

3.3 Bandpass filter

Place a chip bandpass filter between the antenna-matching components and the CYW20706 device to attenuate harmonics from CYW20706. The recommended part is either Murata LFB182G45CL3D178 or TDK DEA162450BT-1288B1BR. A microstrip is used for all connections of the bandpass filter.

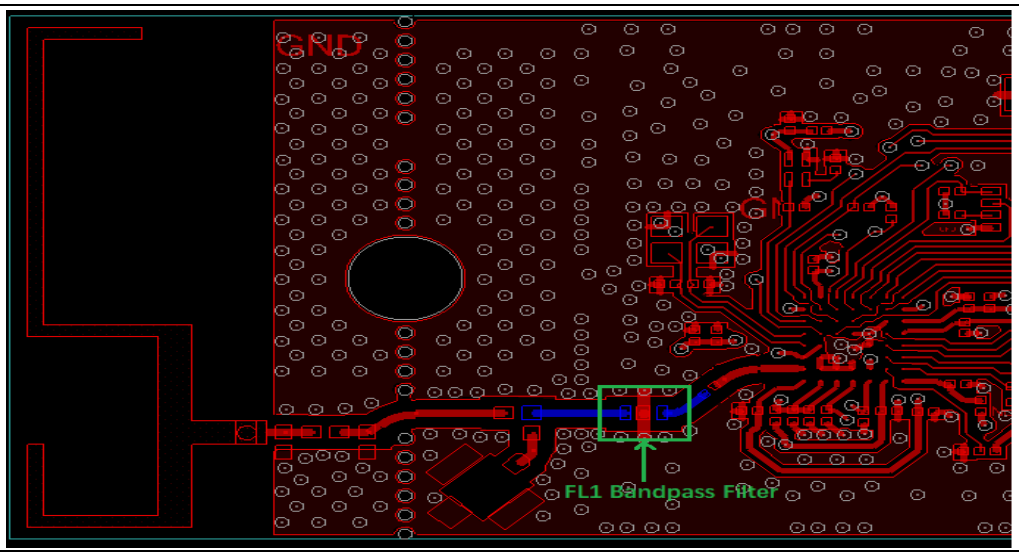


Figure 5 Bandpass filter placement

3.4 Crystal placement

Protect the crystal and related traces from noise sources and use a solid ground to separate the crystal from RF traces. The crystal ground plane should have direct vias to the reference ground plane.

The load capacitors placement as shown in Figure 6 is recommended, because this placement uses the least amount of PCB trace to connect the CYW20706 chip; the crystal and the load capacitors together which will minimize the parasitic capacitance.

See the CYW20706 datasheet for crystal specifications and requirements. See References.

The recommended crystal is TXC 7R24070007.

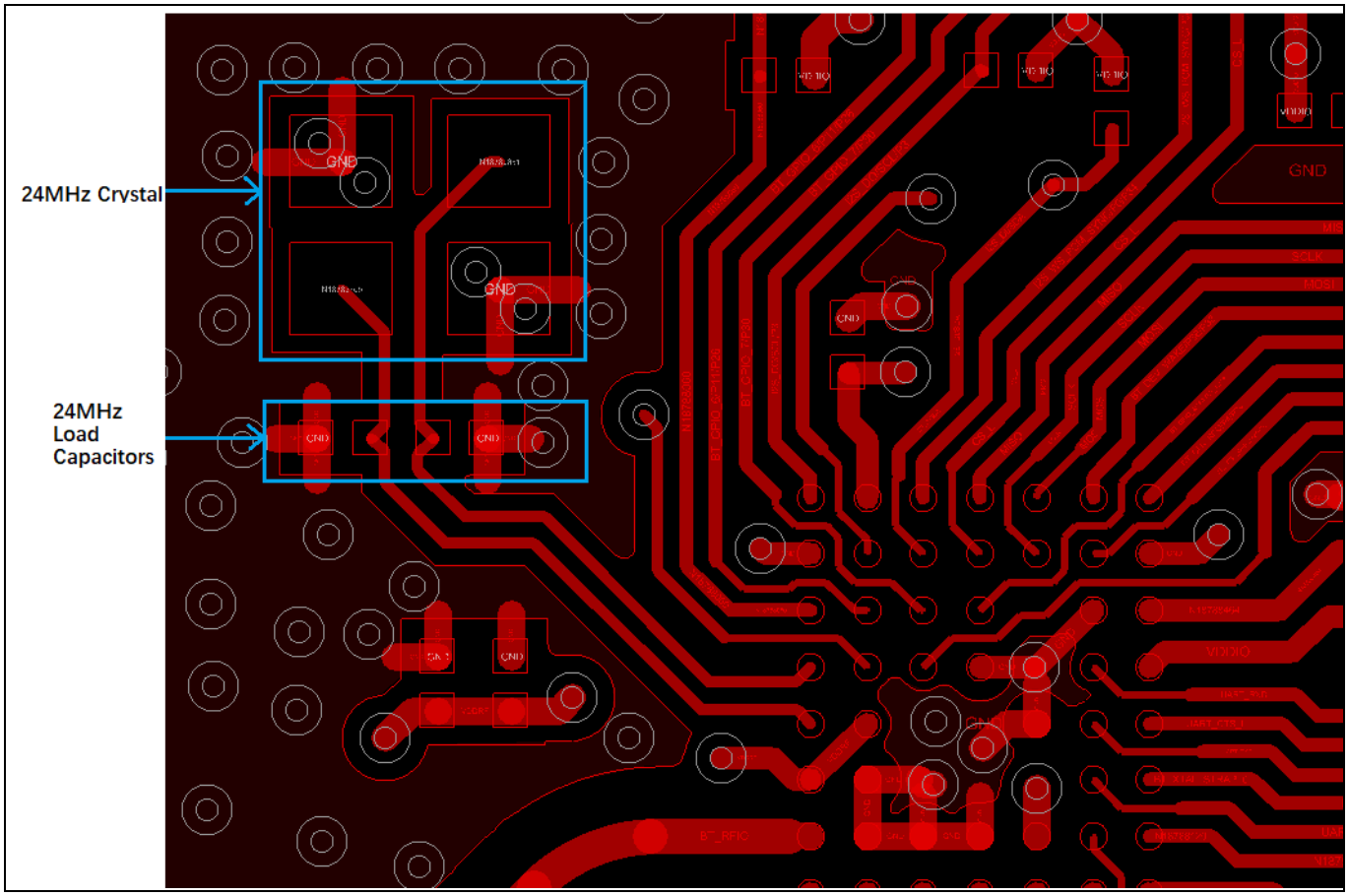


Figure 6 24-MHz crystal placement

4 PCB layers and routing

4.1 Ground vias

Do not use long thin traces to connect components to ground vias; doing so adds inductance that can significantly alter circuit performance. Instead, place the vias directly on the ground pads of the components. Do not use through hole vias on the pins of the CYW20706 chip; instead, use 1:2 laser vias to connect the ground pads directly to the main ground. Only use through-hole vias in the open area to stitch the ground plane on all layers together.

4.2 Layer 1: Components, signal fanout, and RF trace

All the passive components for the chip can be placed on the top layer. Signal fanout from the CYW20706 chip will also be done on the top layer.

The RF trace, shown as blue, must be well isolated and have a solid ground plane along both sides of the trace.

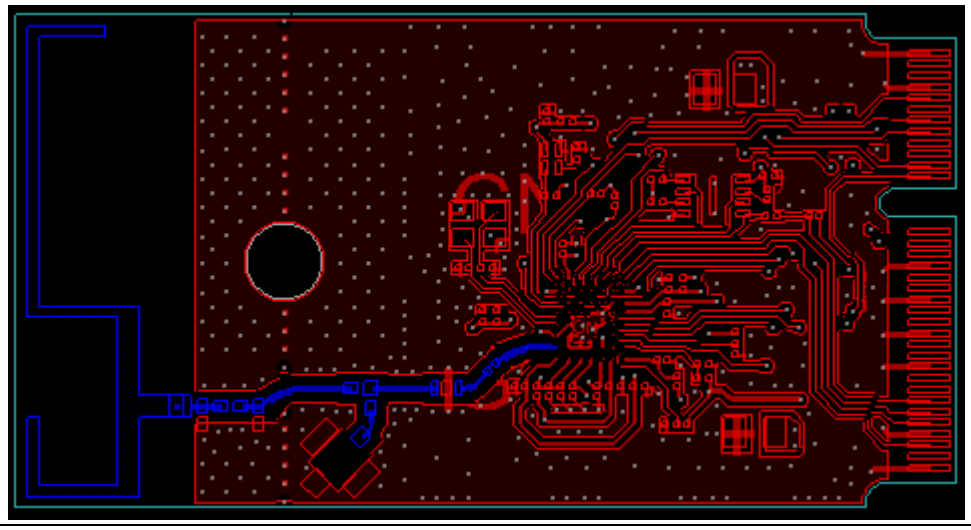


Figure 7 Layout 1, components and signal fanout

4.3 Layer 2: Solid ground plane

Fill the layer immediately below the layer where CYW20706 is located with solid ground plane for optimal ground return path.

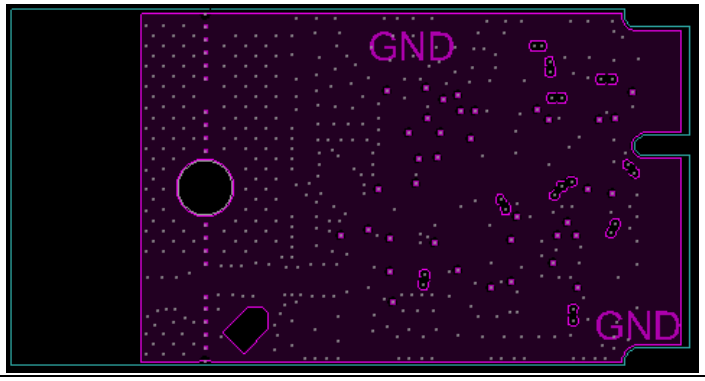


Figure 8 Layer 2, solid ground fill

4.4 Layer 3: Power traces

- Route the main DC power supply line up the middle of the board like a spine, branching off left and right as needed.
- Avoid routing DC power in a loop.
- Consider the current flow when routing the power traces to the chip. For input power pins, make sure the power trace goes through the decoupling capacitors before going into the power pin. For output power pins, make sure that the power trace goes to the decoupling capacitors immediately before going to the load.
- Protect the RF power supply from main power, noisy signals, and digital power by separating with ground fill.
- Ensure that adequate power trace width and vias are available to minimize parasitic impedance.
- Recommended trace width for the power signals are as follows:
  - VBAT (Pin D1) → Minimum 10-mils trace width
  - VPA_BT to pin VIN_BTLDO1P2_OUT (Pin E1) → Minimum 10-mils trace width
  - VDDC_LDO1P2_OUT (Pin F1) → Minimum 10-mils trace width
  - BT_PLLVDD1P2 (Pin A3)/BT_VCOVDD1P2 (Pin C1)/BT_VCOVDD1P2 (Pin B1)/ BT_IFVDD1P2 (Pin B4) → Minimum 8-mils trace width
  - BT_VDDC-1 (Pin G6)/ BT_VDDC-2 (Pin B8) → Minimum 8-mils trace width
  - BT_VDDO (Pin G5) → Minimum 8-mils trace width
  - VOUT_BTVDD2P5 (Pin E2) to BT_PAVDD2P5 (Pin A1) → Minimum 10-mils trace width

Note: The trace width can be decreased to 8 mil to adapt the limited space near BGA pads.

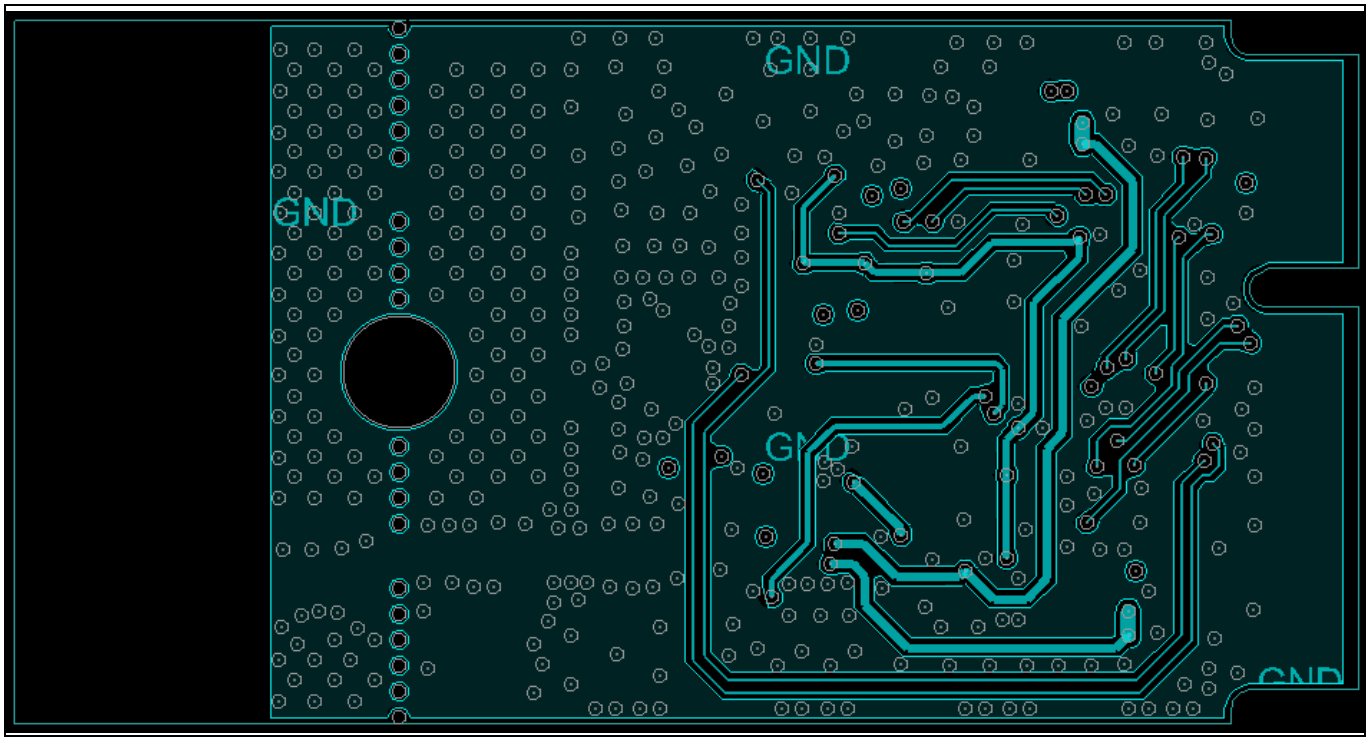


Figure 9 Power supply traces on layer 3

4.5 Layer 4: Power traces and non-critical signals

Use Layer 4 for all non-critical signal routing as well as additional power traces that could not be routed on Layer 3. Ensure that the power traces routed on Layer 4 do not cross with the power traces that are on Layer 3.

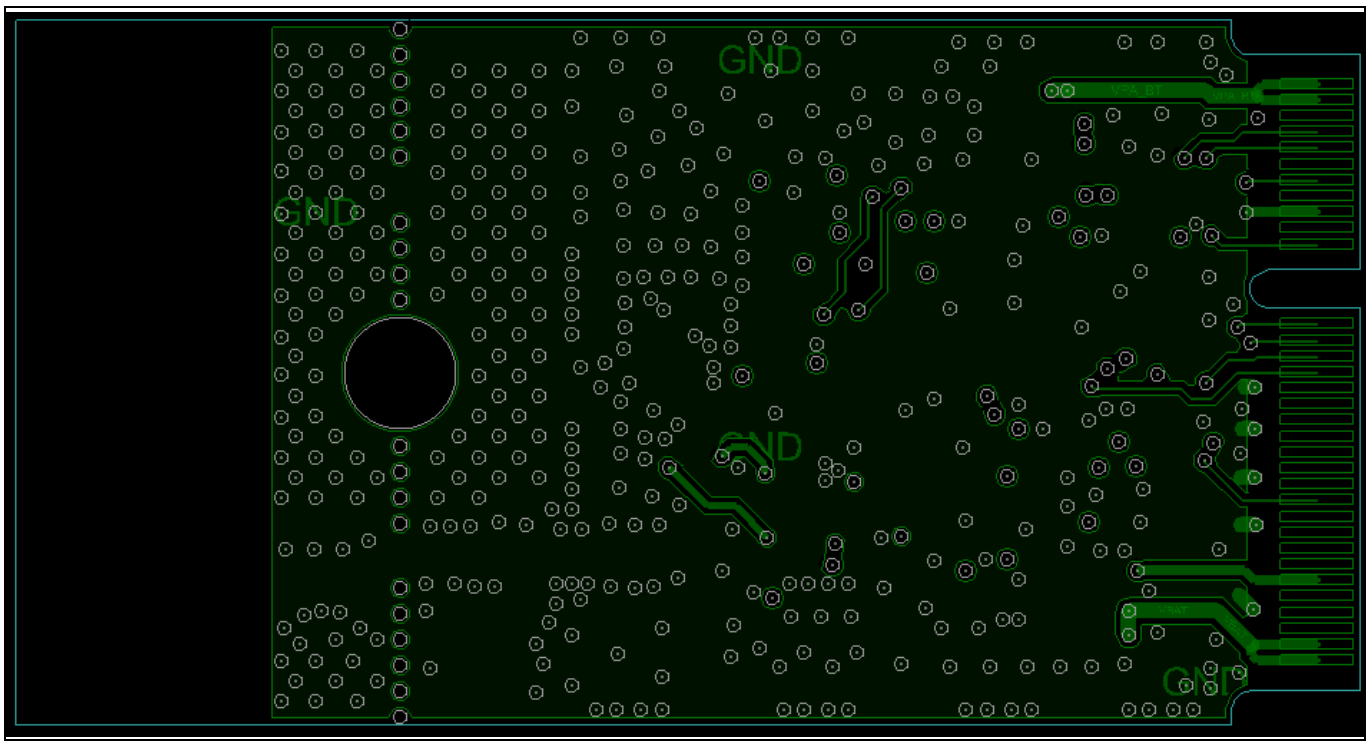


Figure 10 Layer 4, power traces and non-critical signal

References

A wealth of data is available at www.infineon.com to help you to select the right device, and quickly and effectively integrate the device into your design.

[1] Datasheets

- CYW20706

[2] Application note

- Antenna design and RF layout guidelines

Revision history

Document revision	Date	Description of changes
**	2023-03-02	Initial release.

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