Trim and Margin code example with PSoC™3/PSoC™ 5LP

About this document

Scope and purpose

This code example demonstrates the basic operation of the Trim and Margin Component in PSoC™ Creator.

Intended audience

The intended audience for this document are design engineers, technicians, and developers of electronic systems.

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1 Overview

This code example shows how the Trim and Margin Component runs on PSoC™ 3 and PSoC™ 5LP devices. It is intended for use with the CY8CKIT-030 PSoC™ 3 development kit (DVK) or CY8CKIT-050 PSoC™ 5LP DVK and the CY8CKIT-035 PSoC™ Power Supervision expansion board kit (EBK). The example project consists of the Trim and Margin, Power Monitor, Status Register, Control Register, and Character LCD Components.

The Power Monitor Component is configured to monitor the output voltages of the four power converters installed on the CY8CKIT-035 board for display on the LCD. The Trim and Margin Component is used to adjust the power converter output voltages by pressing the two switches on the DVK. These switches are also used to turn off/on the power converters. The Control Register Component is used to control the power-up sequence of the power converters. The Character LCD Component displays the measured and desired voltage for the selected rail. It also displays the current duty cycle of the internal Trim and Margin Component's PWM of the selected rail.

2 Requirements

Tool: PSoC™ Creator 3.2 SP1

Programming language: C (GCC 4.8.4 or later)

Associated parts: All PSoC™ 3 and PSoC™ 5LP parts

Related hardware: CY8CKIT-030, CY8CKIT-050, CY8CKIT-035

3 Design

The code example consists of the Trim and Margin, Power Monitor, Control Register, Status Register, and Character LCD Components. Figure 1 shows the design schematic. The blue annotated block in the middle of the schematic shows the components that are installed on the PSoC™ Power Supervision EBK, most notably the power converters and the components used for trimming and margining. The Power Monitor Component and the associated Status Registers are used to measure the power converter output voltages, which are then displayed on the Character LCD. The Control Register is used to control the power-up sequence of the power converters.

The four power converter enables are mapped to PSoC™ GPIO pins P3[4], P3[5], P3[6], and P3[7] respectively. The four PWM pseudo-DAC outputs from the Trim and Margin Components are mapped to PSoC™ GPIO pins P0[0], P0[1], P0[2], and P0[3] respectively. The four power converter output voltages are mapped to PSoC™ GPIO pins P4[0], P4[2], P4[4], and P4[6] respectively.

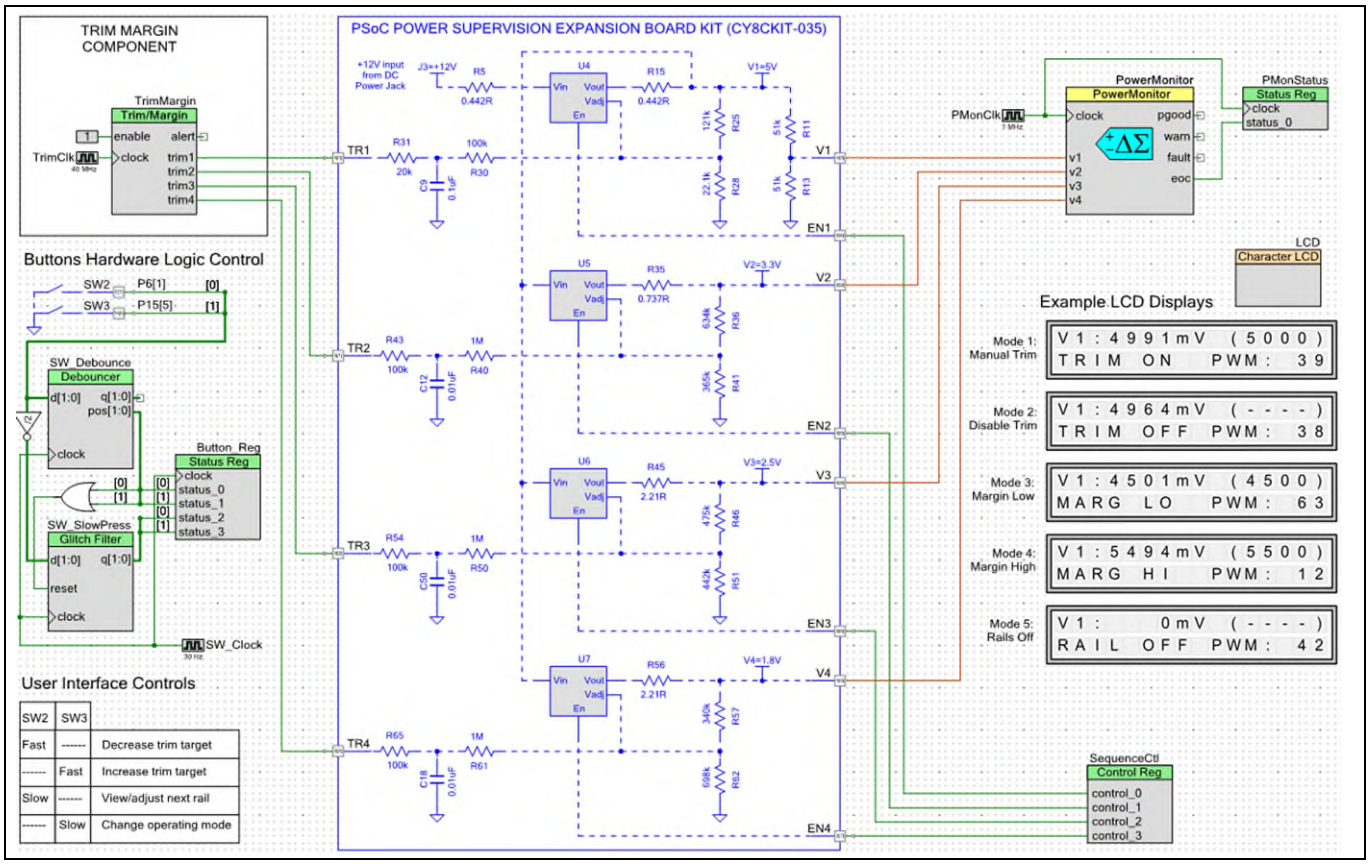


Figure 1 Example project power supervision schematic

The Debouncer Component prevents mechanical noise associated with pressing a switch, avoiding false triggering of a button press. The Glitch Filter Component works as a slow-press detector. A sticky status register with four bits is used to inform the CPU when the switches are pressed and how. The first two bits represent fast presses, and the other two bits represent slow presses on each switch. Fast and slow presses perform different functions in the design as discussed in the Operation section.

3.1 Design considerations

This design can be extended to a much larger scale system by simply adjusting the number of converters in the various Components and adding Pins Components to the design.

4 Hardware setup

1. Configure the PSoC™ DVK to 5-V operation by setting jumpers J10 and J11 to position 2-3.
2. If using a CY8CKIT-050, remove the SAR bypass jumpers J43 and J44.
3. Connect a USB cable to J1, and connect the other end to an available USB connection on a PC. Proceed to build and program the PSoC™ DVK. Do not connect the PSoC™ Power Supervision EBK until you have programmed the PSoC™ with one of the example projects.
4. Disconnect the USB cable from the PSoC™ DVK. Ensure the LCD module included with the PSoC™ DVK is mounted. Connect the Power Supervision EBK to Port E.
5. On the CY8CKIT-035, insert jumper J5 in position 1-2 and populate J6, J7, J8, J9, J10, J11, J12, and J13.
6. Connect the 12-V/3-A supply to J3 and connect the MiniProg3 to white connector J2 of the CY8CKIT-035.

5 Software setup

No special software setup is required to use this project.

6 Components

Table 1 lists the PSoC™ Creator Components used in this example, as well as the hardware resources used by each.

Table 1 PSoC™ Creator Components

Component	Hardware resources
Trim/Margin	Universal digital blocks (UDBs) (4x Datapath Cells, 1x Macrocell, 1x Control Cell)
Power monitor	1x PGA, 1x DelSig ADC, 1x ISR, UDBs (4x Macrocells, 2x Control Cells)
Character LCD	7x GPIOs
Debouncer	UDBs (5x Macrocells)
Glitch Filter	UDBs (2x Datapath Cells, 2x Macrocells)
Pins	GPIOs
Control register	UDBs (1x Control Cell)
Status register	UDB (2x Status Cells)

6.1 Parameter settings

The Trim and Margin and Power Monitor Components are configured to support the four power converters installed on the CY8CKIT-035. Figure 2, Figure 3, and Figure 4 show the Component Configuration Tools. The Character LCD is used in its default configuration. For more information on the use of the Character LCD, Control Register, and Status Register Components, refer to the corresponding Component datasheets.

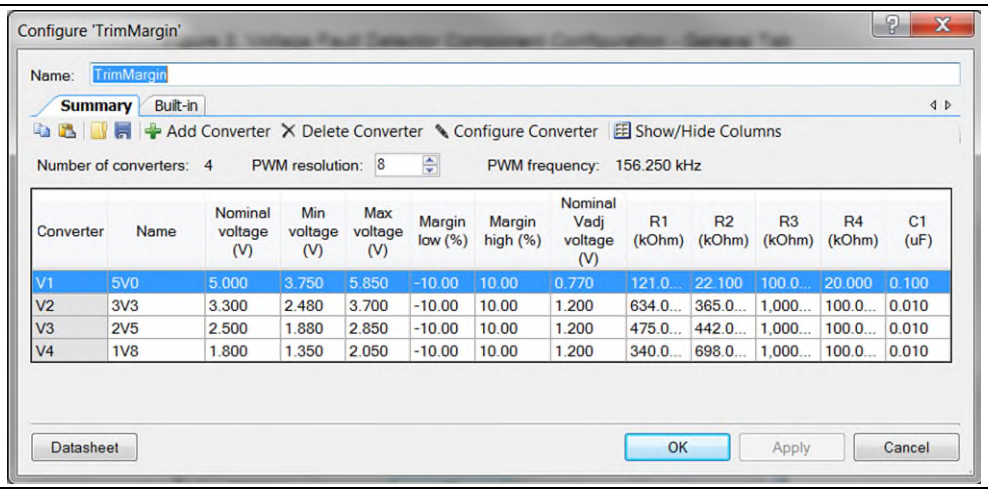


Figure 2 Trim and Margin Component configuration

Components

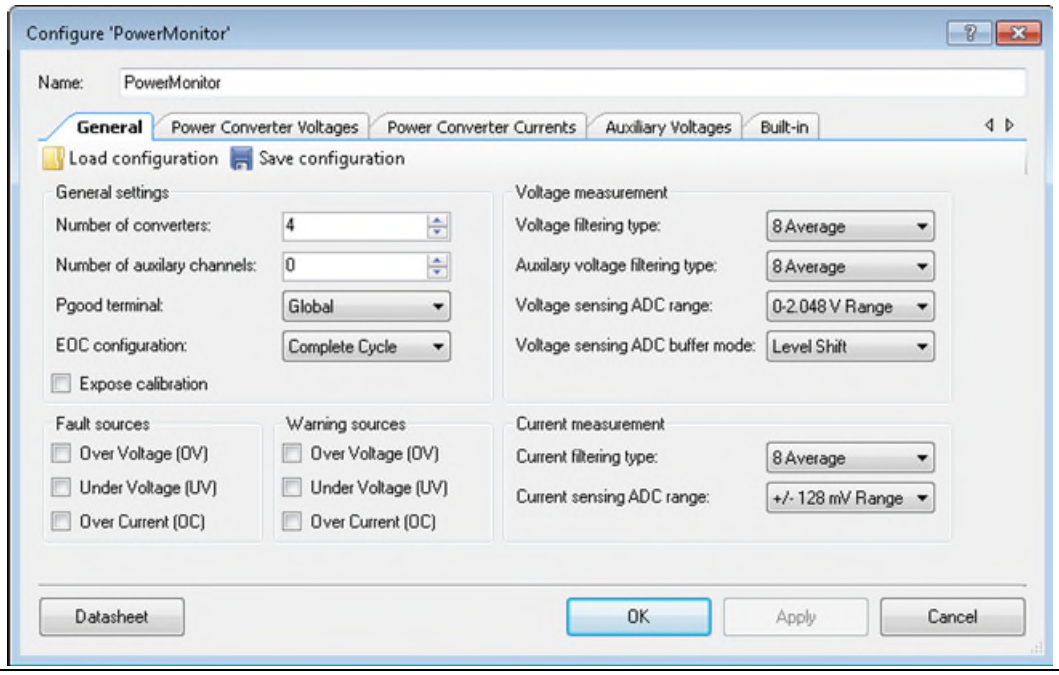


Figure 3 Power Monitor Component configuration – General tab

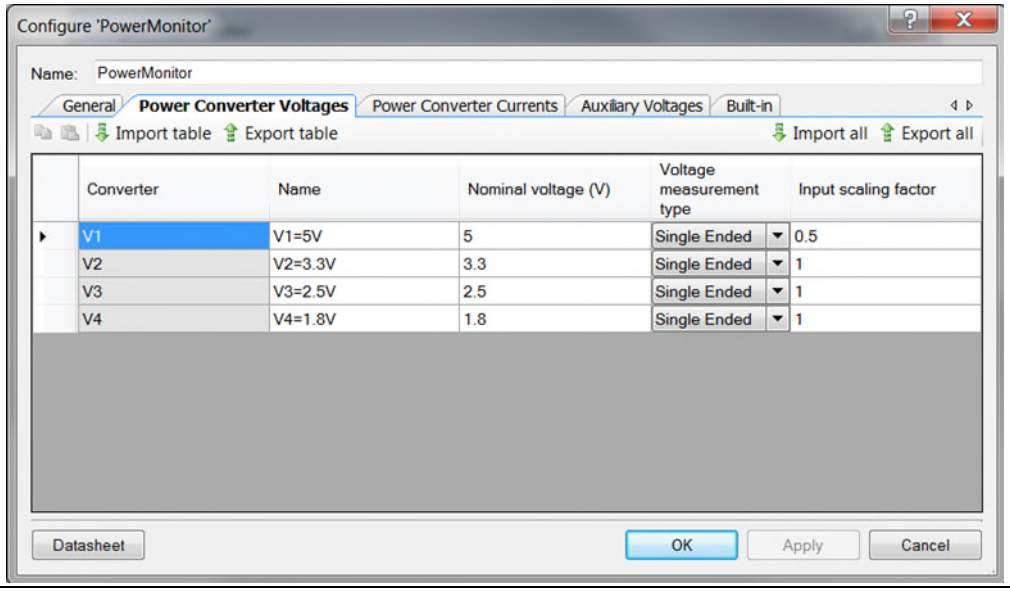


Figure 4 Power Monitor Component configuration – Power Converter Voltages tab

6.2 Design-wide resources

Figure 5 shows the pin selections for the project.

Alias	Name	Port	Pin	Lock
	\LCD:LCDPort[6:0]\	P2[6:0]	95..99,1..2	☑
	EN1	P3[4] OpAmp1:vminus	48	☑
	EN2	P3[5] OpAmp1:vplus	49	☑
	EN3	P3[6] OpAmp1:vout	51	☑
	EN4	P3[7] OpAmp3:vout	52	☑
	SW2	P6[1]	90	☑
	SW3	P15[5]	94	☑
	TR1	P0[0] OpAmp2:vout	71	☑
	TR2	P0[1] OpAmp0:vout	72	☑
	TR3	P0[2] OpAmp0:vplus	73	☑
	TR4	P0[3] OpAmp0:vminus, DSM:ext_pin_1	74	☑
	V1	P4[0]	69	☑
	V2	P4[2]	80	☑
	V3	P4[4]	82	☑
	V4	P4[6]	84	☑

Figure 5 Pin selections

7 Operation

On power up, the power converters on the Power Supervision EBK are turned on, and the Trim and Margin Component assists in regulating them to their nominal voltages. As shown in Figure 6, the LCD displays the measured and desired voltages of the selected power converter. It also displays the operating mode of the example project and the duty cycle of the PWM output that adjusts the power converter output voltage.

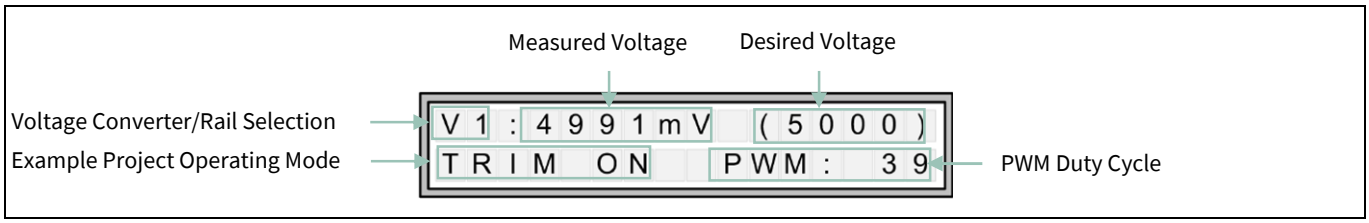


Figure 6 Character LCD display configuration

References

[1] 001-94248: PSoC™ Creator Component datasheet-Power Monitor

[2] 001-89124: PSoC™ Creator Component datasheet-Trim and Margin

Revision history

Document revision	Date	Description of changes
**	2015-07-03	New code example
*A	2023-02-15	Migrated to Infineon template Removed SMC app note references

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