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CE223549 – PSoC 6 MCU IPC Semaphore

Objective

This example demonstrates how to use the inter processor communication (IPC) driver to implement a semaphore in PSoC® 6 MCU. The semaphore is used as a lock to control access to a resource shared by the CPUs.

Requirements

Tool: PSoC Creator™ 4.2; Peripheral Driver Library (PDL) 3.1.0

Programming Language: C (Arm® GCC 5.4.1 and Arm MDK 5.22)

Associated Parts: All PSoC 6 MCU parts with dual CPUs

Related Hardware: CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit and CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit

Overview

In this example, both CPUs in PSoC 6 MCU share the UART hardware block to send messages to the computer. An IPC semaphore controls the access to the UART to avoid situations where both CPUs attempt to send messages at the same time. The example also provides an option to disable the semaphore to observe how it affects the system. The red LED on the kit indicates whether the semaphore is being used.

Hardware Setup

This example uses the kit's default configuration. Refer to the kit guide to ensure the kit is configured correctly.

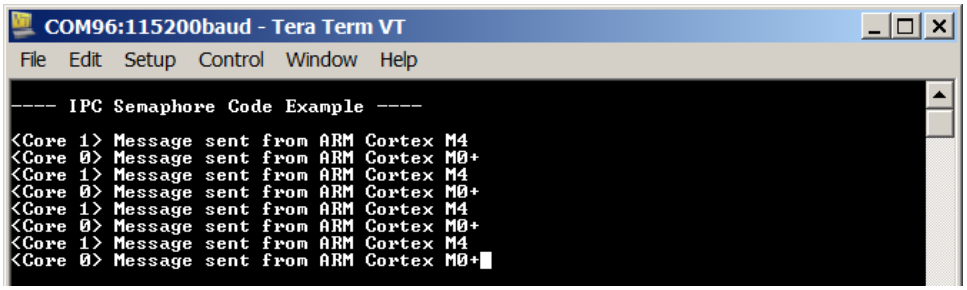
Software Setup

If necessary, install a terminal emulator like Tera Term or PuTTY on your personal computer. The example uses the terminal window to display messages.

Operation

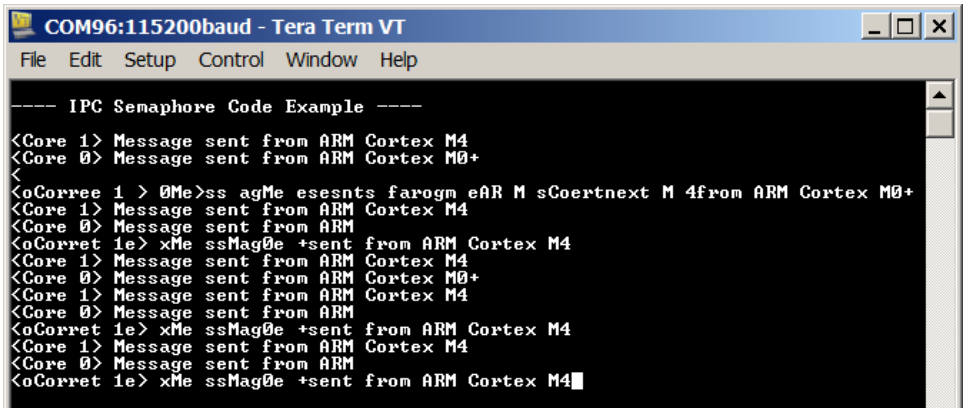
1. Plug the CY8CKIT-062 kit board into your computer's USB port.
2. Build the project and program it into the PSoC 6 MCU device. Choose **Debug** > **Program**. For more information on device programming, see PSoC Creator Help. Flash for both CPUs is programmed in a single program operation.
3. Open a serial port communication program such as Tera Term and select the corresponding COM port. Configure the terminal with 115200 baud rate, 8 data bits, 1 stop bits, and with parity and flow control set to none.
4. Press the SW2 switch on the kit. The terminal prints messages from both cores without any conflicts, as shown in Figure 1. Messages are printed every time you press the switch.

Figure 1. Terminal Prints Using Semaphore



5. Set the **#define SEMA_ENABLE** to 0u in the main_cm0p.c file at line 41. Recompile the project and program it into the PSoC 6. The red LED in the board should be ON, indicating that the semaphore is not used in the CM0+.
6. Press the SW2 switch on the kit. The terminal will print messages from both CPUs, but with conflicts, as shown in Figure 2.

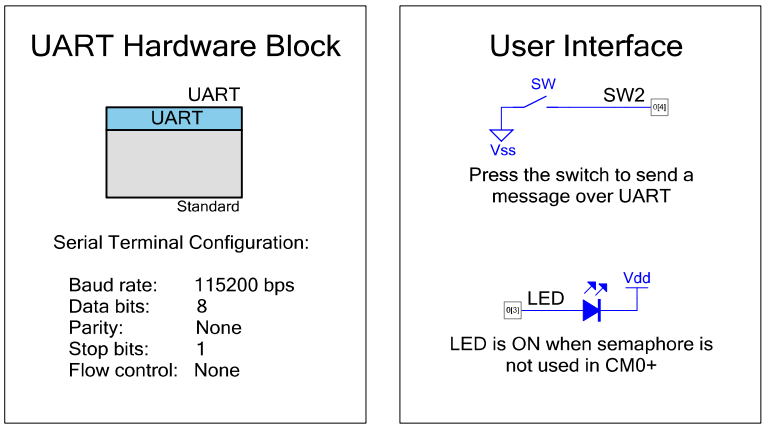
Figure 2. Terminal Prints Without Using Semaphore



Design and Implementation

The design shown in Figure 3 has a UART Component, and two GPIOs (SW2 and LED). UART is configured in TX mode to transmit data at 115200 baud rate. The GPIO SW2 is configured as an input pin to detect presses on the switch. The GPIO LED is configured as an output pin. When the LED is on, the semaphore is not in use.

Figure 3. PSoC Creator Project Schematic

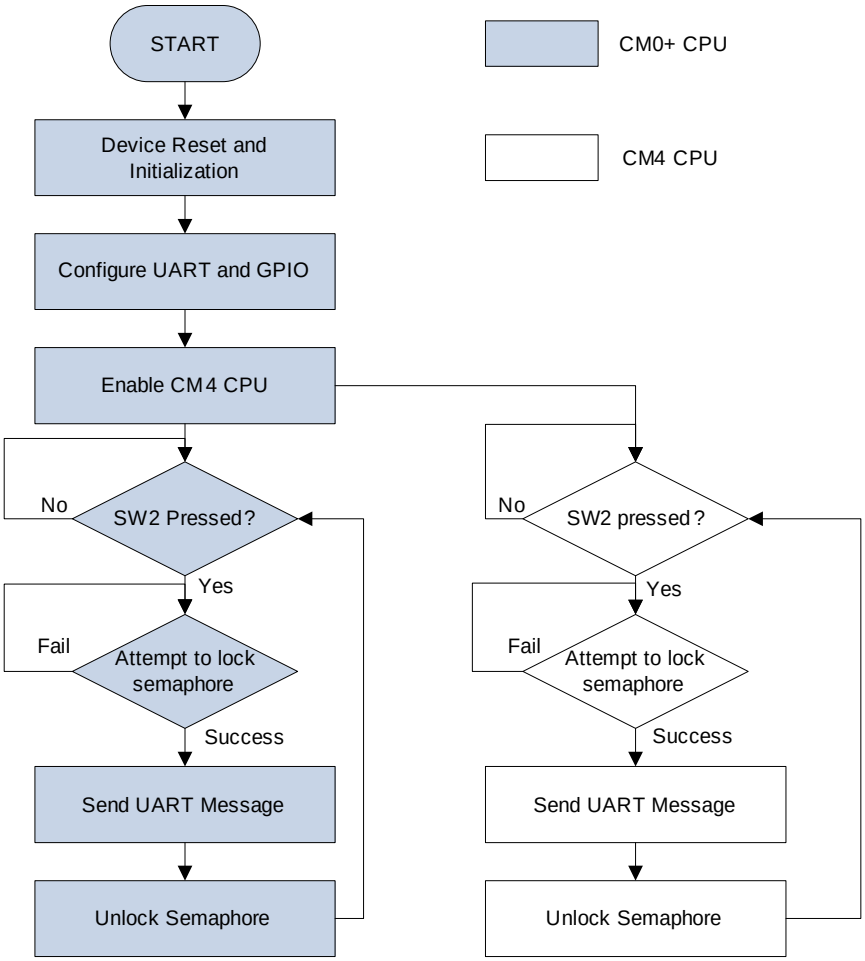


The CM0+ CPU creates the IPC semaphore, which allows synchronizing the access to a shared resource by the two CPUs. Every time one of the CPUs wants to call the UART function to print a message in the terminal, it attempts to lock the semaphore first. If it succeeds, it prints the message, and then unlocks the semaphore afterwards. If the semaphore is already locked, it keeps trying to lock it until it succeeds.

The firmware has an option to disable the semaphore in the CM0+ CPU. By simply changing the #define SEMA_ENABLE to 0u in the main_cm0p.c file, the semaphore is no longer locked by the CM0+ CPU, and the red LED on the kit is turned ON. Without the semaphore to synchronize access to the UART block, messages from both CPUs might overlap.

Figure 4 shows the firmware flowchart for the design.

Figure 4. Firmware Flowchart



Components and Settings

Table 1 lists the PSoC Creator Components used in this example, how they are used in the design, and the non-default settings required so they function as intended.

Table 1: PSoC Creator Components

Component	Instance Name	Purpose	Non-default Settings
UART	UART	Prints a message to a terminal window	TX/RX mode: TX Only
Digital Input Pin	SW2	Pin connected to the SW2 switch	Drive mode: Resistive Pull Up
Digital Output Pin	LED	Pin connected to the red LED	Initial drive state: High (1)

For information on the hardware resources used by a Component, see the Component datasheet.

Reusing This Example

This example is designed for the CY8CKIT-062-WiFi-BT pioneer kit. To port the design to a different PSoC 6 MCU device and/or kit, change the target device using the Device Selector and update the pin assignments in the Design Wide Resources Pins settings as needed.

Related Documents

Application Notes	
AN210781 – Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity	Describes PSoC 6 MCU with BLE Connectivity devices and how to build your first PSoC Creator project
AN215656 – PSoC 6 MCU: Dual-CPU System Design	Describes the dual-CPU architecture in PSoC 6 MCU, and shows how to build a simple dual-CPU design
AN219434 – Importing PSoC Creator Code into an IDE for a PSoC 6 MCU Project	Describes how to import the code generated by PSoC Creator into your preferred IDE
Code Examples	
Visit the Cypress Code Example site for a comprehensive collection of code examples using PSoC Creator IDE.	
PSoC Creator Component Datasheets	
Pins	Supports connection of hardware resources to physical pins
UART	Provides asynchronous serial communications
Device Documentation	
PSoC 6 MCU Datasheets	PSoC 6 MCU Technical Reference Manuals
Development Kit Documentation	
CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit	

Document History

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**	6161859	RLOS	04/30/2018	New code example
*A	6457461	RLOS	01/23/2019	Updated document and project to use PDL 3.1.0

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