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CE220925 - PSoC 6 MCU VDAC Sample and Hold

Objective

This example demonstrates how to sample and hold the VDAC output while in Deep-Sleep mode using a PSoC® 6 MCU.

Overview

This example demonstrates how to maintain the VDAC output voltage using the sample and hold capacitor while in Deep Sleep mode. Both Component and low-level Peripheral Driver Library (PDL) function calls are demonstrated. When the voltage across the capacitor drifts below the internal 1.20-V bandgap voltage, the comparator wakes the device to re-sample the VDAC output. When the device wakes up, the red LED on the kit is toggled for a visual cue.

Requirements

Tool: PSoC Creator™ 4.2 with PDL 3.0.1

Programming Language: C (Arm® GCC 5.4-2016-q2-update)

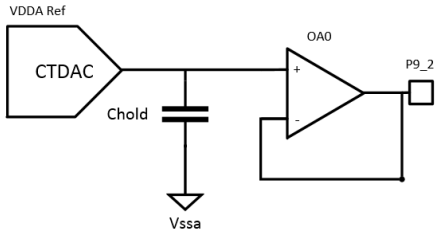
Associated Parts: PSoC 6 MCU family of devices

Related Hardware: CY8CKIT-062-BLE PSoC 6 MCU BLE Pioneer Kit and CY8CKIT-062-WiFi-BT PSoC 6 MCU Pioneer Kit

Design

The sample and hold (SH) capacitor is used to hold the DAC output voltage so that the DAC output can be turned OFF to save power. The SH capacitor is connected to one of the CTBm amplifier inputs as shown in Figure 1 to buffer the voltage. Sampling and holding are controlled by firmware.

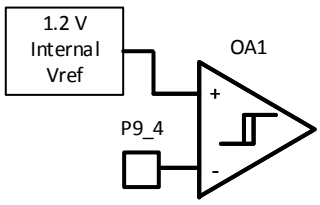
Figure 1. Sample and Hold Capacitor Connection



The opamps, analog routing switches, and bandgap reference voltage are enabled to operate in Deep Sleep mode. In Deep Sleep mode, the input voltage range of the opamps are limited to 0 V to V_{DDA} – 1.5 V. Therefore, the minimum V_{DDA} for this code example is 2.7 V.

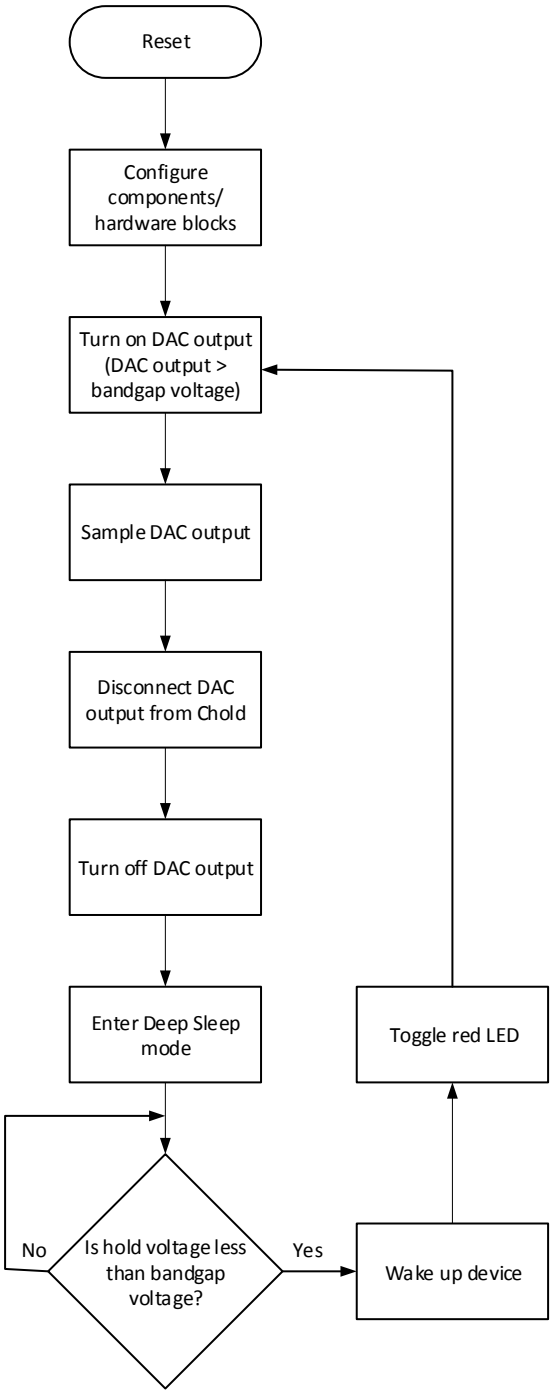
The opamp output in Figure 1 is routed to the negative terminal of OA1, configured as a comparator. The voltage is compared to an internal 1.20-V bandgap voltage. When the sampled VDAC voltage drifts below the 1.20 V bandgap voltage, the comparator will wake the device to re-sample the VDAC output.

Figure 2. Comparator Configuration



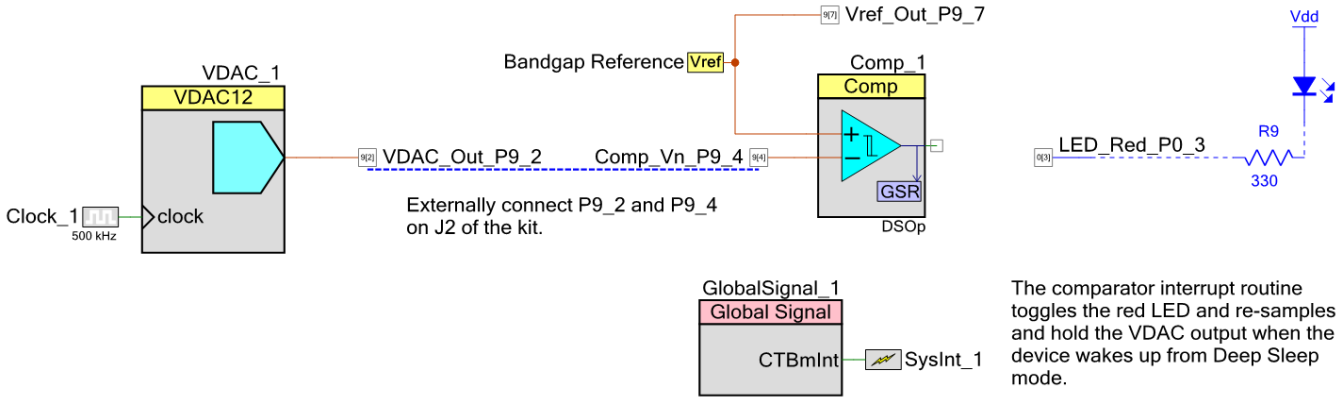
Because there are no internal analog routes between the output of OA0 and the negative input terminal of OA1 available in Deep Sleep, P9[2] and P9[4] must be externally connected.

Figure 3. Firmware Flow Chart



Using Components

Figure 4. PSoC Creator Component Schematic



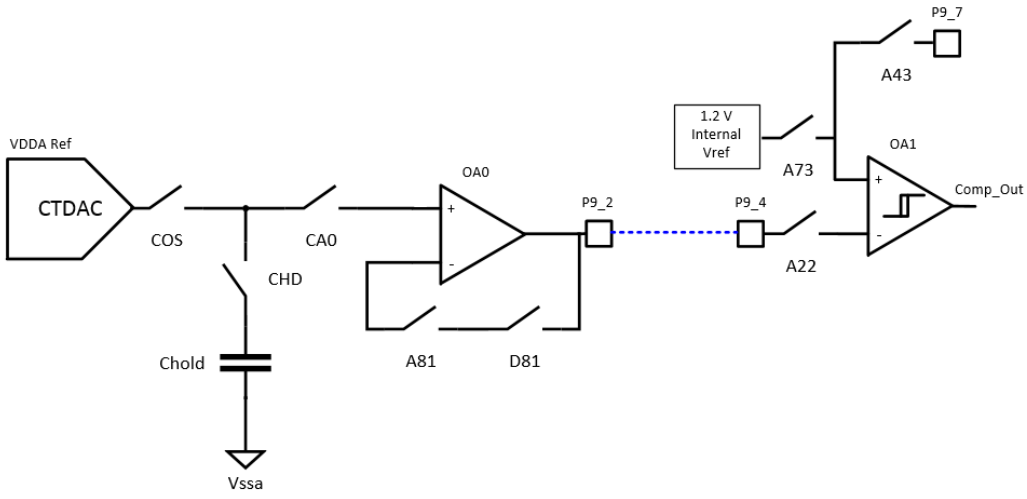
PSoC 6 MCU has one global interrrupt for all CTBm blocks. To configure and assign this interrupt, use the Global Signal Resource Component.

The internal bandgap voltage is routed to a device pin so that it can be measured.

Using PDL

To implement the design using PDL, a series of low-level API function calls are made to configure and enable the CTDAC, both opamps of the CTB, the internal 1.2 V bandgap, the sample and hold capacitor connection, and analog routing switches. Figure 5 shows the design with all the required the analog switches.

Figure 5. Schematic Implemented in PDL



Design Considerations

This code example is designed to run on the CY8CKIT-062-BLE Pioneer Kit with the CY8C6347BZI-BLD53 MCU device. To port the design to a different PSoC 6 MCU device and/or kit, change the target device using **Device Selector** and update the pin assignments in the **Design Wide Resources Pins** settings as needed. For single-core PSoC 6 MCU devices, port the code from *main_cm4.c* to *main.c*.

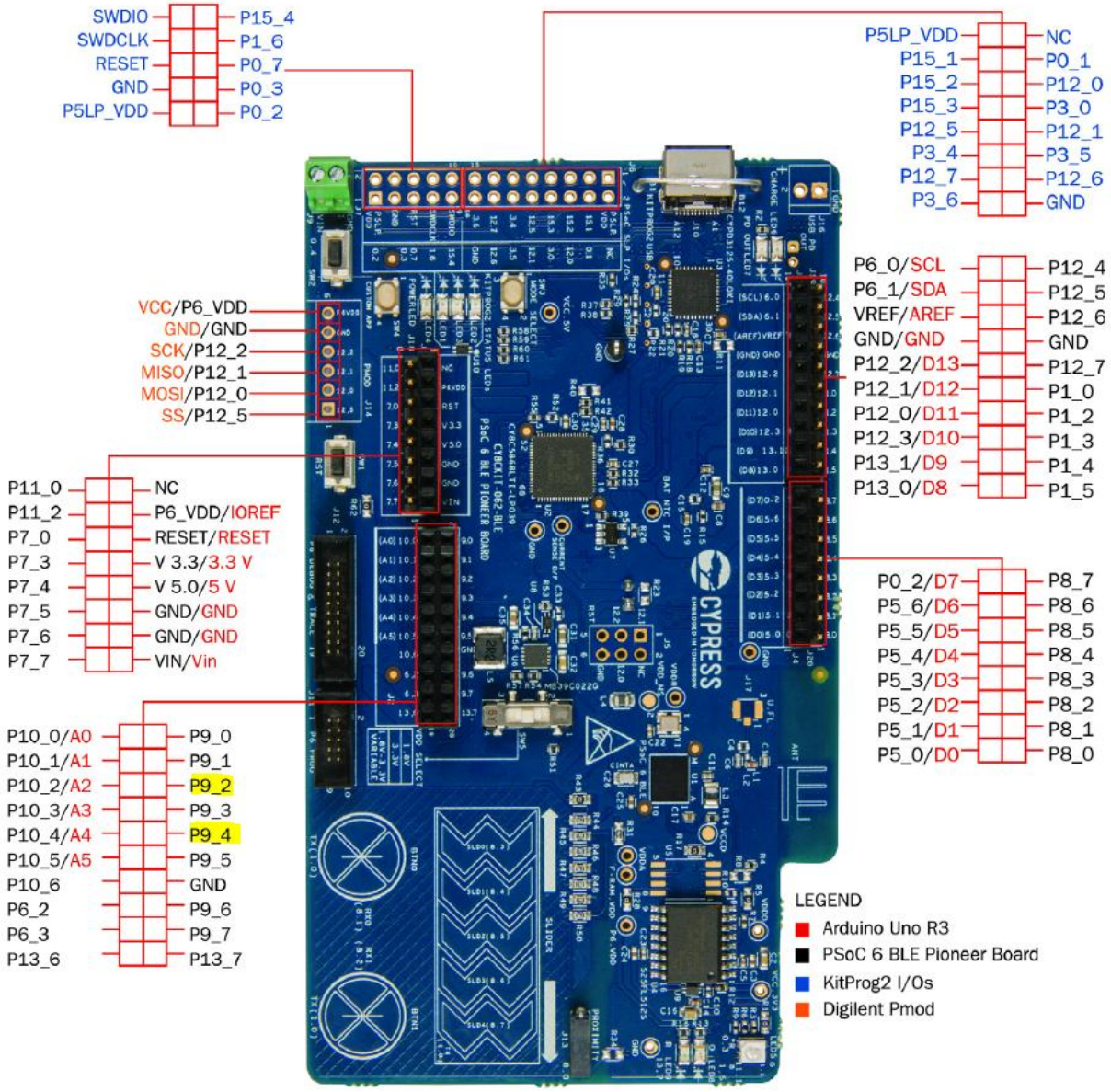
The code example relies on the VDAC output to begin at a voltage greater than the internal 1.20-V bandgap. The code example targets 1.21 V as the initial voltage based on a V_{DDA} reference of 3.3 V. Depending on the actual V_{DDA} voltage, the starting VDAC code (voltage) may require modification if it is less than 1.20 V.

Hardware Setup

This example uses the kit's default configuration and an external jumper to connect P9[2] and P9[4] on J2 (highlighted yellow in Figure 6). Connect P9[2] such that it can be probed using a digital multimeter (DMM).

Refer to the kit guide to ensure that the kit is configured correctly.

Figure 6. Pioneer Kit Pinout



Software Setup

By default, the code example uses Component API function calls. Alternatively, the `PDL_CONFIGURATION` macro can be set to (1u) to demonstrate how to use the low-level CTDAC PDL function calls.

Operation

1. Plug CY8CKIT-062 BLE into your computer's USB port.
2. Ensure switch SW5 on the kit is in position 2 to select 3.3 V for V_{DDA}.
3. Connect a wire between P9[2] and P9[4] as described in Hardware Setup.
4. Build the project and program it into the PSoC 6 MCU device. Choose **Debug** > **Program**. For more information on device programming, see PSoC Creator Help. Flash for both CPUs is programmed in a single program operation.
5. Using a digital multimeter (DMM), measure the internal bandgap voltage on P9[7] and record this value.
6. Connect a DMM to P9[2]. This is the SH voltage.

   If this voltage is less than the bandgap voltage measured in Step 5, the comparator interrupt will never trigger. Increase the VDAC output by changing the `DAC_VALUE` target in the code:

```
/* Set the VDAC output to be slightly above the 1.20 V bandgap.
* The actual value required will depend on VDDA. */
#define DAC_VALUE                (1210u) /* 1.21 volts */
```

1. Rebuild the project and program the PSoC 6 MCU device.
2. Observe the SH voltage drop slowly. When the SH voltage drops below the bandgap voltage, the red LED (LED5) on the kit turns ON. The firmware resamples the VDAC output voltage across the SH capacitor. The red LED inverts state each time the SH voltage drops below the bandgap voltage. The time it takes for the SH voltage to drop below the bandgap voltage may be a few minutes depending on device leakage.

Components

Table 1 lists the PSoC Creator Components used in this example, as well as the hardware resources used by each.

Table 1. PSoC Creator Components

Component	Instance Name	Hardware Resources
Voltage DAC (12-bit)	VDAC_1	1 CTDAC, 1 opamp, 1 sample and hold
Comparator	Comp_1	1 opamp
Global Signal Resource	GlobalSignal_1, SysInt_1	1 Interrupt
Clock	Clock_1	1 Peripheral clock divider
Vref	Bandgap Reference	1 Analog reference block
Digital Pin	LED_Red_P0_3	1 Digital output pin
Analog Pin	VDAC_Out_P9_3 Comp_Vn_P9_4 Vref_Out_P9_7	3 Analog pins

Parameter Settings

Figure 7 to Figure 10 highlight the non-default settings for the Components.

Figure 7. VDAC Component Parameter Settings

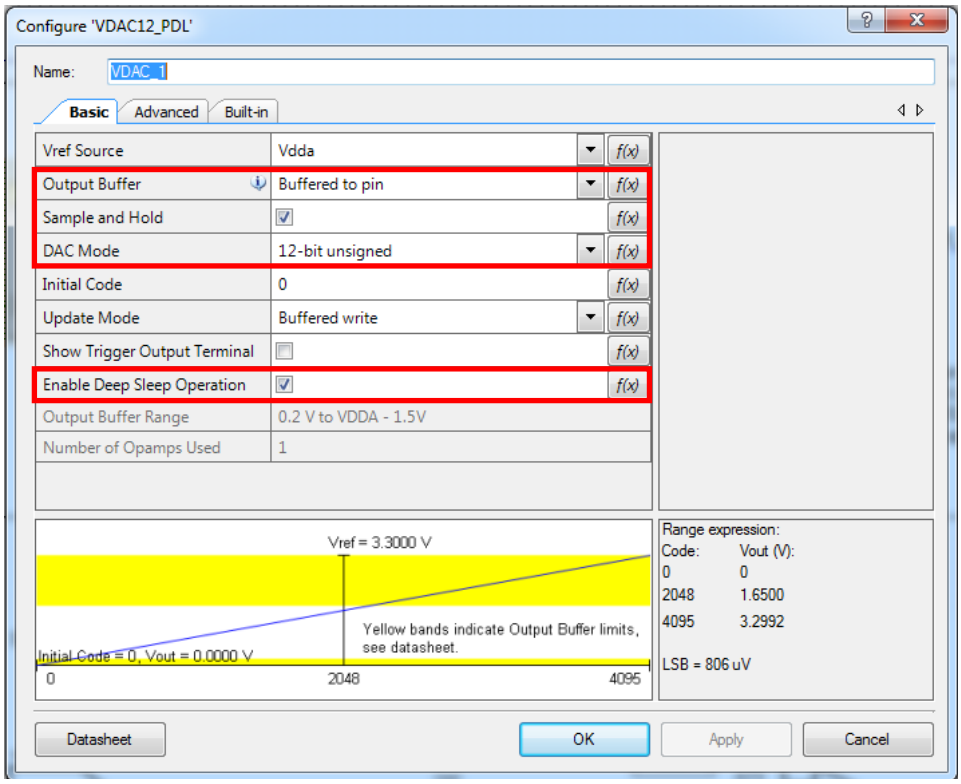


Figure 8. Comparator Component Parameter Settings

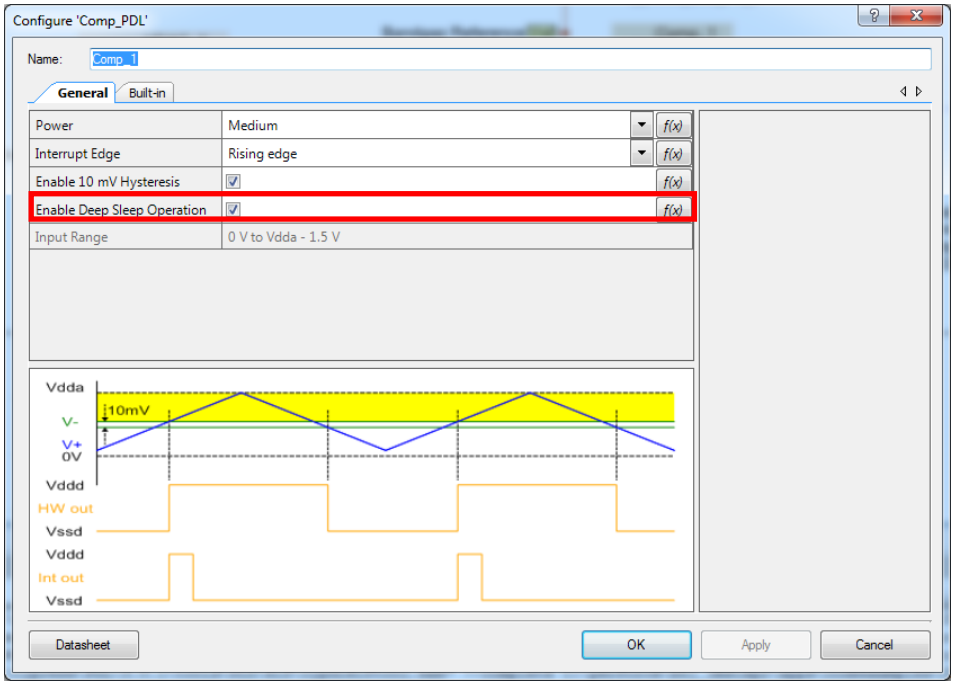


Figure 9. Global Signal Resource Component Parameter Settings

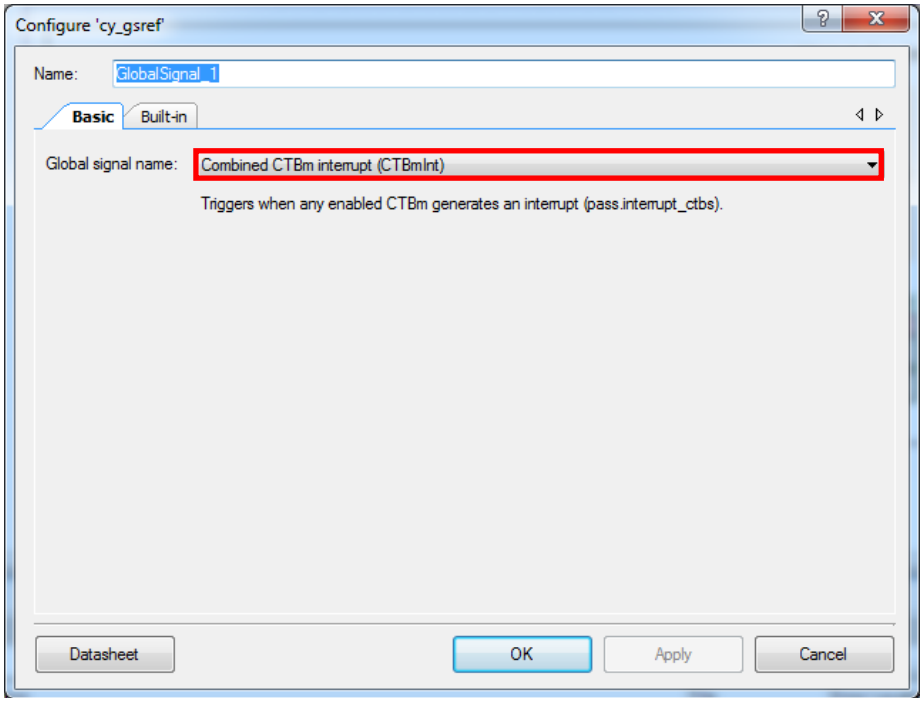
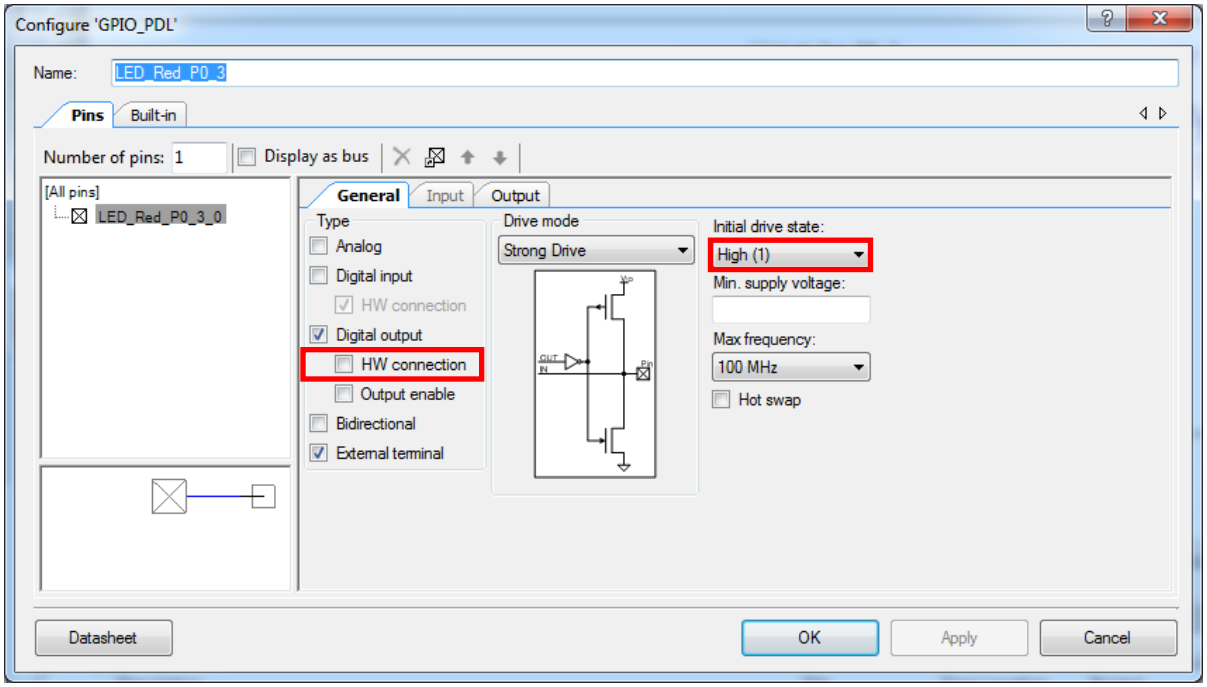


Figure 10. LED_Red_P0_3 Digital Output GPIO Parameter Settings



The LEDs on the kit turn ON when the GPIO drives a LOW and turns OFF when the GPIO drives a HIGH. The initial drive state of the LED_Red_P0_3 digital output pin is HIGH so that the LED on the board is OFF at reset.

Design-Wide Resources

Table 2 shows the pin assignments for the code example.

Table 2. Pin Names and Location

Pin Name	Pin Location
Comp_Vn_9_4	P9[4]
LED_Red_P0_3	P0[3]
VDAC_Out_P9_2	P9[2]
Vref_Out_P9_7	P9[7]

Related Documents

Application Notes	
AN210781	Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity
PSoC Creator Component Datasheets	
VDAC12	Supports continuous-time DAC functions
Comparator	Supports comparator functions
Global Signal Resource	Allows access to device level global signals
General Purpose Input / Output (GPIO)	Supports all GPIO pin features
Device Documentation	
PSoC 6 MCU: PSoC 63 with BLE Datasheet	
PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual	
PSoC 6 MCU: PSoC 63 with BLE Register Technical Reference Manual	
PSoC 6 MCU: PSoC 62 Datasheet	
Development Kit (DVK) Documentation	
PSoC 6 MCU BLE Pioneer Kit	
PSoC 6 MCU WiFi BT Pioneer Kit	

Document History

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Document Number: 002-20925

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5947250	GJV	02/19/2018	New code example

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