FM4 Family

32-BIT Microcontroller
FM4
Peripheral Manual Timer Part

Errata Sheet

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td colspan="3">Original document code:MN709-00002-2v0-E</td></tr>
<tr><td colspan="3">Rev. 1.0 December 24, 2014</td></tr>
<tr><td>121</td><td>CHAPTER 4-27</td><td>"List of registers in the RTC control block" should be corrected as indicated by the shading below.

(Error)
<table>
<tr><th>Abbreviation</th><th>Register name</th><th>Reference</th></tr>
<tr><td>WTCR10</td><td>Control Register 10</td><td>7.1</td></tr>
<tr><td>WTCR11</td><td>Control Register 11</td><td>7.2</td></tr>
<tr><td>WTCR12</td><td>Control Register 12</td><td>7.3</td></tr>
<tr><td>WTCR13</td><td>Control Register 13</td><td>7.4</td></tr>
<tr><td>WTCR20</td><td>Control Register 20</td><td>7.5</td></tr>
<tr><td>WTCR21</td><td>Control Register 21</td><td>7.6</td></tr>
<tr><td>WTSR</td><td>Second Register</td><td>7.7</td></tr>
<tr><td>WTMIR</td><td>Minute Register</td><td>7.8</td></tr>
<tr><td>WTHR</td><td>Hour Register</td><td>7.9</td></tr>
<tr><td>WTDR</td><td>Day Register</td><td>7.10</td></tr>
<tr><td>WTDW</td><td>Day Of the Week Register</td><td>7.11</td></tr>
<tr><td>WTMOR</td><td>Month Register</td><td>7.12</td></tr>
<tr><td>WTYR</td><td>Year Register</td><td>7.13</td></tr>
<tr><td>ALMIR</td><td>Alarm Minute Register</td><td>7.14</td></tr>
<tr><td>ALHR</td><td>Alarm Hour Register</td><td>7.15</td></tr>
<tr><td>ALDR</td><td>Alarm Day Register</td><td>7.16</td></tr>
<tr><td>ALMOR</td><td>Alarm Month Register</td><td>7.17</td></tr>
<tr><td>ALYR</td><td>Alarm Year Register</td><td>7.18</td></tr>
<tr><td>WTTR0</td><td>Timer Setting Register 0</td><td>7.19</td></tr>
<tr><td>WTTR1</td><td>Timer Setting Register 1</td><td>7.20</td></tr>
<tr><td>WTTR2</td><td>Timer Setting Register 2</td><td>7.21</td></tr>
</table>
The registers shown in Table 5-1 correspond to “Circuit Type 1” or “Circuit Type 3” in the chapter “VBAT Domain”. For that reason, a system reset and RTC reset do not initialize the registers in the VBAT domain. They do, however, initialize the buffers in the Always ON domain. After a reset, therefore, the save operation must be performed after the value is set again or the recall operation is performed.</td></tr>
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<tr><td>121</td><td>CHAPTER 4-27</td><td>(Correct)
<table>
<tr><th>Abbreviation</th><th>Register name</th><th>Interface circuit type</th><th>Reference</th></tr>
<tr><td>WTCR10</td><td>Control Register 10</td><td>2</td><td>7.1</td></tr>
<tr><td>WTCR11</td><td>Control Register 11</td><td>2</td><td>7.2</td></tr>
<tr><td>WTCR12</td><td>Control Register 12</td><td>-</td><td>7.3</td></tr>
<tr><td>WTCR13</td><td>Control Register 13</td><td>-</td><td>7.4</td></tr>
<tr><td>WTCR20</td><td>Control Register 20</td><td>1</td><td>7.5</td></tr>
<tr><td>WTCR21</td><td>Control Register 21</td><td>2</td><td>7.6</td></tr>
<tr><td>WTSR</td><td>Second Register</td><td>2</td><td>7.7</td></tr>
<tr><td>WTMIR</td><td>Minute Register</td><td>2</td><td>7.8</td></tr>
<tr><td>WTHR</td><td>Hour Register</td><td>2</td><td>7.9</td></tr>
<tr><td>WTDR</td><td>Day Register</td><td>2</td><td>7.10</td></tr>
<tr><td>WTDW</td><td>Day Of the Week Register</td><td>2</td><td>7.11</td></tr>
<tr><td>WTMOR</td><td>Month Register</td><td>2</td><td>7.12</td></tr>
<tr><td>WTYR</td><td>Year Register</td><td>2</td><td>7.13</td></tr>
<tr><td>ALMIR</td><td>Alarm Minute Register</td><td>2</td><td>7.14</td></tr>
<tr><td>ALHR</td><td>Alarm Hour Register</td><td>2</td><td>7.15</td></tr>
<tr><td>ALDR</td><td>Alarm Day Register</td><td>2</td><td>7.16</td></tr>
<tr><td>ALMOR</td><td>Alarm Month Register</td><td>2</td><td>7.17</td></tr>
<tr><td>ALYR</td><td>Alarm Year Register</td><td>2</td><td>7.18</td></tr>
<tr><td>WTTR0</td><td>Timer Setting Register 0</td><td>2</td><td>7.19</td></tr>
<tr><td>WTTR1</td><td>Timer Setting Register 1</td><td>2</td><td>7.20</td></tr>
<tr><td>WTTR2</td><td>Timer Setting Register 2</td><td>2</td><td>7.21</td></tr>
</table>

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For the details of interface circuit type, refer to “Interfacing with Always-on Domain in CHAPTER: VBAT Domain” in “FM4 Family PERIPHERAL MANUAL”.</td></tr>
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<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>173</td><td>CHAPTER 4-37</td><td>"List of registers in the RTC control block" should be corrected as indicated by the shading below.

(Error)
<table>
<tr><th>Abbreviation</th><th>Register name</th><th>Reference</th></tr>
<tr><td>WTCR10</td><td>Control Register 10</td><td>7.1</td></tr>
<tr><td>WTCR11</td><td>Control Register 11</td><td>7.2</td></tr>
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<tr><td>WTYR</td><td>Year Register</td><td>7.13</td></tr>
<tr><td>ALMIR</td><td>Alarm Minute Register</td><td>7.14</td></tr>
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<tr><td>WTTR0</td><td>Timer Setting Register 0</td><td>7.19</td></tr>
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<tr><td>WTTR0</td><td>Timer Setting Register 0</td><td>-</td><td>7.19</td></tr>
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<tr><td>208</td><td>CHAPTER 4-43</td><td>
"Table3-1 Example of frequency correction range with WTCALPRD=19" should be corrected as indicated by the shading below.

(Error)
Table 3-1 Example of frequency correction range with WTCALPRD=19 (ideal value)
<table>
<tr><th>WTCAL</th><th>Correction rate[ppm]</th><th>Sub clock frequency [Hz]</th></tr>
<tr><td>0</td><td>122.1</td><td>32764.00</td></tr>
<tr><td>1</td><td>120.5</td><td>32764.05</td></tr>
<tr><td>2</td><td>119.0</td><td>32764.10</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>79</td><td>1.5</td><td>32767.95</td></tr>
<tr><td>80</td><td>0.0</td><td>32768.00</td></tr>
<tr><td>81</td><td>-1.5</td><td>32768.05</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>159</td><td>-120.5</td><td>32771.95</td></tr>
<tr><td>160</td><td>-122.1</td><td>32772.00</td></tr>
<tr><td>161</td><td>-123.6</td><td>32772.05</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>318</td><td>-363.2</td><td>32779.90</td></tr>
<tr><td>319</td><td>-364.7</td><td>32779.95</td></tr>
<tr><td>320</td><td>-366.2</td><td>32780.00</td></tr>
</table>
(Correct)
Table 3-1 Example of frequency correction range with WTCALPRD=19 (Target frequency is 32768Hz)
<table>
<tr><th>Sub clock frequency before correction[Hz]</th><th>WTCAL</th><th>Correction rate [ppm]</th></tr>
<tr><td>32768.00</td><td>0</td><td>0.0</td></tr>
<tr><td>32768.05</td><td>1</td><td>-1.53</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>32769.95</td><td>39</td><td>-59.51</td></tr>
<tr><td>32770.00</td><td>40</td><td>-61.0</td></tr>
<tr><td>32770.05</td><td>41</td><td>-62.6</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>32771.90</td><td>78</td><td>-119.0</td></tr>
<tr><td>32771.95</td><td>79</td><td>-120.5</td></tr>
<tr><td>32772.00</td><td>80</td><td>-122.1</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>208</td><td>CHAPTER 4-4 3</td><td>"Table3-2 Example of frequency correction range with WTCALPRD=59" should be corrected as indicated by the shading below.

(Error)
Table 3-2 Example of frequency correction range with WTCALPRD=59 (ideal value)
<table>
<tr><th>WTCAL</th><th>Correction rate[ppm]</th><th>Sub clock frequency [Hz]</th></tr>
<tr><td>0</td><td>122.1</td><td>32764.00</td></tr>
<tr><td>1</td><td>121.6</td><td>32764.02</td></tr>
<tr><td>2</td><td>121.1</td><td>32764.03</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>79</td><td>0.5</td><td>32767.98</td></tr>
<tr><td>80</td><td>0.0</td><td>32768.00</td></tr>
<tr><td>81</td><td>-0.5</td><td>32768.02</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>159</td><td>-121.6</td><td>32771.98</td></tr>
<tr><td>160</td><td>-122.1</td><td>32772.00</td></tr>
<tr><td>161</td><td>-122.6</td><td>32772.02</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>318</td><td>-365.2</td><td>32779.97</td></tr>
<tr><td>319</td><td>-365.7</td><td>32779.98</td></tr>
<tr><td>320</td><td>-366.2</td><td>32780.00</td></tr>
</table>
(Correct)
Table 3-2 Example of frequency correction range with WTCALPRD=59 (Target frequency is 32768Hz)
<table>
<tr><th>Sub clock frequency before correction[Hz]</th><th>WTCAL</th><th>Correction rate [ppm]</th></tr>
<tr><td>32768.00</td><td>0</td><td>0.0</td></tr>
<tr><td>32768.02</td><td>1</td><td>-0.51</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>32771.98</td><td>239</td><td>-121.6</td></tr>
<tr><td>32772.00</td><td>240</td><td>-122.1</td></tr>
<tr><td>32772.02</td><td>241</td><td>-122.6</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>32779.97</td><td>718</td><td>-365.1</td></tr>
<tr><td>32779.98</td><td>719</td><td>-365.6</td></tr>
<tr><td>32780.00</td><td>720</td><td>-366.1</td></tr>
</table></td></tr>
<tr><td>209</td><td>CHAPTER 4-4 4</td><td>"Setting procedures of frequency correction, Find out the setting of WTCAL with the following formula." should be corrected as indicated by the shading below.

(Error)
WTCAL = {(Frequency before correction-8192×4) / (WTCALPRD+1)} × 2^20

(Correct)
WTCAL = {(Frequency before correction – ideal Frequency) / ideal Frequency} ×32768×(WTCALPRD + 1)</td></tr>
</table>

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>226</td><td>CHAPTER 4-5 3</td><td>"Table3-1 Example of frequency correction range with WTCALPRD=19" should be corrected as indicated by the shading below.

(Error)
Table 3-1 Example of frequency correction range with WTCALPRD=19 (ideal value)
<table>
<tr><th>WTCAL</th><th>Correction rate[ppm]</th><th>Sub clock frequency [Hz]</th></tr>
<tr><td>0</td><td>122.1</td><td>32764.00</td></tr>
<tr><td>1</td><td>120.5</td><td>32764.05</td></tr>
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<tr><td>79</td><td>1.5</td><td>32767.95</td></tr>
<tr><td>80</td><td>0.0</td><td>32768.00</td></tr>
<tr><td>81</td><td>-1.5</td><td>32768.05</td></tr>
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<tr><td>320</td><td>-366.2</td><td>32780.00</td></tr>
</table>
(Correct)
Table 3-1 Example of frequency correction range with WTCALPRD=19 (Target frequency is 32768Hz)
<table>
<tr><th>Sub clock frequency before correction[Hz]</th><th>WTCAL</th><th>Correction rate [ppm]</th></tr>
<tr><td>32768.00</td><td>0</td><td>0.0</td></tr>
<tr><td>32768.05</td><td>1</td><td>-1.53</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>32769.95</td><td>39</td><td>-59.51</td></tr>
<tr><td>32770.00</td><td>40</td><td>-61.0</td></tr>
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</table></td></tr>
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<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>226</td><td>CHAPTER 4-5
3</td><td>"Table3-2 Example of frequency correction range with WTCALPRD=59" should be corrected as indicated by the shading below.

(Error)
Table 3-2 Example of frequency correction range with WTCALPRD=59 (ideal value)
<table>
<tr><th>WTCAL</th><th>Correction rate[ppm]</th><th>Sub clock frequency [Hz]</th></tr>
<tr><td>0</td><td>122.1</td><td>32764.00</td></tr>
<tr><td>1</td><td>121.6</td><td>32764.02</td></tr>
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<tr><td>:</td><td>:</td><td>:</td></tr>
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<tr><td>80</td><td>0.0</td><td>32768.00</td></tr>
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<tr><td>319</td><td>-365.7</td><td>32779.98</td></tr>
<tr><td>320</td><td>-366.2</td><td>32780.00</td></tr>
</table>
(Correct)
Table 3-2 Example of frequency correction range with WTCALPRD=59 (Target frequency is 32768Hz)
<table>
<tr><th>Sub clock frequency before correction[Hz]</th><th>WTCAL</th><th>Correction rate [ppm]</th></tr>
<tr><td>32768.00</td><td>0</td><td>0.0</td></tr>
<tr><td>32768.02</td><td>1</td><td>-0.51</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>32771.98</td><td>239</td><td>-121.6</td></tr>
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(Correct)
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<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>436</td><td>CHAPTER 6
3.3</td><td>3.3.26. ADCMP Control Register C (ACSC) should be corrected as indicated by the shading below.

(Error)
<table>
<tr><th rowspan="2">Process</th><th colspan="2">Value</th><th colspan="2">Function</th></tr>
<tr><th>APBM</th><th>BUFE</th><th>Buffer function</th><th>Transfer timing</th></tr>
<tr><td rowspan="9">Write</td><td>0</td><td>00</td><td>Disabled</td><td>Always when writing to ACMP and ACMC from CPU</td></tr>
<tr><td>0</td><td>01</td><td rowspan="2">Enabled</td><td>When connected FRT is Zero/Bottom status</td></tr>
<tr><td>0</td><td>10</td><td>When connected FRT is Peak/Top status</td></tr>
<tr><td>0</td><td>11</td><td>Disabled</td><td>When connected FRT is Zero/Bottom status or Peak/Top status</td></tr>
<tr><td>1</td><td>00</td><td rowspan="4">Enabled</td><td>Always when writing to ACMP and ACMC from CPU</td></tr>
<tr><td>1</td><td>01</td><td>When connected FRT is Zero/Bottom status, and MSZC=0000</td></tr>
<tr><td>1</td><td>10</td><td>When connected FRT is Peak/Pop status, and MSPC=0000</td></tr>
<tr><td>1</td><td>11</td><td>Condition A : connected FRT is Zero/Bottom status.
Condition B :connected FRT is MSZC=0000.
Condition C: connected FRT is Peak/Top status
Condition D: connected FRT is MSPC=0000.
When (Condition A and Condition B) or (Condition C and Condition D)</td></tr>
<tr><td>Read</td><td>-</td><td>-</td><td colspan="2">Reads the register setting.</td></tr>
</table>
(Correct)
<table>
<tr><th rowspan="2">Process</th><th colspan="2">Value</th><th colspan="2">Function</th></tr>
<tr><th>APBM</th><th>BUFE</th><th>Buffer function</th><th>Transfer timing</th></tr>
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<tr><td>0</td><td>01</td><td rowspan="3">Enabled</td><td>When connected FRT is Zero/Bottom status</td></tr>
<tr><td>0</td><td>10</td><td>When connected FRT is Peak/Top status</td></tr>
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<tr><td>1</td><td>01</td><td rowspan="4">Enabled</td><td>When connected FRT is Zero/Bottom status, and MSZC=0000</td></tr>
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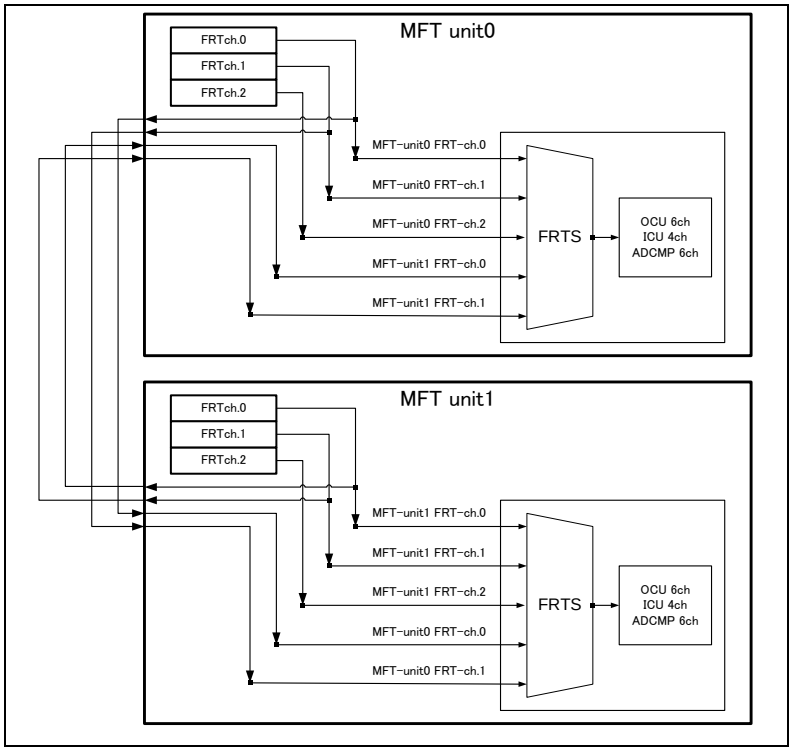
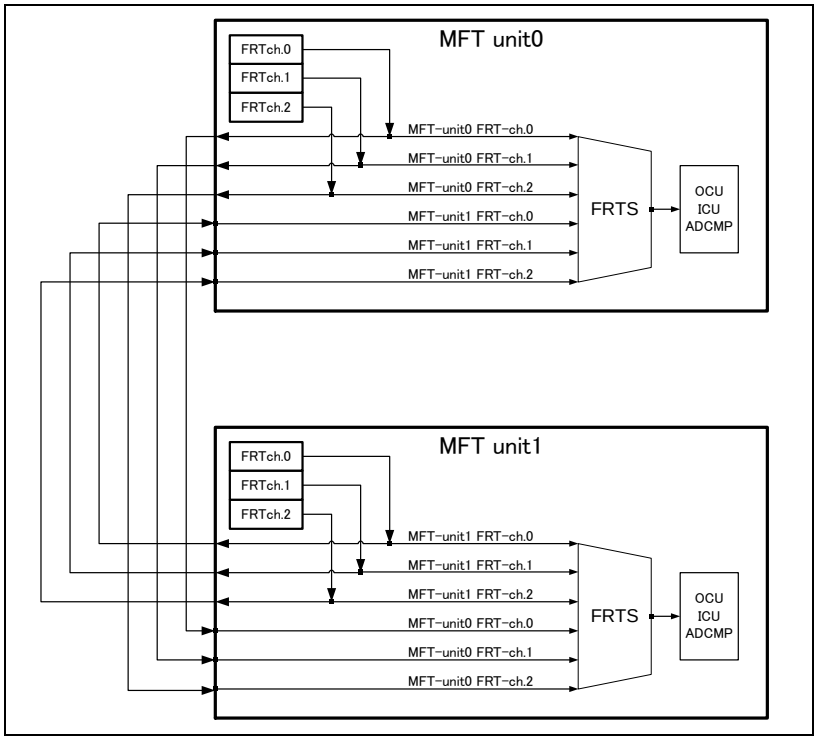
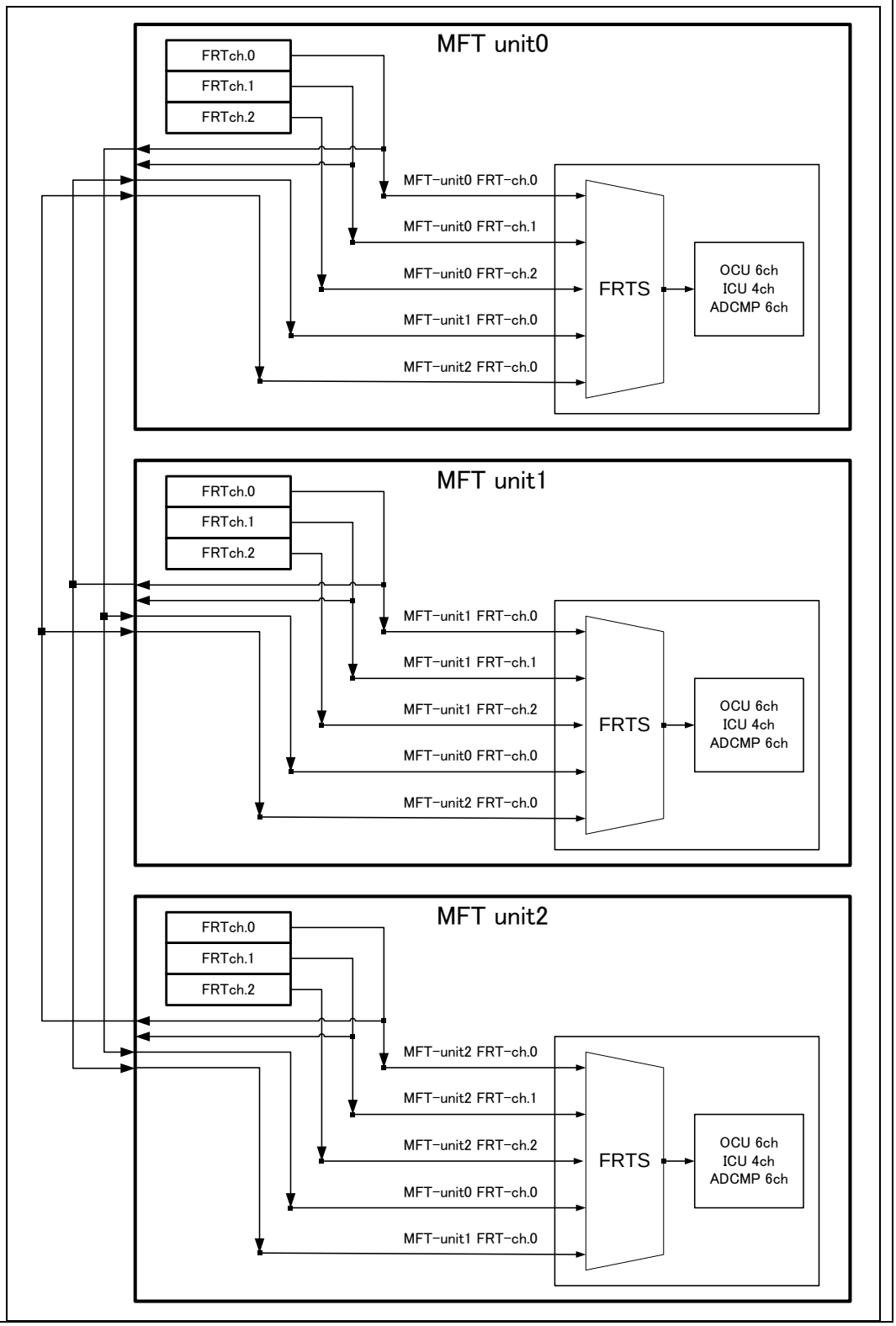
<tr><td>Read</td><td>-</td><td>-</td><td colspan="2">Reads the register setting.</td></tr>
</table></td></tr>
</table>

Page	Item	Description
512	CHAPTER 6 4.8.1	Figure 4-55 should be corrected as below. (Error) **Figure 4-55 Diagram of FRT Connected between Multifunction Timer Units (For Product Mounting 2 Multifunction Timer Units)**  (Correct) **Figure 4-55 Diagram of FRT Connected between Multifunction Timer Units (For Product Mounting 2 Multifunction Timer Units)** 

Page	Item	Description
514	CHAPTER 6 4.8.2	Figure 4-56 should be corrected as below. (Error) **Figure 4-56 Diagram of FRT Connected between Multifunction Timer Units (For Product Mounting 3 Multifunction Timer Units)**



Page	Item	Description
514	CHAPTER 6 4.8.2	(Correct) **Figure 4-56 Diagram of FRT Connected between Multifunction Timer Units (For Product Mounting 3 Multifunction Timer Units)**

