FM4 Family

32-BIT Microcontroller
FM4
Peripheral Manual

Errata Sheet

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td colspan="3">Original document code: MN709-00001-2v0-E</td></tr>
<tr><td colspan="3">Rev. 1.0 November 28, 2014</td></tr>
<tr><td>98</td><td>CHAPTER 2-2: 4.6</td><td>"4.6 Peripheral Function Reset Control Reset 2 (MRST2)" should be corrected as indicated by the shading below.

(Error)
[bit28] QSPIRST: Reset control of Hi-Speed Quad SPI controller
This bit controls the reset of the Hi-Speed Quad SPI controller unit. If this bit is set to "1", the SD card interface becomes a reset state, the operation of the Hi-Speed Quad SPI controller stops, and the register settings are initialized. For products to which the Hi-Speed Quad SPI controller is not mounted, do not set this bit to "1". To release the above-mentioned reset state, be sure to set this bit to "0" again.

(Correct)
[bit28] QSPIRST: Reset control of Hi-Speed Quad SPI controller
This bit controls the reset of the Hi-Speed Quad SPI controller unit. If this bit is set to "1", the Hi-Speed Quad SPI controller becomes a reset state, the operation of the Hi-Speed Quad SPI controller stops, and the register settings are initialized. For products to which the Hi-Speed Quad SPI controller is not mounted, do not set this bit to "1". To release the above-mentioned reset state, be sure to set this bit to "0" again.</td></tr>
<tr><td>175</td><td>CHAPTER 5 5.1</td><td>"[bit6:2] SVHI ■ For TYPE1-M4 and TYPE2-M4 products" should be corrected as indicated by the shading below.

<table>
<tr><th>bit6:2</th><th>Description</th></tr>
<tr><td>00111</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 2.8V.
[Initial value]</td></tr>
<tr><td>00100</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 3.0V.</td></tr>
<tr><td>01100</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 3.2V.</td></tr>
<tr><td>01111</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 3.6V.</td></tr>
<tr><td>01110</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 3.7V.</td></tr>
<tr><td>01001</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 4.0V.</td></tr>
<tr><td>01000</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 4.1V.</td></tr>
<tr><td>11000</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 4.2V.</td></tr>
<tr><td>Others</td><td>Setting is prohibited.</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>175</td><td>CHAPTER 5
5.1</td><td>"[bit6:2] SVHI ■ For TYPE3-M4 products" should be corrected as indicated by the shading below.

<table>
<tr><th>bit6:2</th><th>Description</th></tr>
<tr><td>00111</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 2.9V.
[Initial value]</td></tr>
<tr><td>00100</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 3.1V.</td></tr>
<tr><td>01100</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 3.3V.</td></tr>
<tr><td>01111</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 3.8V.</td></tr>
<tr><td>01110</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 3.9V.</td></tr>
<tr><td>01001</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 4.2V.</td></tr>
<tr><td>01000</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 4.3V.</td></tr>
<tr><td>11000</td><td>Set the low-voltage detection interrupt voltage in the vicinity of 4.4V.</td></tr>
<tr><td>Others</td><td>Setting is prohibited.</td></tr>
</table></td></tr>
<tr><td>361</td><td>CHAPTER 8
2</td><td>"Table 2-3 List of interrupt signals input to DSTC" should be corrected as indicated by the shading below.

<table>
<tr><th>Number</th><th>Interrupt signal name</th></tr>
<tr><td></td><td></td></tr>
<tr><td>218</td><td>I2S reception DSTC transfer request (Refer marginal remarks)</td></tr>
<tr><td>219</td><td>I2S transmission DSTC transfer request (Refer marginal remarks)</td></tr>
<tr><td>220</td><td>Hi-Speed Quad SPI reception DSTC transfer request
(Refer marginal remarks)</td></tr>
<tr><td>221</td><td>Hi-Speed Quad SPI transmission DSTC transfer request
(Refer marginal remarks)</td></tr>
<tr><td>222</td><td>Programmable CRC DSTC transfer request (Refer marginal remarks)</td></tr>
<tr><td>223</td><td>CAN-FD DSTC transfer request (Refer marginal remarks)</td></tr>
<tr><td>224 to 255</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td colspan="3">Rev. 2.0 December 19, 2014</td></tr>
<tr><td>900</td><td>CHAPTER 19:
4.5</td><td>"4.5 CRC Computing Configuration Register" should be corrected as indicated by the shading below.

(Error)
[bit25] CIEN(PRGCRC Interrupt request enable)

(Correct)
[bit26] CDEN(PRGCRC DMA request enable)</td></tr>
</table>