Programmable Gain Amplifier Datasheet PGA V 3.2

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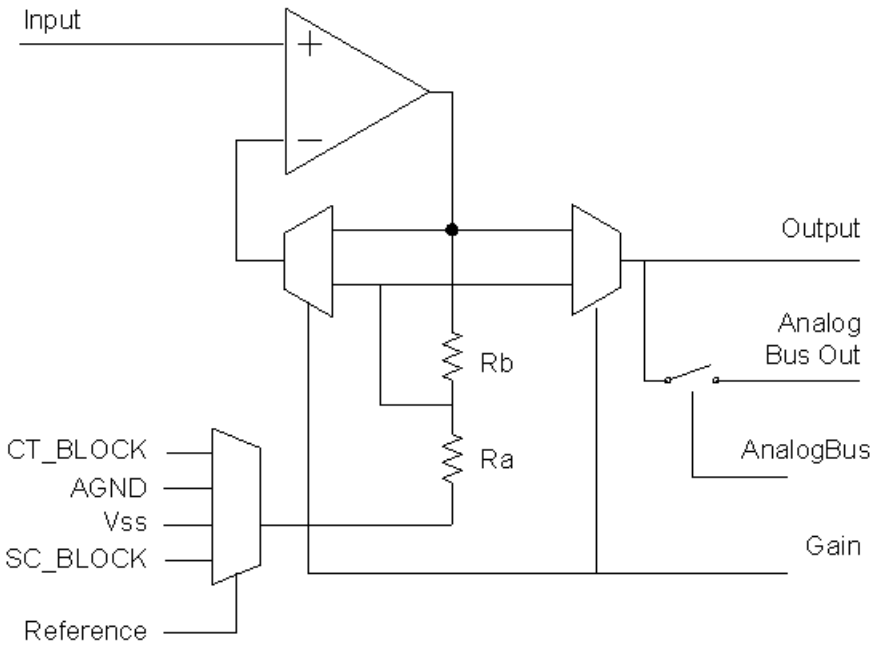
Resources	PSoC® Blocks			API Memory (Bytes)		Pins (per External I/O)
	Digital	Analog CT	Analog SC	Flash	RAM	
CY8C29/27/24/22xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CTMA30xx, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52						
	0	1	0	52	0	1

Features and Overview

- CY8C26/25xxx: thirty-one user-programmable gain settings with a maximum gain of 16.0.
- All other PSoC Devices: thirty-three user-programmable gain settings with a maximum gain of 48.0.
- High impedance input
- Single-ended output with selectable reference

The PGA User Module implements an opamp based non-inverting amplifier with user-programmable gain. This amplifier has high input impedance, wide bandwidth, and selectable reference.

Figure 1. PGA Block Diagram



Functional Description

The PGA User Module amplifies an internal or externally-applied signal. This signal can be referenced to the internal analog ground, V_{SS}, or other selected references. The gain, of the programmable gain amplifier, is set by programming the selectable tap in a resistor array and the feedback tap in a continuous time analog PSoC block. The gain, input, reference, and output bus enable are set by the user from tables of values in the Device Editor. The output of the programmable gain amplifier has a two-part transfer function.

For gains greater than or equal to one, the top of the resistor string is connected to the opamp output and the resistor tap is connected to the inverting input of the opamp. The amplifier has the following transfer function.

Equation 1

$$V_O = (V_{IN} - V_{GND}) \cdot \left(1 + \frac{R_b}{R_a}\right) + V_{GND}$$

For gains less than one (i.e., attenuation), the opamp is set as a voltage follower and the user module output is selected at the resistor tap. The amplifier then has the following transfer function.

Equation 2

$$V_O = (V_{IN} - V_{GND}) \cdot \left(\frac{R_a}{R_a + R_b}\right) + V_{GND}$$

The user can specify the reference as one of the following: a fixed value derived from the internal bandgap reference, a value ratiometric to the supply voltage, analog ground, or an external input.

The input and output voltage ranges of the amplifier do not extend to the power supplies (i.e., they are not "rail-to-rail" opamps). The allowed input range is a combination of input limit, output limit, power supply voltage, analog ground value, and selected gain. This is illustrated in the DC and AC Electrical Characteristics section.

The user selects the Gain from the values in the Device Editor. The Device Editor then programs the appropriate resistor taps in the PSoC block. API routines are provided to start, stop, set power, and set gain.

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in tables below, TA = 25°C, Vdd = 5.0V, Power HIGH, Op-Amp Bias LOW, output referenced to Analog Ground = 2*VBandGap.

Table 1. 5.0V PGA DC Electrical Characteristics

Parameter	Typical	Limit	Units	Conditions and Notes
Gain Deviation from Nominal				
G=48.00	3.0	--	%	
G=24.00	2.2	--	%	
G=16.00	1.5	--	%	
G=4.00	0.7	--	%	
G=1.0	0.5	--	%	
Input				
Input Offset Voltage[3]	4.5	--	mV	
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance[1]	3	--	pF	
Output Swing	0.05 to Vdd-0.05	--	V	
PSRR	73	--	dB	
Operating Current				
Low Power	142	--	µA	
Med Power	540	--	µA	
High Power	2083	--	µA	

Table 2. 5.0V PGA AC Electrical Characteristics

Parameter	Typical	Limit	Units	Conditions and Notes
Slew Rate(20% to 80%)[2]				
Low Power	0.6	--	V/µs	
Med Power	2.5	--	V/µs	
High Power	9.5	--	V/µs	
Settling Time[2]				

Parameter	Typical	Limit	Units	Conditions and Notes
Low Power	13	--	µs	
Med Power	4	--	µs	
High Power	1	--	µs	
Noise[2]				Referred to input
Low Power	354		nV/√Hz	OpAmp bias low except at High Power. Reference input set to AGND
Med Power	112		nV/√Hz	
High Power	99		nV/√Hz	

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the tables below, all TA = 25°C, Vdd = 3.3V, Power HIGH, Op-Amp bias LOW, output referenced to Analog Ground = Vdd/ .

Table 3. 3.3V PGA DC Electrical Characteristics

Parameter	Typical	Limit	Units	Conditions and Notes
Gain Deviation from Nominal				
G=48.00	4.0	--	%	
G=24.00	2.2	--	%	
G=16.00	1.2	--	%	
G=4.00	0.6	--	%	
G=1.0	0.3	--	%	
Input				
Input Offset Voltage[3]	3.5	--	mV	
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance[1]	3	--	pF	
Output Swing	0.05 to Vdd-0.05	--	V	
PSRR	68	--	dB	
Operating Current				
Low Power	135	--	µA	
Med Power	523	--	µA	
High Power	2017	--	µA	

Table 4. 3.3V PGA AC Electrical Characteristics

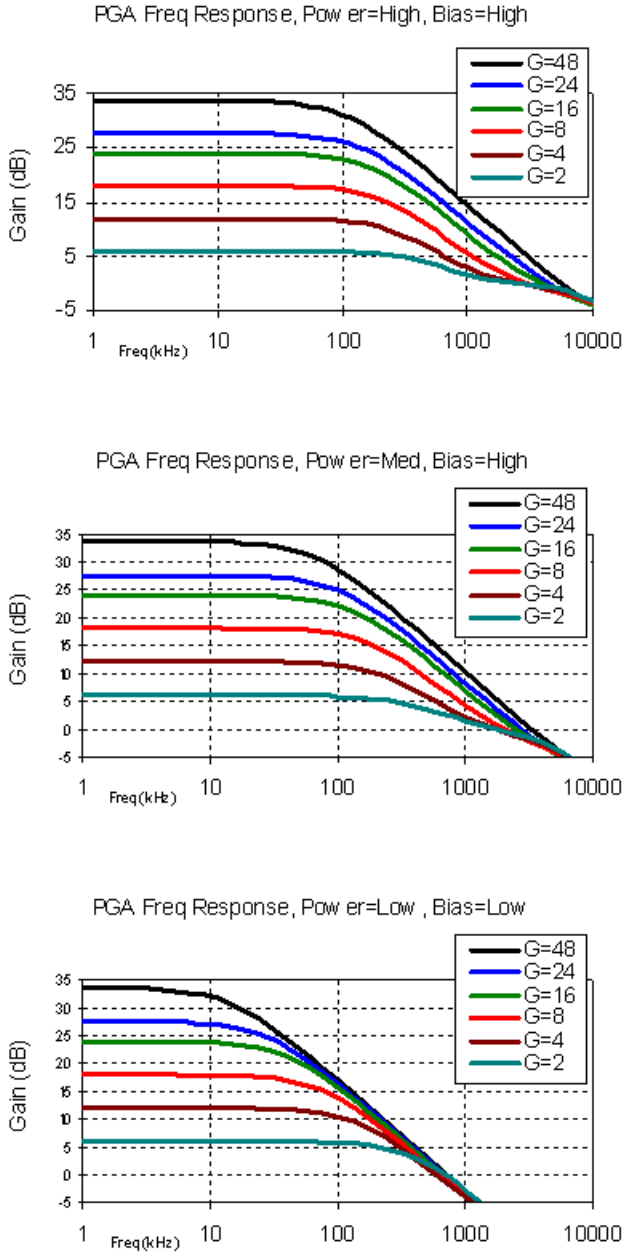
Parameter	Typical	Limit	Units	Conditions and Notes
Slew Rate (20% to 80%)[2]				
Low Power	.6	--	V/µs	
Med Power	2.4	--	V/µs	
High Power	9.0	--	V/µs	
Settling Time[2]				
Low Power	12	--	µs	
Med Power	4	--	µs	
High Power	1	--	µs	
Noise[2]				Referred to input
Low Power	354		nV/√Hz	OpAmp bias low except at High Power. Reference input set to AGND
Med Power	112		nV/√Hz	
High Power	99		nV/√Hz	

Electrical Characteristics Notes

1. Includes I/O pin.
2. Based upon device simulation.
3. Input offset voltage is affected by reference power setting in CY8C24x23 only. Input offset voltage is not affected for reference connections other than Vss and not affected for chips other than CY8C24x23. In applications where the gain is greater than 1.0 and reference is selected to be Vss, an offset may be added to the PGA input offset voltage. This offset is up to -7.5 mV for RefPower=HIGH, -4 mV for RefPower=MEDIUM, and 0.6 mV for RefPower=LOW. RefPower is selected in Global Resources. The added offset voltage is always negative.

The bandwidth of the PGA is determined by the open loop gain bandwidth of the opamp; higher power settings yields higher band width.

Figure 2. CY8C29/27/24/22xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CTMA30xx, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52 Bandwidth



Placement

The GAIN block maps freely onto any of the continuous time PSoC blocks in the device.

Parameters and Resources

Gain

The Gain is selected from values ranging from 0.062 to 48.00, using PSoC Designer or the SetGain routine provided in the API. If the output of the PGA is used as input for an ADC the Gain must be one or greater.

Input

The inputs to the programmable gain amplifier are driven by the outputs of the adjacent PSoC blocks and the analog column input multiplexer. The user makes selections of specific input in the Device Editor.

Reference

The gain of the PGA is referenced to a "ground" value selected by the user. Choices include AGND (on-chip analog ground), V_{ss}, and adjacent continuous time (CT) and switched capacitor (SC) blocks. CT and SC block connections allow for adjustable offsets as a controlled reference voltage.

AnalogBus

The GAIN block output may be routed through the analog PSoC block array’s network of local interconnections and/or through an analog output bus. Setting the PGA User Module AnalogBus parameter to Disable, the default value, restricts the set of possible connections to the local network. If the GAIN AnalogBus output is enabled onto the bus, care must be exercised to ensure that no other user module drives this same bus.

Application Programming Interface

The Application Programming Interface (API) routines are provided as part of the user module to allow the designer to deal with the module at a higher level. This section specifies the interface to each function together with related constants provided by the “include" files.

Note

In this, as in all user module APIs, the values of the A and X register may be altered by calling an API function. It is the responsibility of the calling function to preserve the values of A and X prior to the call if those values are required after the call. This “registers are volatile" policy was selected for efficiency reasons and has been in force since version 1.0 of PSoC Designer. The C compiler automatically takes care of this requirement. Assembly language programmers must ensure their code observes the policy, too. Though some user module API function may leave A and X unchanged, there is no guarantee they will do so in the future.

For Large Memory Model devices, it is also the caller's responsibility to preserve any value in the CUR_PP, IDX_PP, MVR_PP, and MVW_PP registers. Even though some of these registers may not be modified now, there is no guarantee that will remain the case in future releases.

PGA_Start

Description:

Performs all required initialization for this user module and sets the power level for the continuous time PSoC block. The output will be driven once the PowerSetting is applied to the block.

C Prototype:

```
void  PGA_Start(BYTE bPowerSetting)
```

Assembler:

```
mov   A, bPowerSetting
lcall  PGA_Start
```

Parameters:

bPowerSetting: One byte that specifies the power level to the analog PSoC block. Following reset and configuration, the PSoC block assigned to the PGA is powered down. Symbolic names provided in C and assembly, and their associated values, are given in the following table.

Symbolic Name	Value
PGA_OFF	0
PGA_LOWPOWER	1
PGA_MEDPOWER	2
PGA_HIGHPOWER	3

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

PGA_SetPower

Description:

Sets the power level for the continuous time PSoC blocks. May be used to turn the PGA off and on. Output will be driven if the PowerSetting is not off.

C Prototype:

```
void  PGA_SetPower(BYTE bPowerSetting)
```

Assembler:

```
mov   A, bPowerSetting
lcall  PGA_SetPower
```

Parameters:

bPowerSetting: Same as the PowerSetting used for the Start function.

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

PGA_SetGain

Description:

Sets the gain for the continuous time PSoC block.

C Prototype:

```
void  PGA_SetGain(byte bGainSetting)
```

Assembler:

```
mov   A, bGainSetting
lcall  PGA_SetGain
```

Parameters:

bGainSetting: CY8C29/27/24/22xxx, CY8C23x33, CY8CLED04/08/16, and CY8CLED04D/01/02/03/04, symbolic names provided in C and assembly, and their associated values, are given in the following table. Programmed gain of 48.0 uses declared name of ....G48_0.

Symbolic Name	Value		Symbolic Name	Value
PGA_G48_0	0Ch		PGA_G1_00	F8h
PGA_G24_0	1Ch		PGA_G0_93	E0h
PGA_G16_0	08h		PGA_G0_87	D0h
PGA_G8_00	18h		PGA_G0_81	C0h
PGA_G5_33	28h		PGA_G0_75	B0h
PGA_G4_00	38h		PGA_G0_68	A0h
PGA_G3_20	48h		PGA_G0_62	90h
PGA_G2_67	58h		PGA_G0_56	80h
PGA_G2_27	68h		PGA_G0_50	70h
PGA_G2_00	78h		PGA_G0_43	60h
PGA_G1_78	88h		PGA_G0_37	50h
PGA_G1_60	98h		PGA_G0_31	40h
PGA_G1_46	A8h		PGA_G0_25	30h
PGA_G1_33	B8h		PGA_G0_18	20h
PGA_G1_23	C8h		PGA_G0_12	10h
PGA_G1_14	D8h		PGA_G0_06	00h
PGA_G1_06	E8h			

Return Value:

None

Side Effects:

Gain will be reset to 1.0 during routine then programmed to desired value. The A and X registers may be altered by this function.

PGA_Stop

Description:

Powers the user module off.

C Prototype:

```
void  PGA_Stop(void)
```

Assembler:

```
lcall  PGA_Stop
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

PGA_EnableAGNDBuffer

Description:

Enables AGND Buffer. This function is applicable only to CY8C28xxx devices.

Make sure, if AGND is used as a source for Input or Reference then AGND Buffer must be enabled by this API function.

C Prototype:

```
void  PGA_EnableAGNDBuffer(void)
```

Assembler:

```
lcall  PGA_EnableAGNDBuffer
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

PGA_DisableAGNDBuffer

Description:

Disables AGND Buffer. This function is applicable only to CY8C28xxx devices.

Make sure, if AGND is used as a source for Input or Reference then AGND Buffer must be enabled by PGA_EnableAGNDBuffer API function.

C Prototype:

```
void  PGA_DisableAGNDBuffer(void)
```

Assembler:

```
lcall  PGA_DisableAGNDBuffer
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

Sample Firmware Source Code

The sample code creates an amplifier with the gain fixed to 8.00, over-riding the gain value set in the PSoC Designer configuration screen.

```
;;-------------------------------------------------------------------
;; Sample Code for the PGA.
;; Turn on power and set gain to 8.00.
;;-------------------------------------------------------------------

export _main

include "m8c.inc"
include "PSoCAPI.inc"

_main:


mov  A, PGA_G8_00            ; specify amplifier gain
call PGA_SetGain             ; update amplifier gain

mov  A, PGA_MEDPOWER         ; specify PGA power level
call PGA_Start               ; and turn it on

ret
```

The equivalent code in C is:

```
//-------------------------------------------------------------------
// Sample C Code for the PGA.
// Turn on power and set gain to 8.00.
//-------------------------------------------------------------------

#include <m8c.h>        // part specific constants and macros
#include "PSoCAPI.h"    // PSoC API definitions for all user modules


void main(void)
{
    PGA_SetGain(PGA_G8_00);
    PGA_Start(PGA_MEDPOWER);

// User program ...
}
```

Configuration Registers

The topology of the PGA User Module sets most of the bits in the configuration registers for the chosen Analog CT PSoC block. These include values for opamp compensation, comparator mode, and feedback connection.

Table 5. Block GAIN Register: CR0

Bit	7	6	5	4	3	2	1	0
Value	GAIN					1	Reference	

GAIN sets the gain value per selection. Reference sets the reference point (effective "ground") for gain.

Table 6. Block GAIN Register: CR1

Bit	7	6	5	4	3	2	1	0
Value	AnalogBus	0	1	0	0	Input		

AnalogBus determines whether the GAIN PSoC block drives the bus. The value of this bit-field is determined by the choice made for the parameter of the same name in user module Placement mode of the Device Editor. Input is the value selected in PSoC Designer.

Table 7. Block GAIN Register: CR2

Bit	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	Power	

Power is set to ‘Off’ following device reset and configuration. It is modified by calling Start, SetPower, or Stop functions in the API.

Table 8. Block GAIN Register: CR3

Bit	7	6	5	4	3	2	1	0
Value	0	0	AGND_PD	0	LPCMPEN	CMOUT	INSAMP	EXGAIN

The AGND_PD is used to power down AGND buffer in CT block (only to CY8C28xxx devices). The EXGAIN bit is automatically set when ever a gain of 24 or 48 is selected.

Version History

Version	Originator	Description
3.2	DHA	Added DRC to check if AGND is disabled.

Note PSoC Designer 5.1 introduces a Version History in all user module datasheets. This section documents high level descriptions of the differences between the current and previous user module versions.

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