EzI2C Slave Datasheet EzI2Cs V 1.50

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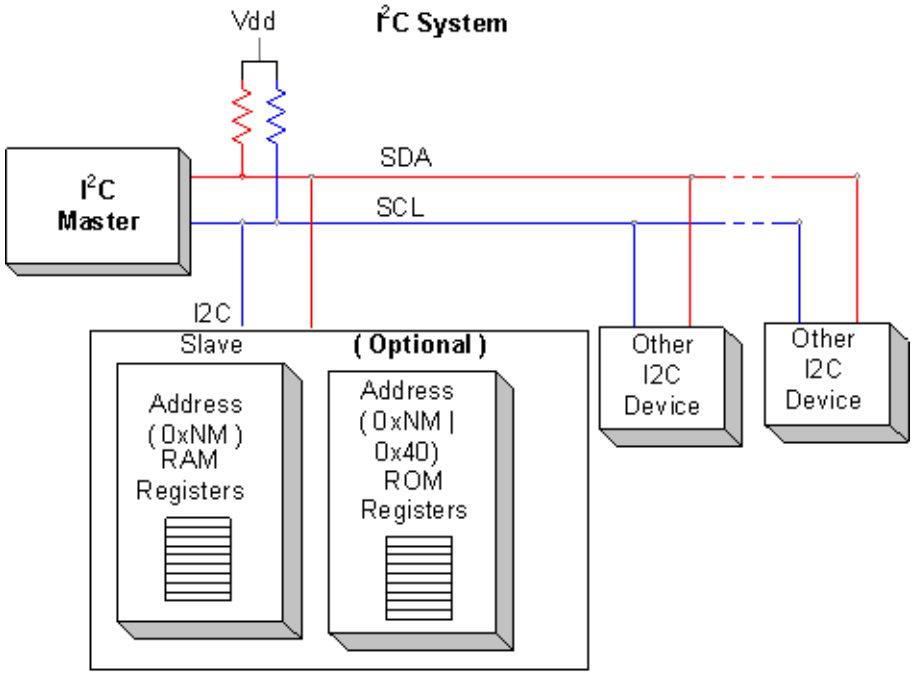
Resources	PSoC® Blocks				API Memory (Bytes)		Pins per senor
	CapSense®	I2C/SPI	Timer	Comparator	Flash	RAM	
CY8C20x66, CY8C20x36, CY8C20336AN, CY8C20436AN, CY8C20636AN, CY8C20xx6AS, CY8C20XX6L, CY8C20x46, CY8C20x96, CY8C20045, CY8C20055, CY7C643/4/5xx, CY7C60413, CY7C60424, CY7C6053x, CYONS2010, CYONS2011, CYONSFN2051, CYONSFN2053, CYONSFN2061, CYONSFN2151, CYONSFN2161, CYONSFN2162, CY8CTST200, CY8CTMG2xx, CY8CTMA30xx, CYONSFN2010-BFXC, CYONSCN2024-BFXC, CYONSCN2028-BFXC, CYONSCN2020-BFXC, CYONSKN2033-BFXC, CYONSKN2035-BFXC, CYONSKN2030-BFXC, CYONSTN2040, CY8CTMA140, CY8C20xx7/S, CYRF89x35, CY8C20065, CY8C24x93, CY7C69xxx							
RAM Read/Write Buffers	–	1	–	–	264	6	2
Additional for ROM Buffer Support	–	1	–	–	379	6	2

Features and Overview

- Industry standard Philips I^2C bus compatible interface
- Emulates common I^2C EEPROM interface
- Only two pins (SDA and SCL) required to interface to I^2C bus
- Standard data rate of 100/400 kbps
- High level API requires minimal user programming

The EzI2Cs User Module implements an I^2C register-based slave device. The I^2C bus is an industry standard, two-wire hardware interface developed by Philips® (now NXP).The master initiates all communication on the I^2C bus and supplies the clock for all slave devices. The EzI2Cs User Module supports the standard mode with speeds up to 400 kbps. No digital or analog PSoC blocks are consumed with this module. The EzI2Cs User Module is compatible with multiple devices on the same bus.

Figure 1. I²C Block Diagram



Single I2C Slave Device (Address 0xNM)
Shown with RAM registers and optional ROM registers

Functional Description

The EzI2Cs User Module takes a different approach from the I2CHW User Module provided with PSoC Designer. This user module supports only an I²C slave configuration with one or two I²C addresses. The first I²C address accesses the RAM allocated area and the optional second I²C address accesses the ROM area. The second I²C address is the RAM area I²C address OR'ed with 0x40. For example, if you select an I²C address of 0x15, the RAM area I²C address is 0x15 and the optional ROM I²C address is 0x55.

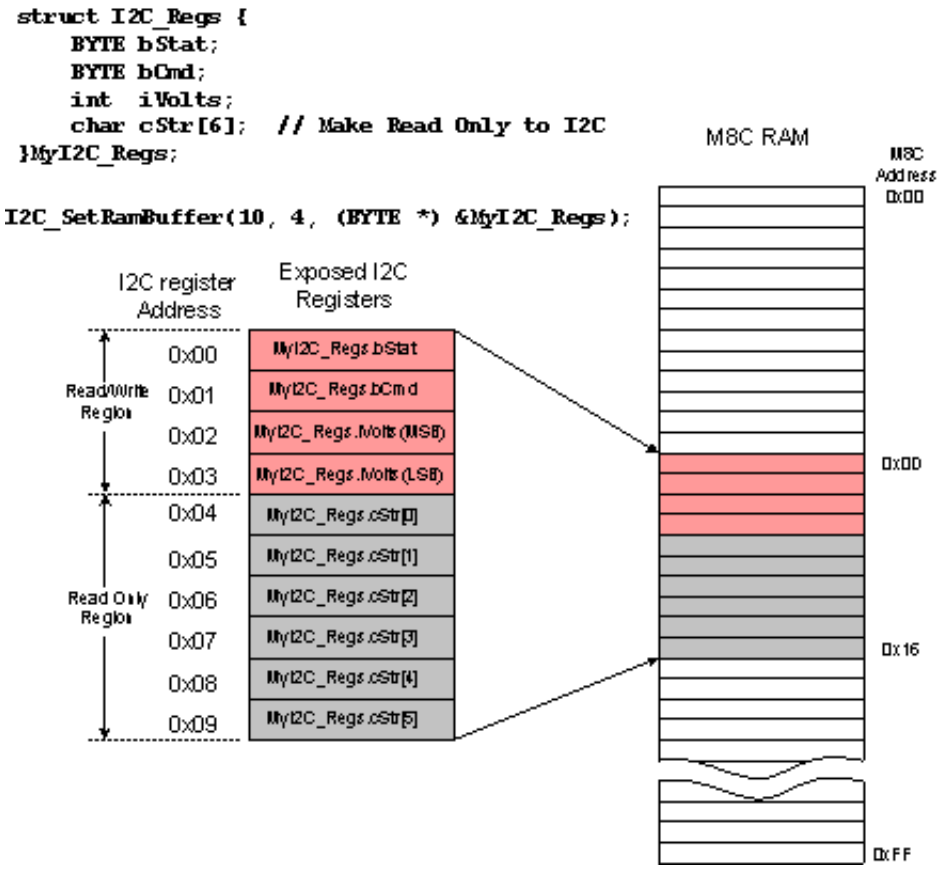
This user module requires that you enable global interrupts since the I²C hardware is interrupt driven. Even though this user module requires interrupts, the user's code does not need to add any code to the ISR (Interrupt Service Routine). The module services all interrupts (data transfers) independent of the user's code. Instead, the memory buffers allocated for this interface look like simple dual port memory between the user's application and the I²C Master.

If required, a user can create a higher-level interface between a master and this slave by defining semaphores and command locations in the data structure.

RAM Area Interface

To an I²C master the interface looks very similar to a common 256 byte I²C EEPROM. The PSoC API is treated as RAM that can be configured as simple variables, arrays, or structures. In a sense it acts as a shared RAM interface between the user's program and an I²C master on the I²C bus. The API allows the user to expose any data structure to an I²C Master. The user module only allows the I²C master to access the specified area of RAM and prevents any reads or writes outside that area. The data exposed to the I²C interface can be a single variable, an array of values, or a structure. All that is required is a pointer to the start of the variable or data structure when initialized. See the following figure:

Figure 2. RAM Area Interface



For example, a user could create this structure:

```
struct I2C_Regs {   // Example I2C interface structure
    BYTE bStat;
BYTE bCmd;
int  iVolts;
char cStr[6];  // Read only string
} MyI2C_Regs;
```

This structure may contain any group of variables with any name as long as it is contiguous in memory and referenced by a pointer. The interface (I²C Master) only sees it as an array of bytes, and cannot access any memory outside the defined area. Using the example structure above, a supplied API is used to expose the data structure to the I²C interface. The first parameter sets the size of the exposed RAM to the I²C interface, in this case it is the entire structure. The second parameter sets the boundary between

the read/write and read only areas by setting the number of bytes in the read/write area. The read/write area is first, followed by the read only area. In this case, only the first 4 bytes may be written to, but all bytes may be read by the I^{2}C master. The third parameter is a pointer to the data.

```
EzI2Cs_SetRamBuffer(sizeof(MyI2C_Regs), 4,(BYTE *) &MyI2C_Regs);
```

In the following example a 15-byte array is created and exposed to the I^{2}C interface. The first 8 bytes of the array are read/write, and the remaining 7 bytes are read only.

```
char theArray[15];
EzI2Cs_SetRamBuffer(15, 8, (BYTE *) theArray);
```

The following example is a very simple example where only a single integer (2 bytes) is exposed. Both bytes are readable and writable by the I^{2}C master.

```
int iRegister;
EzI2Cs_SetRamBuffer(2, 2, (BYTE *) (&iRegister);
```

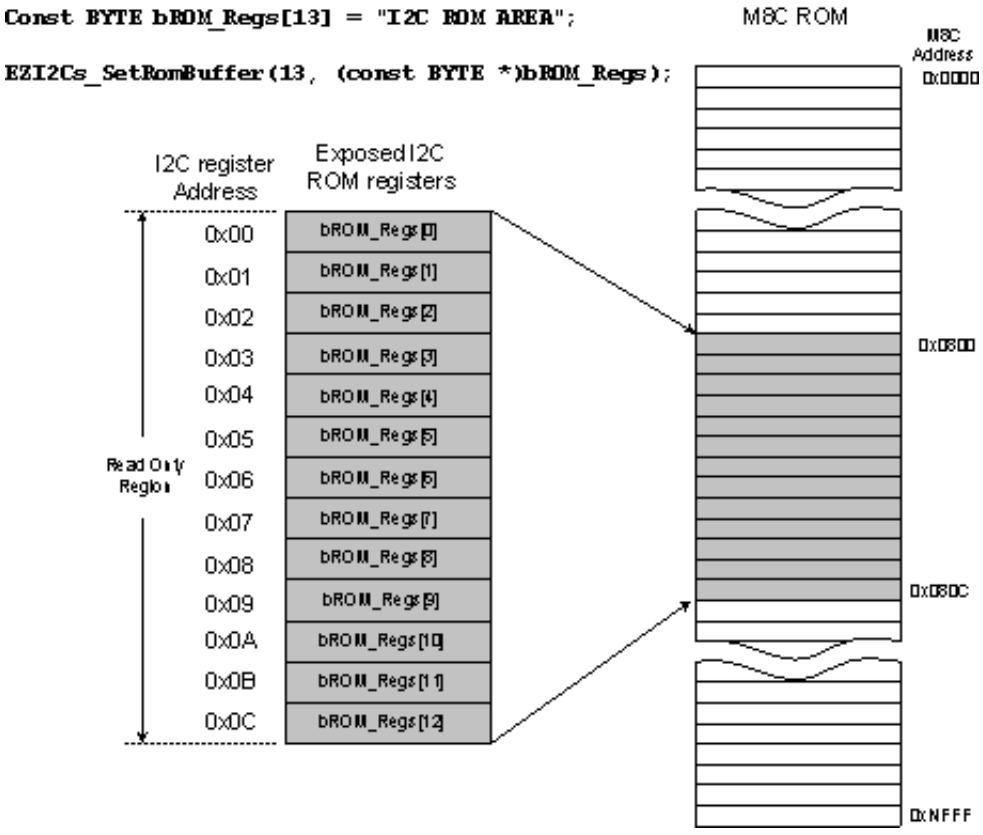
ROM Area Interface (Optional)

The ROM interface is almost identical to the RAM interface, except that it is read only. As seen in the following example, the SetRomBuffer function is similar to the SetRamBuffer function. In this example, the data area is a simple constant string 13 bytes in length counting the terminating NULL (0x00) character.

```
const BYTE bROM_Regs[13] = "I2C ROM AREA";
EzI2Cs_SetRomBuffer(13, (const BYTE *)bROM_Regs);
```

As mentioned before, the ROM area has its own I²C address. This address is simply the RAM area address OR'ed with 0x40. If the main RAM address is 0x15, the I²C address to access the ROM area would be 0x55. The following diagram shows how this example may appear in memory:

Figure 3. ROM Area Interface



Interface as Seen by External Master

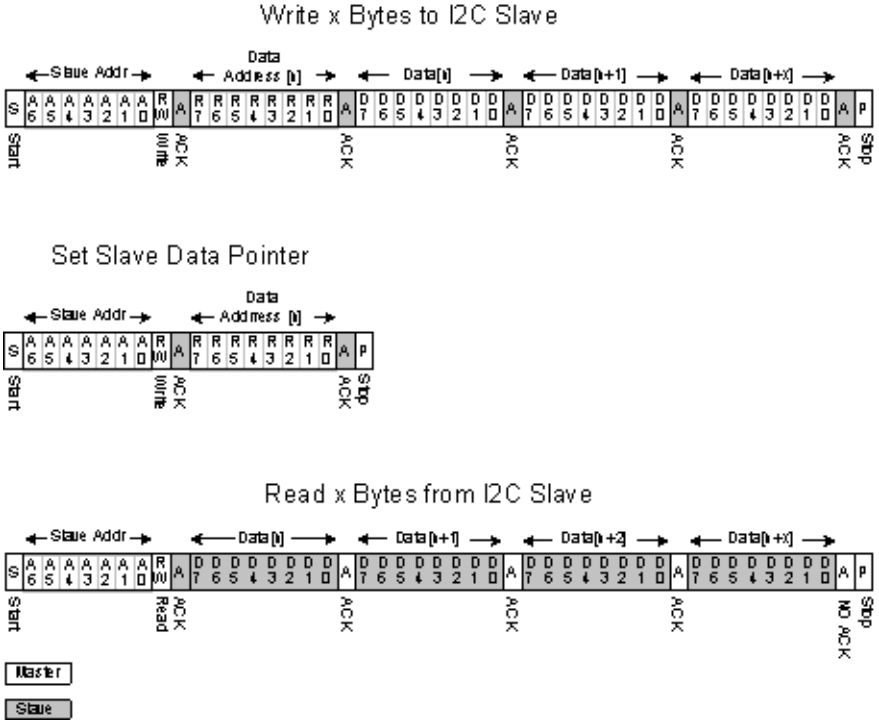
The EzI2Cs User Module supports basic read and write operations for the RAM area and read only operations for the ROM area. The RAM and ROM area interfaces contain separate data pointers that are set with the first data byte of a write operation. Even the ROM area accepts a single byte write to set the data pointer. When writing one or more RAM bytes, the first data byte is always the data pointer. The byte after the data pointer is written into the location pointed to by the data pointer byte. The third byte (second data byte) is written to the data pointer plus 1 and so on. This data pointer increments for each byte read or written but is reset to the first value written at the beginning of each new read operation. A new read operation begins to read data at the location pointed to by the data pointer.

For example, if the data pointer is set to four, each read operation resets the data pointer to four and reads sequentially from that location until the end of the data or until the host completes the read operation. This is true whether a single or multiple read operations are performed. The data pointer is not changed until a new write operation is initiated.

If the I²C master attempts to write data past the area specified by the SetRamBuffer() function, the data is discarded and does not affect any RAM inside or outside the designated RAM area. Data cannot be read outside the allowed range. Any read requests by the master, outside the allowed range, results in the return of invalid.

The following diagram illustrates the bus communication for a data write, data pointer write, and a data read operation. Remember that a data write operation always rewrites the data pointer.

Figure 4. Write and Read x Bytes to I2C Slave



At reset, or power on, the EzI2Cs User Module is configured and APIs are supplied, but the resource must be explicitly turned on using the EzI2Cs_Start() function.

The I^2C resource supports data transfer at a byte-by-byte level. At the end of each address or data transmission/reception, status is reported or a dedicated interrupt may be triggered. Status reporting and interrupt generation depend upon the direction of data transfer and the condition of the I^2C bus as detected by the hardware. Interrupts may be configured to occur on byte-complete, or bus-error detection.

Every I^2C transaction consists of a Start, Address, R/W Direction, Data, and a Termination. For an I^2C slave, an interrupt occurs after the 8th bit of incoming data. At this point a receiving device must decide to acknowledge (ACK) or not-acknowledge (NAK) the incoming byte whether it is an address or data. The receiving device then writes appropriate control bits to the I2C_SCR register, informing the I^2C resource of the ack/nak status. The write to the I2C_SCR register paces data flow on the bus by installing the bus, placing the ack/nak status on the bus and shifting the next data byte in. For the second case of a transmitter, an interrupt occurs after an external receiving device provided an ack or nak. The I2C_SCR may be read to determine the status of this bit. For a transmitter, data is loaded into the I2C_DR register and the I2C_SCR register is again written to trigger the next portion of the transmission.

Detailed descriptions of the I^2C bus and the implementation here are available in the complete I^2C specification available on the NXP web site, and by referring to the device datasheet supplied with PSoC Designer.

Design Considerations

Set the main oscillator to any clock speed. Data throughput may be affected by processor speed but byte-by-byte data transfer operates at the specified I^2C speed.

Dynamic Reconfiguration

Do not incorporate the EzI2Cs resource into dynamically loaded or unloaded overlays. Place the EzI2Cs resource as part of the base configuration only. Operation of the EzI2Cs block may be modified as operational requirements dictate, but attempting to remove the resource as part of dynamic reconfiguration may result in adverse effects on external I^2C devices. It is also possible to accidentally reconfigure pins assigned for I^2C; doing this disables the I^2C functions. Take care to avoid this possibility when switching between configurations.

Sleep and I2C Operation

CY8C20xx7/S family of device supports wake up on I2C slave address match event. This feature helps to wake the device up sleep when host is tried to access CY8C20xx7/S device. To make this feature work, power to I2C block should be turned on by setting I2C_ON bit in SLP_CFG2 register and auto NACK feature should be set before entering into sleep. When device is in sleep, upon the address match event, device will NACK address and also wakeup from sleep (only if received address is matched). Once device woken up from sleep, auto NACK will be automatically disabled.

Example code is provided in section “Example C Code: To enable wakeup sleep using I2C address match event”.Not setting Auto NACK for I2C block before entering sleep will corrupt traffic on I2C bus.

DC and AC Electrical Characteristics

Refer to the device datasheet for your PSoC Device for the electrical characteristics of the I^2C interface.

As the block diagram illustrates, the I^2C bus requires external pull-up resistors. The pull-up resistor values (R_P) are determined by the supply voltage, clock speed, and bus capacitance. Make the minimum sink current for any device (master or slave) no less 3 mA at V_{OLmax} = 0.4V for the output stage. This limits the minimum pull-up resistor value for a 5V system to about 1.5 kΩ. The maximum value for R_P depends upon the bus capacitance and clock speed. For a 5V system with a bus capacitance of 150 pF, the pull-up resistors are no larger than 6 kΩ. For more information on "The I^2C-Bus Specification", see the NXP web site at www.nxp.com.

Note Purchase of I^2C components from Cypress or one of its sublicensed Associated Companies, conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by NXP.

Placement

The EzI2Cs User Module does not require any digital or analog PSoC blocks. There are no placement restrictions. Multiple placements of I^2C modules are not possible since the I^2C module uses a dedicated PSoC resource block and interrupt.

Parameters and Resources

Slave_Addr

Selects the 7-bit slave address that is used by the I^2C master to address the slave. Valid selections are from 0 to 127 (in decimal format) if only the RAM registers are used. If the ROM registers are enabled, only addresses between 0 and 63 are valid because the ROM register space is the RAM address plus 64 (64 to 127 in decimal format).

Address_Type

Selects whether the address is static or dynamic. If set to static, the I^2C address cannot be changed, but one byte of RAM is saved. Setting this option to dynamic enables the firmware to change the address at any time. This option is generally for applications where external resistors or dip switches are used to set the LSBs of the I^2C address.

ROM_Registers

The RAM area is always enabled, but you may enable a second address that allows you to access constants in the ROM area. Choose the enable option for this parameter if the ROM address is desired. If not choose disable.This second address is the base address OR'ed with 0x40. Access to ROM area is not operable if the HW address recognition feature is used. Therefore, the ROM_Registers parameter is disabled if the HW Addr Rec parameter is enabled.

HW Addr Rec

This parameter enables or disables the hardware I^2C slave address recognition feature. It also allows decreasing the ROM/RAM usage and decreasing the time of I^2C ISR executing. This parameter is disabled if the ROM_Registers parameter is enabled.

I2C_Clock

This parameter selects the clock speed used with this slave. Options are 50 KHz, 100 KHz, or 400 KHz. The 400-KHz speed can only be used when IMO (SysClk) is 12 MHz.

I2C_Pin

Selects the pins from Port 1 for use with I^2C signals. There is no need to select the proper drive mode for the pins. PSoC Designer does this automatically. This allows you to place the I^2C clock and data signals on P1[5] - P1[7] or P1[1] - P1[0].

Application Programming Interface

To guarantee the data integrity of variables with length of 2 or more bytes, check the EzI2Cs_bBusy_Flag variable before changing values of such variables in code, for example:

```
EzI2Cs_DisableInt();
if(!(EzI2Cs_bBusy_Flag == EzI2Cs_I2C_BUSY_RAM_READ))
{
data.wData1++; //safely increment some 2 byte variable
}
EzI2Cs_ResumeInt();
```

Note that interrupts must be disabled to prevent an I2C read transaction from starting after the flags are checked, but before the data is modified. With interrupts disabled, if an I2C transaction does start during this time, clock stretching will be used on the I2C bus until after the interrupt is resumed.

The EzI2Cs_bBusy_Flag variable is updated automatically in the ISR and has the following predefined values:

Table 1. Predefined values of EzI2Cs_bBusy_Flag variable

Symbol Name	Value	Description
I2C_FREE	0x00	No transaction at the current moment
I2C_BUSY_RAM_READ	0x01	RAM read transaction in progress
I2C_BUSY_RAM_WRITE	0x02	RAM write transaction in progress
I2C_BUSY_ROM_READ	0x04	ROM read transaction in progress
I2C_BUSY_ROM_WRITE	0x08	ROM write transaction in progress

EzI2Cs_Start

Description:

Enables the I^2C slave and enable interrupts. Call the required EzI2Cs_SetRamBuffer() function before this function call.

C Prototype:

```
void  EzI2Cs_Start(void);
```

Assembler:

```
lcall EzI2Cs_Start
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_Stop

Description:

Disables the EzI2Cs by disabling the I^2C interrupt and disabling the slave functionality of the I^2C block, to re-enable the slave, call EzI2Cs_Start().

C Prototype:

```
void   EzI2Cs_Stop(void);
```

Assembler:

```
lcall  EzI2Cs_Stop
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_DisableSlave

Description:

Disables the EzI2Cs without disabling the I^2C interrupt.

C Prototype:

```
void   EzI2Cs_DisableSlave(void);
```

Assembler:

```
lcall  EzI2Cs_DisableSlave
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_SetAddr

Description:

This function sets the address that is recognized by the EzI2Cs User Module. This command is only valid if the Address_Type is set to Dynamic in the parameters. Call this function only after the EzI2Cs_Start() function. This is because the start function sets the default address and this function overwrites that address. This function is optional and only needed if you change the address from the default.

C Prototype:

```
void  EzI2Cs_SetAddr(BYTE bAddr);
```

Assembler:

```
mov    A,0x05             ; Set I2C slave address to 0x05
lcall  EzI2Cs_SetAddr
```

Parameters:

BYTE char: Slave address between 1 and 127.

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_GetActivity

Description:

This function returns a nonzero value if an I^2C read or write cycle occurred since last time this function was called. The activity flag resets to zero at the end of this function call.Symbolic constants are provided in C and assembly. Their values are defined as:

Symbol	Value	Meaning
EzI2Cs_ANY_ACTIVITY	0x80	Either a write cycle or a read cycle occurred
EzI2Cs_READ_ACTIVITY	0x20	A read cycle occurred
EzI2Cs_WRITE_ACTIVITY	0x10	A write cycle occurred

C Prototype:

```
BYTE EzI2Cs_GetActivity(void);
```

Assembler:

```
lcall  EzI2Cs_GetActivity     ; Return value in A
```

Parameters:

None.

Return Value:

Returns a nonzero value if an I^2C read or write has occurred. Returns zero if no activity has occurred since the last time the function was called.

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_GetAddr

Description:

This function returns the current address of this I^2C slave. This function is optional and is usually only required if the application must determine the current or default address.

C Prototype:

```
BYTE EzI2Cs_GetAddr(void);
```

Assembler:

```
lcall  EzI2Cs_GetAddr     ; Return value in A
```

Parameters:

None.

Return Value:

The current I^2C address of this I^2C slave

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_EnableInt

Description:

Enables I^2C interrupt allowing start condition detection. Remember to call the global interrupt enable function by using the macro: M8C_EnableGInt. This function is not required if the EzI2Cs_Start func-

tion is called. By default this function clears pending interrupts. To avoid clearing pending interrupts see the ResumeInt function.

C Prototype:

```
void   EzI2Cs_EnableInt(void);
```

Assembler:

```
lcall  EzI2Cs_EnableInt
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_ResumeInt

Description:

Enables I^2C interrupt allowing start condition detection. This function does not clear pending interrupts before enabling interrupts. Remember to call the global interrupt enable function by using the macro: M8C_EnableGInt. This function is not required if the EzI2Cs_Start function is called.

C Prototype:

```
void   EzI2Cs_ResumeInt(void);
```

Assembler:

```
lcall  EzI2Cs_ResumeInt
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_DisableInt

Description:

Disables I^2C's slave by disabling the I^2C interrupt.

C Prototype:

```
void   EzI2Cs_DisableInt(void);
```

Assembler:

```
lcall EzI2Cs_DisableInt
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_SetRamBuffer

Description:

This function sets the location and size of the RAM buffer (up to 255 bytes) that is exposed to an I^2C master. This function is required and called before calling EzI2Cs_Start().

C Prototype:

```
void EzI2Cs_SetRamBuffer(BYTE bSize, BYTE bRWboundary, (BYTE *)pAddr);
```

Assembler:

```
lcall  EzI2Cs_SetRamBuffer
```

Parameters:

BYTE bSize: Size of the data structure exposed to an I^2C master. The minimum value for bSize is 1 and the maximum is 255.

BYTE bRWboundary: The size of the writable area which starts from the location pointed by *pAddr". This value should always be less than or equal to bSize for proper operation.

BYTE * pAddr: A pointer to the data structure.

Return Value:

None

Side Effects:

The A and X registers may be altered by this function. If RWboundary is set to a value larger than bSize, the entire RWboundary size is writable. Setting bSize to the invalid value of 0 may allow the I2C host to write to undefined memory locations.

EzI2Cs_SetRomBuffer

Description:

This function sets the location and size of the ROM buffer (up to 255 bytes) that is exposed to an I^2C master. This function is required before enabling the EzI2Cs_Start function if ROM use is desired.

C Prototype:

```
void EzI2Cs_SetRomBuffer(BYTE bSize,(const BYTE *)pAddr);
```

Assembler:

```
lcall  EzI2Cs_SetRomBuffer
```

Parameters:

BYTE bSize: Size of the data structure exposed to an I^2C master. const BYTE * pAddr: A pointer to the data structure in flash ROM.

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_SetAutoNACK (only for CY8C20xx7/S device families)

Description:

This function sets the respective bit to engage the auto NACK (also referred as force NACK) feature in I2C slave block. Auto NACK may not be activated immediately and will be active only upon the next byte boundary.

C Prototype:

```
void EzI2Cs_SetAutoNACK(void)
```

Assembler:

```
lcall EzI2Cs_SetAutoNACK
```

Parameters:

None.

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_ClearAutoNACK (only for CY8C20xx7/S device families)

Description:

This function clears the respective bit to disable auto NACK feature in I2C slave block.

C Prototype:

```
void EzI2Cs_ClearAutoNACK(void)
```

Assembler:

```
lcall EzI2Cs_ClearAutoNACK
```

Parameters:

None.

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

EzI2Cs_bCheckStatus (only for CY8C20xx7/S device families)

Description:

This function returns a value that indicates status of I2C data transaction.

C Prototype:

```
BYTE  EzI2Cs_bCheckStatus(void)
```

Assembler:

```
lcall  EzI2Cs_bCheckStatus
```

Parameters:

None.

Return Value:

The status of I2C data transaction: four bits in one byte return value indicates the below information as using I2C_XSTAT register. Symbolic names used for the bits are mentioned below.

Symbol	Value	Description
EzI2Cs_BUS_BUSY	0x80	This bit is set only if there is an ongoing I2C traffic on bus
EzI2Cs_AUTO_NACK_ON	0x04	This bit is set only if auto NACK feature is activated by I2C block
EzI2Cs_LAST_TX_RD	0x20	This bit is set if last I2C transaction by host is a read operation
EzI2Cs_LAST_TX_WR	0x40	This bit is set if last I2C transaction by host is a write operation

Note: If the EzI2Cs_AUTO_NACK_ON bit is set then all other status bits are cleared automatically.

Side Effects:

The A and X registers may be altered by this function.

Sample Firmware Source Code

Example C Code:

```
//*****************************************************
// Example code to demonstrate the use of the EzI2Cs UM
//
// This code sets up the EzI2Cs slave to expose both
// a RAM and a ROM data structure.  The RAM structure is
// addressed at I2C address 0x05, and the ROM structure
// is at I2C address 0x45.
//
// * The instance name of the EzI2Cs User Module is "EzI2Cs".
// * The "Address_Type" parameter is set to "Dynamic"
// * The "ROM_Registers" parameter is set to "Enable"
//
// NOTE: to guarantee data integrity of variables with length 2 or more
// bytes check the EzI2Cs_bBusy_Flag variable before changing values of such
// variables.//*************************************************************

#include <m8c.h>        // Part specific constants and macros
```

```
#include "PSoCAPI.h"    // PSoC API definitions for all User Modules

struct I2C_Regs {    // Example I2C interface structure
    BYTE bStat;
    BYTE bCmd;
    int  iVolts;
    char cStr[6];    // Read only string
} MyI2C_Regs;

const BYTE DESC[] = "Hello I2C Master";

void main(void)
{
    // Set up RAM buffer
   EzI2Cs_SetRamBuffer(sizeof(MyI2C_Regs), 4, (BYTE *) &MyI2C_Regs);
   EzI2Cs_SetRomBuffer(sizeof(DESC), DESC);   // Set up ROM buffer

   M8C_EnableGInt ;                           // Turn on interrupts

   EzI2Cs_Start();                            // Turn on I2C
   EzI2Cs_SetAddr(5);                         // Change address to 5

   while(1) {
      // Place user code here to update and read structure data.
   }
}
```

Example C Code: wakeup sleep using I2C address match event (only for CY8C20xx7/S device families)

```
//*-----------------------------------------------------------
// Example code to demonstrate wakeup sleep using I2C address match event
//
// This code sets up the EzI2Cs slave to expose
// a RAM data structure.  The RAM structure is
// addressed at I2C address 0x05.
//
// * The instance name of the EzI2Cs User Module is "EzI2Cs".
// * The "Slave_Addr" parameter is set to "5"
// * The "Address_Type" parameter is set to "Static"
// * The "ROM_Registers" parameter is set to "Disable"
// * The "HW Addr Rec" parameter is set to "Enable"
// NOTE: To guarantee data integrity of variables with length 2 or more
// bytes check the EzI2Cs_bBusy_Flag variable before changing values of such
// variables.
//*-----------------------------------------------------------

#include <m8c.h>        // Part specific constants and macros
#include "PSoCAPI.h"    // PSoC API definitions for all User Modules

struct I2C_Regs {    // Example I2C interface structure
    BYTE bCmd;
    BYTE bStat;
} MyI2C_Regs;
```

```
void main(void)
{
  EzI2Cs_SetRamBuffer(sizeof(MyI2C_Regs), 4, (BYTE *) &MyI2C_Regs); // Set up RAM buffer
   M8C_EnableGInt ;                    // Turn on interrupts
EzI2Cs_Start();                      // Turn on I2C
  SLP_CFG2 |= SLP_CFG2_I2C_ON;         // Set bit to power I2C block during M8C sleep.

// infinite loop
  while(1)
{
         // Device will fall asleep once non-zero MyI2C_Regs.bCmd is received.
         if(MyI2C_Regs.bCmd)
         {
                 MyI2C_Regs.bCmd = 0;

    // Set auto NACK and check if auto NACK is engaged
                 EzI2Cs_SetAutoNACK();
                 while (! (EzI2Cs_AUTO_NACK_ON & EzI2Cs_bCheckStatus()));

    // enter device into sleep
          M8C_Sleep;
          }
          // Device will be woken up with I2C address match event and auto
// NACK will be automatically disabled upon wakeup

          // Place user code here to update and read structure data.
          MyI2C_Regs.bStat++;
    }
}
```

Example ASM Code:

```
;-------------------------------------------------------------------------
; Example code to demonstrate the use of the ExI2Cs UM
;
; This code sets up the EzI2Cs slave to expose both
; a RAM and a ROM data structure.  The RAM structure is
; addressed at I2C address 0x05, and the ROM structure
; is at I2C address 0x45.
;
; * The instance name of the EzI2Cs User Module is "EzI2Cs".
; * The "Address_Type" parameter is set to "Dynamic".
; * The "ROM_Registers" parameter is set to "Enable".
;
; NOTE: to guarantee data integrity of variables with length 2 or more
; bytes check the EzI2Cs_bBusy_Flag variable before changing values of such
; variables.
;-------------------------------------------------------------------------

include "m8c.inc"       ; part specific constants and macros
include "memory.inc"    ; Constants & macros for SMM/LMM and Compiler
include "PSoCAPI.inc"   ; PSoC API definitions for all User Modules

area bss (RAM, REL, CON)        ; Allocate Variables & define constants
RAM_BUF_SIZE:     equ  10       ; Top of ramp value
```

```
BUF_RW_SIZE:      equ   5       ; Only first five bytes writable from I2C Master

I2C_RAM_Buf:  blk  RAM_BUF_SIZE ; Reserve RAM for I2C buffer

area text (ROM, REL, CON)

.LITERAL
I2C_ROM_BUF:                    ; I2C ROM Buffer
   DB  11h, 22h, 33h, 44h, 55h, 66h, 77h, 88h
.ENDLITERAL
ROM_BUF_SIZE:     equ   8

export _main

_main:
    ; Set RAM Buffer
    mov    A,>I2C_RAM_Buf       ; Save MSB of RAM buffer address
    push   A
    mov    A,<I2C_RAM_Buf       ; Save LSB of RAM buffer address
    push   A
    mov    A,BUF_RW_SIZE        ; Save RW size param
    push   A
    mov    A,RAM_BUF_SIZE      ; Save I2C buffer size
    push   A
    call   EzI2Cs_SetRamBuffer
    ADD    SP,-4                ; Reset Stack

; Set ROM Buffer
    mov    A,>I2C_ROM_BUF       ; Save MSB of ROM buffer address
   push  A
    mov    A,<I2C_ROM_BUF       ; Save LSB of ROM buffer address
    push   A
    mov    A,ROM_BUF_SIZE       ; Save ROM buffer size
    push   A
    call   EzI2Cs_SetRomBuffer
    add    SP,-3                ; Reset Stack

M8C_EnableGInt              ; Enable Global Interrupts

call   EzI2Cs_Start         ; Start and enable IRQ
    mov    A,5                ; Set address to 5
    call   EzI2Cs_SetAddr

.Loop:

    ;; User Code goes here

jmp    .Loop
```

Configuration Registers

This section describes the PSoC Resource Registers used or modified by the EzI2Cs User Module. The use of these registers is not required when using the EzI2Cs User Module but is provided as a reference.

Table 2. Resource I2C_CFG: Bank 0 reg[D6] Configuration Register

Bit	7	6	5	4	3	2	1	0
Value	Reserved	PinSelect	Bus Error IE	Stop IE	Clock Rate[1]	Clock Rate[0]	0	Enable Slave

Pin Select: selects either SCL and SDA as P1[5] - P1[7] or P1[1] - P1[0].

Bus Error Interrupt Enable: enable I^2C interrupt generation on a Bus Error.

Stop Error Interrupt Enable: enable an I^2C interrupt on an I^2C Stop condition.

Clock Rate[1,0]: select among three valid Clock rates 50, 100, 400 kbps.

Enable Slave: enable the I^2C HW block as a bus Slave.

Table 3. Resource I2C_SCR: Bank 0 reg[D7] Status Control Register

Bit	7	6	5	4	3	2	1	0
Value	Bus Error	NA	Stop Status	ACK out	Address	Transmit	Last Recd Bit (LRB)	Byte Complete

Bus Error: indicates the detection of a Bus Error condition.

Stop Status: indicates the detection of an I^2C stop condition.

ACK out: direct the I^2C block to Acknowledge (1) or Not Acknowledge (0) a received byte.

Address: received or transmitted byte is an address.

Last Received Bit (LRB): the value of last received bit (bit 9) in a transmit sequence, status of Ack/Nak from destination device.

Byte Complete: 8 data bits were received. For Receive Mode, the bus is stalled waiting for an Ack/Nak. For Transmit Mode Ack Nak was also received (see LRB) and the bus is stalled for the next action.

Table 4. Resource I2C_DR: Bank 0 reg[D8] Data Register

Bit	7	6	5	4	3	2	1	0
Value	Data							

Received or Transmitted data. To transmit data, you must load this register before a write to the I2C_SCR register. Received data is read from this register and may contain an address or data.

Version History

Version	Originator	Description
1.2	DHA	1. The default pin value of the "I2C Pin" parameter was removed, because it can destroy drive mode of corresponding pins initially set by other user modules. 2. Updated to prevent SCL getting stuck to low. 3. The following changes were done to the Start function: a. Changed Initial Open-Drain Low drive mode of user module pins to HI-Z analog. b. Enabled the I^2C block. c. Gave delay 5 nop instructions. d. Restored the Initial I^2C pin. 4. Added "Export EzI2C_StopSlave API" to *.h and *.inc file. 5. Added ability to update Output Pin through shadow register. 6. Updated RAM paging management. 7. Added RAM and ROM Offset Pointers initialization to Start API. 8. Added hardware address recognition feature.
1.30	DHA	Added User code sections to the EzI2Cs UM ISR file.
1.30.b	DHA	1. Updated EzI2Cs_Stop() and EzI2Cs_DisableInt() API function descriptions. 2. Updated predefined values of EzI2Cs_bBusy_Flag variable. 3. Corrected the example code of the EzI2Cs_bBusy_Flag usage. 4. Updated comments for the EzI2Cs_I2C_BUSY_ROM_READ and EzI2Cs_I2C_BUSY_ROM_WRITE constants definitions.
1.40	DHA	1. Added support for CY8C20xx7/7S devices. 2. The CY8C20xx7/7S devices contain a hardware fix for the interrupt collisionissue. The user module was updated to support this change. 3. Added new _SetAutoNACK(), _ClearAutoNACK(), and _bCheckStatus () API functions for the CY8C20xx7/7S device. 4. Added design rule check for allowed combinations of "HW Addr Rec" and "ROM-registers" parameter.
1.50	HPHA	1. Fixed User Module operation for CY8C20055 family. 2. Added CY8C24093 support.

Note PSoC Designer 5.1 introduces a Version History in all user module datasheets. This section documents high level descriptions of the differences between the current and previous user module versions.

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