Dual Input 7- to 13-Bit Incremental ADC Datasheet DualADC V 2.30

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Resources	PSoC® Blocks			API Memory (Bytes)		Pins (per External I/O)
	Digital	Analog CT	Analog SC	flash	RAM	
CY8C29/27/24xxx, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52						
	4	0	2	444	8	1

See application note “Analog - ADC Selection” AN2239 for other converters.

For one or more fully configured, functional example projects that use this user module go to www.cypress.com/psocexampleprojects.

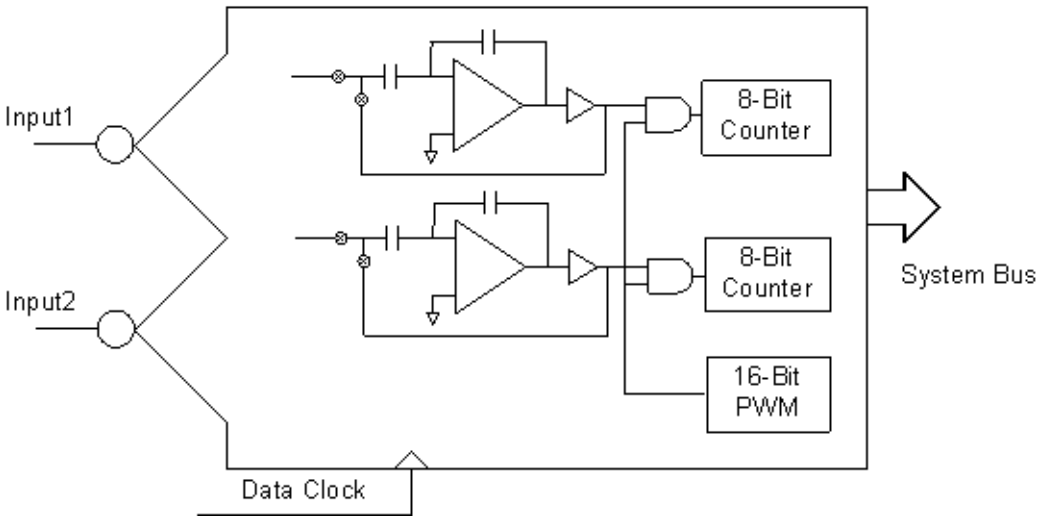
Features and Overview

- Samples two inputs simultaneously
- 7- to 13-bit resolution
- 2’s complement or unsigned integer
- Sample rates from 4 to greater than 10,000 sps
- Multiple input ranges including Vss to Vdd
- Integrating Converter provides good normal mode rejection
- Internal or external clock

The DualADC User Module is a dual input incremental ADC with an adjustable resolution between 7 and 13 bits. It can be configured to remove unwanted high frequencies by optimizing the integrate time. Input voltage ranges, including rail-to-rail, may be measured by configuring the proper reference voltage and analog ground. The output can be configured as 2’s complement or unsigned integer. The DualADC is ideal for applications that require simultaneous sampling of two signals, such as power measurement. As with other PSoC ADCs, signals to both inputs may be multiplexed. The CPU load varies with the input level. For example, when $V_{in} = +V_{ref}$, there are 10,014 CPU cycles (maximum 13 bit). When V_{in} = AGND, there are 5,278 CPU cycles (average 13 bit). When $V_{in} = -V_{ref}$, there are 542 CPU cycles (minimum 7-13 bit).

Figure 1. DualADC Block Diagram

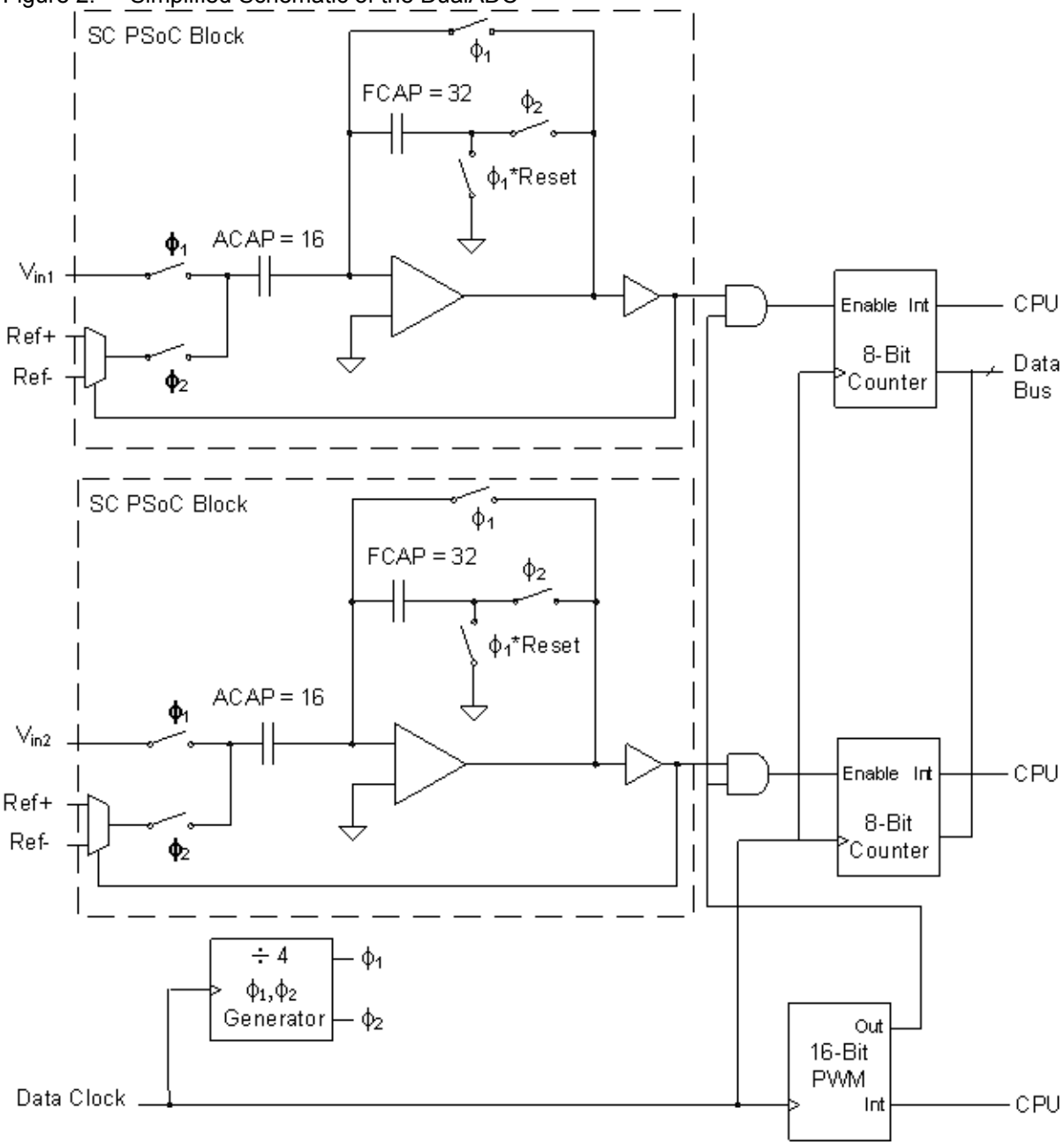
Review Placement Section Prior to Module Placement



Functional Description

The DualADC User Module is composed of two incremental ADCs in a single user module. The 16-bit sample rate timer (PWM) is shared to reduce the required digital blocks. Since both ADCs use the same timer, the sampling is fully synchronized. At the end of a conversion cycle, results for both inputs are available simultaneously. Four digital PSoC blocks and two analog switch cap PSoC blocks are required, see the figure below for a simplified schematic.

Figure 2. Simplified Schematic of the DualADC



The two analog blocks are configured identically as resettable integrators. Depending on the output polarity, the reference control is configured so that the reference voltage is either added or subtracted from the input and placed in the integrator. This reference control attempts to pull the integrator output back towards AGND. If the integrator is operated 2^{Bits} times and the output voltage comparator is positive “n" of those times, the residual voltage (V_{resid}) at the output is as follows.

Equation 1

$$V_{resid} = 2^{Bits} \cdot V_{in} - (n \cdot V_{ref}) + (2^{Bits} - n) \cdot V_{ref}$$

Equation 2

$$V_{in} = \frac{n - 2^{Bits-1}}{2^{Bits-1}} V_{ref} + \frac{V_{resid}}{2^{Bits}}$$

This equation states that the range of this ADC is ± V_{ref}, the resolution (LSB) is $V_{ref}/2^{Bits-1}$, and the voltage on the output at the end of the computation is defined as the residue. Since V_{resid} is always less than, V_{ref}, $V_{resid}/2^{Bits}$ is less than half an LSB and can be ignored. The resulting equation is listed below.

Equation 3

$$V_{in} = \frac{n - 2^{Bits-1}}{2^{Bits-1}} V_{ref}$$

Example 1

For a V_{ref} of 1.3V and a resolution of 8-bits we can easily calculate the input voltage based on the value read from the incremental ADC at the time the data is ready. The equation which can be used would be as follows:

Equation 4

$$V_{in} = \frac{n - 128}{128} 1.3$$

The result of the calculation will be referenced to AGND. For a ADC data value of 200 the Voltage measured can be calculated to be 0.73V as follows:

Equation 5

$$V_{in} = \frac{200 - 128}{128} 1.3 = 0.73V$$

The value calculated is an ideal value and will most likely differ based on system noise and chips offsets.

To determine the code to be expected given a specific input voltage the equation can be rearranged to give us:

Equation 6

$$n = \frac{2^{Bits-1} \cdot V_{in}}{V_{ref}} + 2^{Bits-1}$$

Example 2

For a V_{ref} of 1.3V and a resolution of 8-bits we can easily calculate the expected ADC code based on the input Voltage. The equation which can be used would be as follows:

Equation 7

$$n = \frac{128 \cdot V_{in}}{1.3} + 128$$

For an input voltage of -1V below AGND the code from the ADC can be expected to be 29.53 based on the calculation below:

Equation 8

$$n = \frac{128 \cdot (-1)}{1.3} + 128 = 29.53$$

The value calculated is an ideal value and will most likely differ based on system noise and chips offsets.

To make the integrator function as an incremental ADC, the following digital resources are utilized:

- An 8-bit counter to accumulate the number of cycles that the output is positive (one per channel).
- A 16-bit PWM to time the integrate time and gate the clock into the 8-bit counter (shared between both channels).

A single DataClock is connected to the 8-bit counters, the 16-bit PWM, and the analog column clock, which connects to the analog SC PSoC blocks. The analog column clock is actually two clocks, φ_1 and φ_2, which are generated from the DataClock. These two additional clocks are one-fourth the frequency of the DataClock. This means that the PWM and counter operate four times faster than required and therefore, need to accumulate N+2 bits worth of data (N equal number of bits of resolution).

Note It is imperative, when placing this module, that you configure it with the same clock for all blocks. Failure to do so will cause it to operate incorrectly.

The counters are implemented with an 8-bit digital block for the LSB and a software counter for the MSB. Each time the hardware counter overflows, an interrupt is generated and the upper MSB of the counter is incremented. This allows the DualADC module to be implemented with only four digital blocks instead of six.

The sample rate is the DataClock divided by the integrate time plus the time it takes to do the result calculations, CalcTime. The integrate time is the period when the input signal is being sampled by the DualADC.

Equation 9

$$SampleRate = \frac{DataClock}{2^{Bits+2} + CalcTime}$$

The time it takes to calculate the result, CalcTime, varies inversely proportional with the CPU clock. The CalcTime must be set to a value greater than what is required to calculate the result. The minimum CalcTime is equivalent to 260 CPU cycles and must be expressed in terms of the DataClock. The CalcTime may also be increased beyond the minimum to optimize the sample rate.

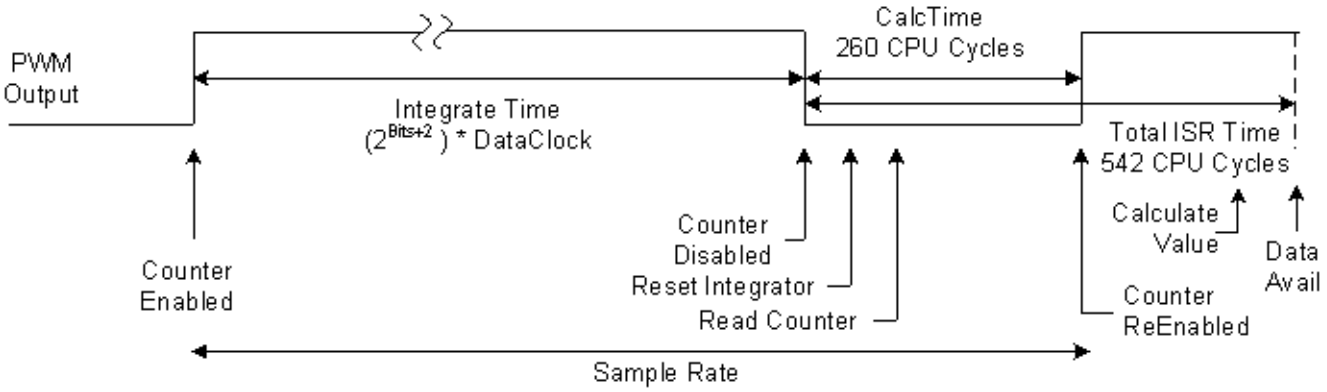
Note The total of 2^{Bits+2} plus the CalcTime must not exceed 2^{16}-1 or 65,535.

Equation 10

$$CalcTime \geq \frac{DataClock * 260}{CPUClock}$$

The 16-bit PWM is programmed to output a high signal that is 2^{Bits+2} times the DataClock. For example, if the resolution is set to 10 bits, the PWM output will remain high for 4096 (2^{10+2}) DataClock periods. The PWM output will be low for the time it takes to do the minimum result calculations and to reset the integrator. This period is controlled by the CalcTime parameter. The CalcTime can also be adjusted to help provide a more exact sample rate in combination with the DataClock. The total period of the PWM is the sum of the integrate time and the CalcTime.

Figure 3. DualADC Timing with Respect to PWM Output



When the first reading is initiated, the PWM configuration is calculated, the integrator is reset, and the counters are all reset to FFh. The initial delay will always be at least that of the calculation time. The PWM is initialized only prior to the first reading. After the compare and period registers are set once, they do not have to be re-initialized unless the resolution or calculation time is changed. When the PWM count is less than or equal to the integrate value, the output goes high, enabling the 8-bit counters to count down. The output of the PWM stays high until the counter reaches zero. At this point, the clock to the 8-bit counters is disabled and the PWM interrupt is generated.

The initial value of the 8-bit software counters is set to 2^{Bits}/64 times the most negative value. Each time the 8-bit counters overflow, the interrupt for the 8-bit counter is executed and the software counter is incremented by one.

When the input to the ADC is greater than or equal to the most positive value, the 8-bit counters will increment on every positive transition of the DataClock. If the input to the ADC is less than or equal to the most negative input value, the 8-bit counters will never decrement and therefore, never generate an interrupt. An input near analog ground under ideal conditions will allow the counter to increment half the time. Depending on the input voltage level, the amount of interrupts from the 8-bit counters will vary from 0 to (2^{Bits+2})/256. For example, if the resolution is set to 10 bits, the PWM compare value is set to 2^{10+2} (4096). This means that it is possible that the processor could be interrupted a maximum of 4096/256 or 16 times during the integrate period.

Because the DualADC control is interrupt based and the sample time takes a relatively long time for a result, it is unreasonable to expect the processor to wait while a sample is being processed. The primary communication between the ADC routine and the main program is a flag that may be polled. When the

most significant bit of DualADC_bfStatus has a non-zero value, the new data is available in DualADC_iResultn (n=1,2). APIs are available to check the data flag and retrieve data.

This data handler was designed to be poll based. If an interrupt based data handler is desired, the user may insert data handler code into the interrupt routine DualADC_CNTn_ISR, located in the assembly file *DualADCINT.asm*. The point to insert code is clearly marked.

CPU Utilization

The DualADC requires CPU time to calculate the result and to increment the software counters each time the hardware counters overflow. The CPU overhead is dependent on three variables: CPU clock, DataClock, and input voltage. At first it may seem odd that input voltage affects the CPU overhead for an ADC. Input voltages that are near or lower than –Vref require very little CPU overhead. Input voltages that are near or greater than +Vref require more CPU overhead. The equations below assume the input signal is the same for both inputs. To calculate the CPU cycles required for a given input, reference the following equations.

Equation 11

$$CPUcycles = PWM16_IRQ_CPUcycles + \left(\frac{2^{Bits}}{64} * \left(\frac{Vref + Vin}{2 * Vref}\right) * (Counter_IRQ_CPUcycles * 2)\right)$$

Equation 12

$$CPUcycles = 542 + \left(\frac{2^{Bits}}{64} * \left(\frac{Vref + Vin}{2 * Vref}\right) * (37 * 2)\right)$$

To calculate the maximum CPU cycles at 10 bits resolution, set Vin to Vref, and reference the following equation.

Equation 13

$$CPUcycles = 542 + \left(\frac{2^{10}}{64} * \left(\frac{Vref + Vref}{2 * Vref}\right) * 74\right) = 542 + (16 * 1 * 74) = 1726$$

To calculate the percent CPU utilization of the DualADC, reference the following equation.

Equation 14

$$Percent_CPU_Utilization = \frac{Sample_Rate * CPUcycles}{CPU_freqency} * 100$$

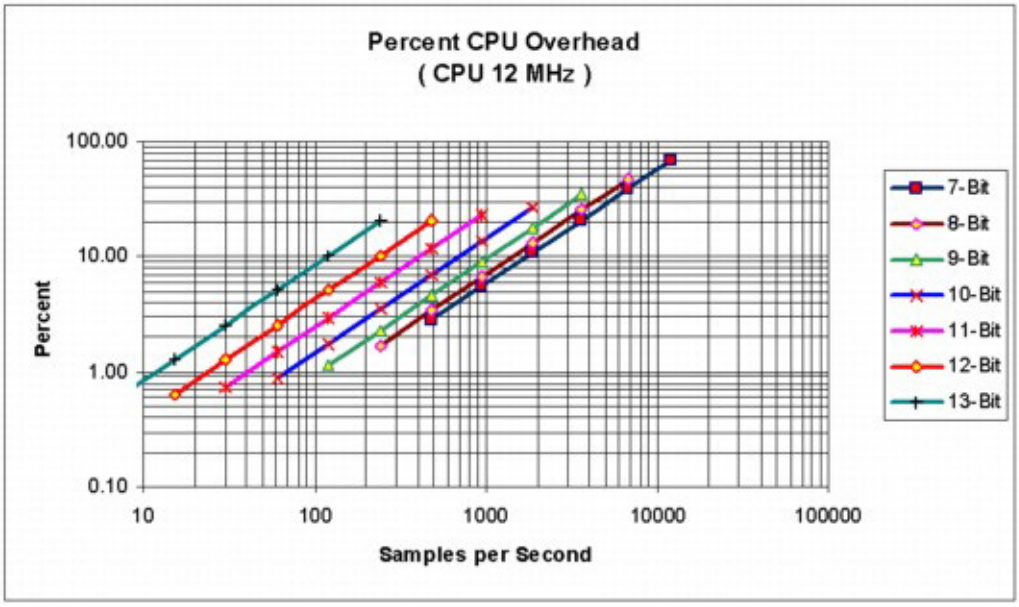
Setting the resolution to 10 bits (as in the above example), sample rate to 1000 samples/sec, and the CPU clock to 12 MHz, then (as in the equation below) utilization is calculated to be 14.4%.

Equation 15

$$Percent_CPU_Utilization = \frac{1000 * 1726}{12MHz} * 100 = 14.4\%$$

The graph below shows CPU utilization for the supported sample rates and resolutions. The default CPU speed is set to 12 MHz.

Figure 4. CPU Usage versus Sample Rate



Channel to Channel Differences

When using the DualADC, there will be differences between channels when measuring the same input voltage. This difference is due to the input offset variations in the switch cap block amplifiers and the column AGND buffers. This channel to channel offset is easily compensated for by routing the same signal into each of the ADC channels. One of the channels can be used as the reference and the difference between subsequent channels would be subtracted after each reading.

Frequency Rejection

By selecting the proper integrate time, specific noise sources may be rejected. To reject a noise source and its harmonics, select an integrate time that is equal to an integral cycle of the noise signal. If more than one signal is to be rejected, select an integrate time that is equal to an integral cycle of both signals.

For example, if noise caused by 50 Hz and 60 Hz signals is to be rejected, select a period that contains an integral number of both the 50 Hz and 60 Hz signals.

Equation 16

$$IntegrateTime = 6 * \frac{1}{60} = 5 * \frac{1}{50} = 100mSec$$

An IntegrateTime of 100 ms will reject both 50 Hz and 60 Hz, and any harmonics of these signals. Next, calculate the DataClock required to generate the proper IntegrateTime.

Equation 17

$$DataClock = \frac{2^{Bits+2}}{IntegrateTime}$$

Notice that the CalcTime is not used in this calculation, although it affects the sample rate. The IntegrateTime is the period when the DualADC is actually sampling the input voltage. The sample rate is based on the IntegrateTime and the time it takes to calculate the result.

Example

An IntegrateTime of 100 ms and an A/D resolution of 13 bits are required for a given application. For a 100 ms IntegrateTime, the data clock must be as follows.

Equation 18

$$DataClock = \frac{2^{Bits+2}}{IntegrateTime} = \frac{2^{13+2}}{100ms} = 327.7kHz$$

The CalcTime, in terms of the Data Clock, must be calculated from the DataClock and the CPU Clock. If the CPU clock is 12 MHz, the minimum calculation time would be as follows.

Equation 19

$$CalcTime \geq \frac{260 \times DataClock}{CPU_Clock}$$

This CalcTime should be rounded up to the nearest whole number, in this example it is 8. To determine the sample rate, proceed as follows.

Equation 20

$$SampleRate = \frac{DataClock}{2^{Bits+2} + CalcTime}$$

If a longer sample rate is desired, the CalcTime may be increased until the CalcTime + 2^{13+2} is less than or equal to 2^{16} – 1 (65535).

DC and AC Electrical Characteristics

Unless otherwise specified in the table below, T_A = 25°C, Vdd = 5.0V, Power HIGH, Op-Amp bias LOW, output referenced to 2.5V external Analog Ground on P2[4] with 1.25 external Vref on P2[6] and resolution set at 13 bits.

Table 1. 5.0V DualADC DC and AC Electrical Characteristics, CY8C29/27/24xxx, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Input				
Input Voltage Range	---	Vss to Vdd		Ref Mux = Vdd/2 ± Vdd/2
Input Capacitance[1]	3	---	pF	
Input Impedance	1/(C*clk)	---	Ω	
Resolution	---	7 to 13	Bits	

Parameter	Typical	Limit	Units	Conditions and Notes
Sample Rate	---	4 to 10,000	SPS	
SNR	77	---	dB	
DC Accuracy				
DNL	2	---	LSB	Column clock 2 MHz
INL	1.0	---	LSB	
Offset Error	9	---	mV	
Gain Error				
Including Reference Gain Error	3.0	--	% FSR	
Excluding Reference Gain Error[2]	0.1	--	% FSR	
Operating Current				
Low Power	370	---	µA	
Med Power	1200	---	µA	
High Power	4000	---	µA	
Data Clock	---	0.125 to 8.0	MHz	Input to digital blocks and analog column clock

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the table below, all limits guaranteed for TA = 25°C, Vdd = 3.3V, Power HIGH, Op-Amp bias LOW, output referenced to 1.64V external Analog Ground on P2[4] with 1.25 external Vref on P2[6] and resolution set at 13 bits.

Table 2. 3.3V DualADC DC and AC Electrical Characteristics, CY8C29/27/24xxx, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Input				
Input Voltage Range	---	Vss to Vdd		Ref Mux = Vdd/2 ± Vdd/2
Input Capacitance[1]	3	---	pF	
Input Impedance	1/(C*clk)	---	Ω	
Resolution	---	7 to 13	Bits	
Sample Rate	---	4 to 10,000	SPS	
SNR	77	---	dB	
DC Accuracy				

Parameter	Typical	Limit	Units	Conditions and Notes
DNL	2	---	LSB	Column clock 2 MHz
INL	1.0	---	LSB	
Offset Error	4	---	mV	
Gain Error				
Including Reference Gain Error	3.0	--	% FSR	
Excluding Reference Gain Error[2]	0.4	--	% FSR	
OperatingCurrent				
Low Power	300	---	µA	
Med Power	1000	---	µA	
High Power	3800	---	µA	
Data Clock	---	0.125 to 8.0	MHz	Input to digital blocks and analog column clock

Electrical Characteristics Notes

1. Includes I/O pin.
2. Reference Gain Error measured by comparing the external reference to $V_{RefHigh}$ and V_{RefLow} routed through the test mux and back out to a pin.
3. Typical values represent parametric norm at +25°C.
4. Input voltages above the maximum will generate a maximum positive reading. Input voltages below the minimum will generate a maximum negative reading.
5. User module only, not including I/O pin.
6. The input capacitance or impedance is only applicable when input to analog block is directly to a pin.
7. C = input capacitance, clk = data clock (Analog Column Clock).
8. Specifications are for sample rates of 100 sps and a maximum data clock of 8 MHz, unless otherwise noted. Sample rate is dependent on both data clock and resolution.
9. SNR = Ratio of power of full scale single tone divided by total noise integrated to Fsample/2.

Placement

The ADC (switch cap) blocks can be placed in any of the switched capacitor PSoC blocks. They must be able to each exclusively drive the comparator bus for the particular column in which it is placed. In other words, each of the two blocks must be in a different column and can not share a column with another switch cap block that connects to the comparator bus.

The counter blocks may be placed in any available digital block, but the PWM16 may only be placed in specific locations. In the CY8C27xxx device family possible placements for the PWB16 (LSB/MSB) are DBB00/DBB01, DBB01/DCB02, DBB10/DBB11, and DBB11/DCB12. In the CY8C29/24/22xxx device families the PWM16 can be placed in any two consecutive digital blocks.

The two counter blocks and PWM block each have an interrupt service routine. It is desirable that the counter block have a higher interrupt priority than the PWM16 block. Therefore, it is recommended that the counter blocks are placed in a lower digital block position than the PWM16 block.

Note When initially selecting the DualADC, a warning may appear that states “Resource allocation prevents placement." This warning is displayed if the original placement has two ADC blocks in the same column. Simply move each ADC block to its own column.

Parameters and Resources

ADC Input1, ADC Input2

The selection of the ADC Input is done after the analog PSoC block is placed. The eight switched cap blocks have different input selections. Each can be connected to most of its neighbors, while some can be connected directly to external input pins. Placement of the analog block must be done with some consideration of how to get an input signal to it. Some placements allow inputs to be routed directly from package pins to the input. These direct connections allow inputs that are within 40 mV of the supply rails to be measured accurately. Signals may also be routed through one of the column muxes, through one of the CT block test muxes, and onto an analog column where the DualADC can also measure signals near the power supply rails. There is one selection for each of the two ADC inputs.

ClockPhase1, ClockPhase2

The selection of the Clock Phase is used to synchronize the output of one switched capacitor analog PSoC block to the input of another. The switched cap analog PSoC blocks use a two-phase clock (φ_1, φ_2) to acquire and transfer signal. Typically, the input to the DualADC is sampled on φ_1, the Normal setting. A problem arises in that many of the user modules auto-zero their output during φ_1 and only provide a valid output during φ_2. If such a module’s output is fed to the DualADC’s input, the DualADC acquires an auto-zeroed output, instead of a valid signal. The Clock Phase selection allows the phases to be swapped so that the input signal is now acquired during φ_2, the Swapped setting. There is one selection for each of the two switch cap blocks.

Clock and Integrator Column Clock

The DataClock determines the sample rate and the signal sample window. This clock must be routed to the clock input of the counter block, the 16-bit PWM block, and the column clock for the column containing the integrator.

Note The column clocks of the integrator switch cap blocks must be manually set to the SAME clock. It is imperative that the same clock be used for all six blocks or the DualADC User Module will not function correctly.

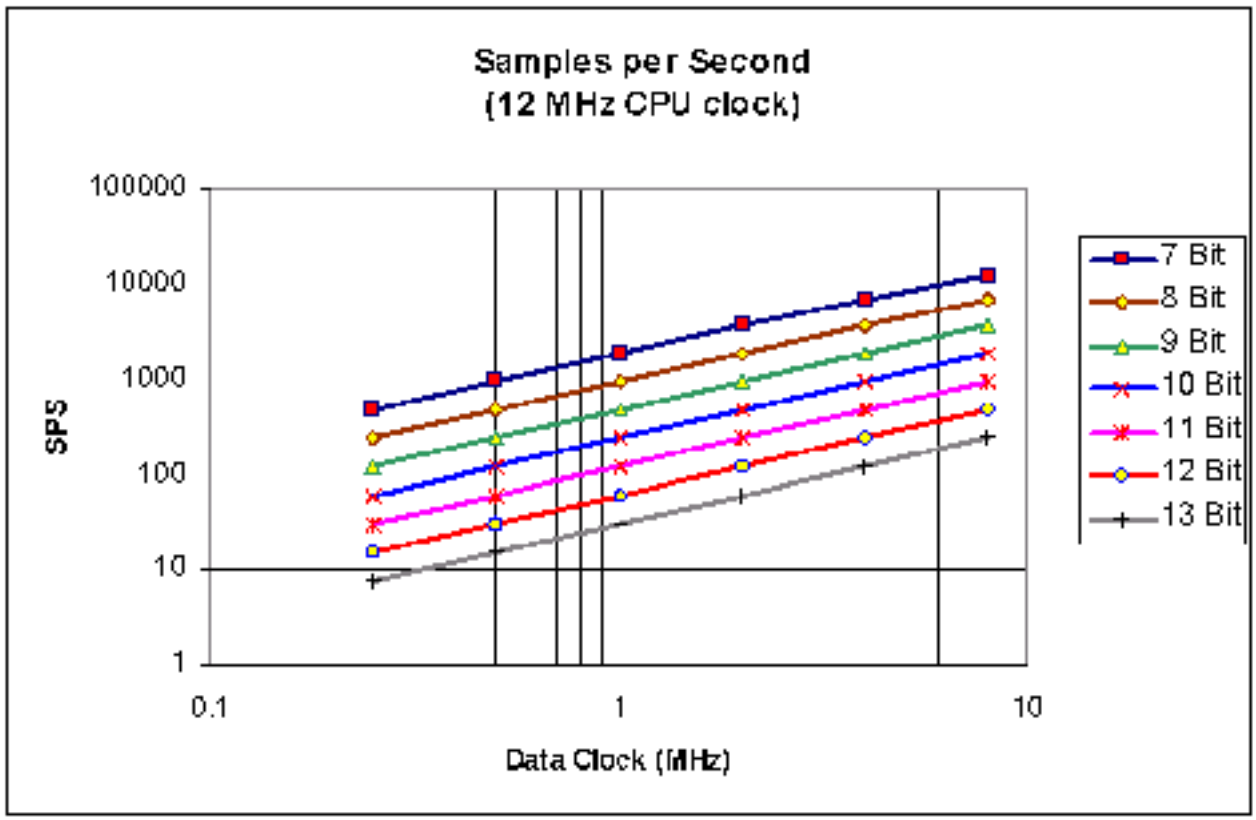
This parameter setting will only set the clock to the counter block and the PWM block. This clock may be any source with a clock rate between 125 kHz and 8 MHz.

Equation 21

$$SampleRate = \frac{DataClock}{2^{Bits+2} + CalcTime}$$

The graph below shows possible sample rates for each of the resolution options for the DualADC.

Figure 5. Samples per Second versus Data Clock



ADCResolution

The ADCResolution selection allows the resolution of the DualADC to be set in the Device Editor. Although there is an API routine to set or change the resolution, it is not required if set in the Device Editor. The resolution can also be changed at anytime with the API call, but the DualADC will be stopped and must be restarted. Valid resolution settings are 7 to 13 inclusive.

CalcTime

The CalcTime is the amount of time it takes the CPU to calculate the intermediate integration result before the next integrate cycle. The time it takes to calculate the result “CalcTime" varies inversely proportionally with the CPU clock. This value must be in terms of the data clock. Minimum CPU calculation time is 260 CPU clocks. CalcTime may also be increased to optimize the sample rate.

Note Care should be taken to make sure the CalcTime + 2^{Bits+2} does not exceed 2^{16}-1 or 65,535.

Below is an equation to determine what the CalcTime should be set to.

$$CalcTime \geq \frac{DataClock * 260}{CPUClock}$$

The table below shows the range that may be selected for the CalcTime parameter. Use the above equation to set the low end of the usable range for a given application.

Table 3. CalcTime Ranges

Resolution	Integrate Time (DataClock Counts)	CalcTime Range (DataClock Counts)
7	512	1 to 65,023
8	1,024	1 to 64,511
9	2,048	1 to 63,487
10	4,096	1 to 61,439
11	8,192	1 to 57,343
12	16,384	1 to 49,151
13	32,768	1 to 32,767

For example, if the DataClock is set to 1.5 MHz and the CPU is running at 12 MHz, the CalcTime should be set to greater than or equal to 33 (see the equation below).

Equation 22

$$CalcTime \geq \frac{DataClock * 260}{CPUClock}$$

DataFormat

This selection determines in what format the result is returned. If “Signed" is selected and “N" is the selected resolution, the result will range from -2^{N-1} to $2^{N-1}-1$. If “Unsigned" is selected, the result will be between 0 and $2^{N}-1$. Reference the following table for the result range for each data format and resolution.

Table 4. Data Format Result Ranges

Resolution Setting	Signed Data Format	Unsigned Data Format
7	-64 to 63	0 to 127
8	-128 to 127	0 to 255
9	-256 to 255	0 to 511
10	-512 to 511	0 to 1023
11	-1024 to 1023	0 to 2047
12	-2048 to 2047	0 to 4095
13	-4096 to 4095	0 to 8191

Ref Mux Global Resource

The most important global resource when dealing with analog to digital converters (ADC) is the RefMux. The setting of the RefMux determines the usable input voltage range of the ADC. The following table shows the ranges for a Vdd of 5 and 3.3 volts.

Table 5. CY8C29/27/24xxx, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52 Input Voltage Ranges for Each Ref Mux Setting

RefMux Setting	Vdd = 5 Volts	Vdd = 3.3 Volts
(Vdd/2) ± BandGap	$1.2 < V_{in} < 3.8$	$0.35 < V_{in} < 2.95$
(Vdd/2) ± (Vdd/2)	$0 < V_{in} < 5$	$0 < V_{in} < 3.3$
BandGap ± BandGap	$0 < V_{in} < 2.6$	$0 < V_{in} < 2.6$
(1.6*BandGap) ± (1.6*BandGap)	$0 < V_{in} < 4.16$	NA
(2*BandGap) ± BandGap	$1.3 < V_{in} < 3.9$	NA
(2*BandGap) ± P2[6]	$(2.6 - V_{P2[6]}) < V_{in} < (2.6 + V_{P2[6]})$	NA
P2[4] ± BandGap	$(V_{P2[4]} - 1.3) < V_{in} < (V_{P2[4]} + 1.3)$	$(V_{P2[4]} - 1.3) < V_{in} < (V_{P2[4]} + 1.3)$
P2[4] ± P2[6]	$(V_{P2[4]}-V_{P2[6]}) < V_{in} < (V_{P2[4]}+V_{P2[6]})$	$(V_{P2[4]}-V_{P2[6]}) < V_{in} < (V_{P2[4]}+V_{P2[6]})$

Interrupt Generation Control

There following parameter is only available if the **Enable interrupt generation control** check box in PSoC Designer is checked. This is available under **Project > Settings > Chip Editor**. Interrupt Generation Control is important when multiple overlays are used with interrupts shared by multiple user modules across overlays.

IntDispatchMode

The IntDispatchMode parameter is used to specify how an interrupt request is handled for interrupts shared by multiple user modules existing in the same block but in different overlays. Selecting “ActiveStatus" causes firmware to test which overlay is active before servicing the shared interrupt request. This test occurs every time the shared interrupt is requested. This adds latency and also produces a nondeterministic procedure of servicing shared interrupt requests, but does not require any RAM. Selecting “OffsetPreCalc" causes firmware to calculate the source of a shared interrupt request only when an overlay is initially loaded. This calculation decreases interrupt latency and produces a deterministic procedure for servicing shared interrupt requests, but at the expense of a byte of RAM.

Application Programming Interface

The Application Programming Interface (API) routines are provided as part of the user module to allow the designer to deal with the module at a higher level. This section specifies the interface to each function together with related constants provided by the “include" files.

Note

In this, as in all user module APIs, the values of the A and X register may be altered by calling an API function. It is the responsibility of the calling function to preserve the values of A and X before the call if those values are required after the call. This “registers are volatile" policy was selected for efficiency reasons and has been in force since version 1.0 of PSoC Designer. The C compiler automatically takes care of this requirement. Assembly language programmers must ensure their code observes the policy, too. Though some user module API function may leave A and X unchanged, there is no guarantee they will do so in the future.

For Large Memory Model devices, it is also the caller's responsibility to preserve any value in the CUR_PP, IDX_PP, MVR_PP, and MVW_PP registers. Even though some of these registers may not be modified now, there is no guarantee that will remain the case in future releases.

API routines can initialize, configure, start sampling, stop, and read the resultant data from the ADC.

DUALADC_Start

Description:

Performs all required initialization for this user module and sets the power level for the switched capacitor PSoC block.

C Prototype:

```
void  DualADC_Start (BYTE bPowerSetting)
```

Assembly:

```
mov   A, DualADC_HIGHPOWER
lcall  DualADC_Start
```

Parameters:

PowerSetting: One byte that specifies the power level. Following reset and configuration, the analog PSoC block assigned to DualADC is powered down. Symbolic names provided in C and assembly, and their associated values, are given in the following table.

Symbolic Name	Value
DualADC_OFF	0
DualADC_LOWPOWER	1
DualADC_MEDPOWER	2
DualADC_HIGHPOWER	3

Power level has an effect on analog performance. The correct power setting is sensitive to the sample rate of the data clock and has to be determined for each application. It is recommended that you start your development with full power selected. Testing can later be done to determine how low you can set the power setting.

Return Value:

None

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

DUALADC_Stop

Description:

Sets the power level on the switched capacitor integrator block to 0ff. This is done when the DualADC in not being used and the user wants to save power. This routine powers down the analog switch

capacitor block and disables the digital blocks. To achieve the lowest power level, the clock should be removed from the digital blocks as well.

C Prototype:

```
void  DualADC_Stop()
```

Assembly:

```
lcall  DualADC_Stop
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions.

DUALADC_SetPower

Description:

Sets the power level for the switched capacitor PSoC block.

C Prototype:

```
void  DualADC_SetPower (BYTE bPowerSetting)
```

Assembly:

```
mov   A, [bPowerSetting]
lcall  DualADC_SetPower
```

Parameters:

PowerSetting: Same as the PowerSetting parameter used for the Start API routine. Allows the user to change the power level while operating the ADC.

Return Value:

None

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

DUALADC_SetResolution

Description:

Sets the resolution of the A/D converter.

C Prototype:

```
void  DualADC_SetResolution (BYTE bResolution)
```

Assembly:

```
mov   A, [bResolution]
lcall  DualADC_SetResolution
```

Parameters:

Resolution: The resolution of the A/D converter may be set either in the Device Editor or in the user firmware. If not set in the firmware, the ADC will use the resolution set in the Device Editor by default. Values for resolution may be set between 7 and 13 bits.

Return Value:

None

Side Effects:

Stops the A/D converter. The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

DUALADC_GetSamples

Description:

Initializes and starts the ADC algorithm to collect the specified number of samples. Remember to enable global interrupts by calling the M8C_EnableGInt macro call defined in *M8C.inc* or *M8C.h*.

C Prototype:

```
void  DualADC_GetSamples (BYTE bNumSamples)
```

Assembly:

```
mov   A, [bNumSamples]
lcall  DualADC_GetSamples
```

Parameters:

bNumSamples: An 8-bit value that sets the number of samples to be retrieved. A value of ‘0‘ causes the ADC to run continuously.

Return Value:

None

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

DUALADC_StopAD

Description:

Immediately halts the ADC.

C Prototype:

```
void  DualADC_StopAD()
```

Assembly:

```
lcall  DualADC_StopAD
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions.

DUALADC_fIsDataAvailable

Description:

Returns non-zero when a data conversion is complete and data is available for reading.

C Prototype:

```
BYTE  DualADC_fIsDataAvailable()
```

Assembly:

```
lcall  DualADC_fIsDataAvailable
```

Parameters:

None

Return Value:

Returns non-zero when data is available.

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

DUALADC_iGetData1

Description:

Returns last converted data for ADC Input1. DUALADC_fIsDataAvailable() should be called prior to getting the data, to ensure that the data is valid. Data must be retrieved before the next conversion cycle is completed or else the data will be overwritten. There is a possibility that the returned data will be corrupted if the call to this function is done exactly at the end of an integration period. It is therefore highly recommended that the data retrieval be done at a higher frequency than the sampling rate, or if that cannot be guaranteed that interrupts be turned off before calling this function.

C Prototype:

```
INT   DualADC_iGetData1()
```

Assembly:

```
lcall  DualADC_iGetData1
```

Parameters:

None

Return Value:

Converted integer value is returned. In assembler, the MSB is returned in the X register and the LSB in the Accumulator.

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

DUALADC_iGetData2

Description:

Returns last converted data for ADC Input2. DUALADC_fIsDataAvailable() should be called prior to getting the data, to ensure that the data is valid. Data must be retrieved before the next conversion cycle is completed or else the data will be overwritten. There is a possibility that the returned data will be corrupted if the call to this function is done exactly at the end of an integration period. It is therefore highly recommended that the data retrieval be done at a higher frequency than the sampling rate, or if that cannot be guaranteed that interrupts be turned off before calling this function.

C Prototype:

```
INT   DualADC_iGetData2()
```

Assembly:

```
lcall  DualADC_iGetData2
```

Parameters:

None

Return Value:

Converted integer value is returned. In assembler, the MSB is returned in the X register and the LSB in the Accumulator.

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

DUALADC_ClearFlag

Description:

Clears Data Available flag.

C Prototype:

```
void  DualADC_ClearFlag()
```

Assembly:

```
lcall  DualADC_ClearFlag
```

Parameters

None

Return Value:

None

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

DUALADC_iGetData1ClearFlag

Description:

Returns last converted data for ADC Input1 and clears the Data Available flag. DUALADC_fIsDataAvailable() should be called prior to getting the data, to ensure that the data is valid. Data must be retrieved before the next conversion cycle is completed or else the data will be overwritten. There is a possibility that the returned data will be corrupted if the call to this function is done exactly at the end of an integration period. It is therefore highly recommended that the data retrieval be done at a higher frequency than the sampling rate, or if that cannot be guaranteed that interrupts be turned off before calling this function.

C Prototype:

```
INT   DualADC_iGetData1ClearFlag()
```

Assembly:

lcall DualADC_iGetData1ClearFlag

Parameters:

None

Return Value:

Converted integer value is returned. In assembler, the MSB is returned in the X register and the LSB in the accumulator.

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

DUALADC_iGetData2ClearFlag

Description:

Returns last converted data for ADC Input2 and clears the Data Available flag. DUALADC_fIsDataAvailable() should be called prior to getting the data, to ensure that the data is valid. Data must be retrieved before the next conversion cycle is completed or else the data will be overwritten. There is a possibility that the returned data will be corrupted if the call to this function is done exactly at the end of an integration period. It is therefore highly recommended that the data

retrieval be done at a higher frequency than the sampling rate, or if that cannot be guaranteed that interrupts be turned off before calling this function.

C Prototype:

```
INT   DualADC_iGetData2ClearFlag()
```

Assembly:

```
lcall  DualADC_iGetData2ClearFlag
```

Parameters:

None

Return Value:

Converted integer value is returned. In assembler, the MSB is returned in the X register and the LSB in the accumulator.

Side Effects:

The A and X registers may be modified by this or future implementations of this function. The same is true for all RAM page pointer registers in the Large Memory Model (CY8C29xxx). When necessary, it is the calling function's responsibility to preserve the values across calls to fastcall16 functions. Currently, only the CUR_PP page pointer register is modified.

Note The functions DUALADC_ClearFlag, DUALADC_iGetData1ClearFlag, and DUALADC_iGetData2ClearFlag all clear the same flag. They are included to provide the greatest amount of flexibility when clearing the conversion complete flag. When the A/D conversion is complete, the user may choose to ignore the result of one or both channels and simply clear the flag without retrieving the data.

Sample Firmware Source Code

A sample project written in assembly code follows.

```
;;; Sample ASM Code for the DualADC
;;;
;;; Continuously sample using the DualADC and store the values in RAM.
;;;

include "m8c.inc"       ; part specific constants and macros
include "PSoCAPI.inc"   ; PSoC API definitions for all User Modules

;; Create storage for readings
area bss(RAM)
iResult1:       BLK   2  ; ADC1 result storage
iResult2:       BLK   2  ; ADC2 result storage
export iResult1          ; Export results in case they are
export iResult2          ; used elsewhere.

area text(ROM,REL)
export _main

_main:

    M8C_EnableGInt                ; Enable interrupts
    mov   A, 10                   ; Set resolution to 10 Bits
```

```
    call  DUALADC_SetResolution

    mov   A, DUALADC_HIGHPOWER     ; Set Power and Enable A/D
    call  DUALADC_Start

    mov   A, 00h                   ; Start A/D in continuous sampling mode
    call  DUALADC_GetSamples


;A/D conversion loop
loop1:

wait:                              ; Poll until data is complete
    call  DUALADC_fIsDataAvailable
    jz    wait
  call  DUALADC_ClearFlag        ; Reset flag

    call  DUALADC_iGetData1        ; Get ADC1 Data (X=MSB A=LSB)
    mov   [iResult1+1],A           ; Store LSB
    mov   [iResult1+0],X           ; Store MSB

    call  DUALADC_iGetData2        ; Get ADC2 Data (X=MSB A=LSB)
    mov   [iResult2+1],A           ; Store LSB
    mov   [iResult2+0],X           ; Store MSB
    jmp   loop1
```

A sample project written in C follows.

```
//-----------------------------------------------------------------------
//  Sample C Code for the DualADC
//  Continuously Sample and call a user function with the data.
//  This example differs from the ASM example, in that the DataAvailable
//  flag is automatically cleared when the second value is read, instead of
//  clearing the flag prior to reading the data.
//
//-----------------------------------------------------------------------
#include <m8c.h>        // part specific constants and macros
#include "PSoCAPI.h"    // PSoC API definitions for all User Modules

extern void User_Function(int iResult1, int iResult2);

void main(void)

{

   int iResult1, iResult2;

   M8C_EnableGInt;                      // Enable global interrupts
   DUALADC_Start(DUALADC_HIGHPOWER);    // Turn on Analog section
   DUALADC_SetResolution(10);           // Set resolution to 10 Bits
   DUALADC_GetSamples(0);               // Start ADC to read continuously

   for(;;)

   {
```

```
      while(DUALADC_fIsDataAvailable() == 0);  // Wait for data to be ready
      iResult1 = DUALADC_iGetData1();          // Get Data from ADC Input1
      iResult2 = DUALADC_iGetData2ClearFlag(); // Get Data from ADC Input2
                                               // and clear data ready flag

    User_Function(iResult1,iResult2);        // User function to use data
   }

}
```

Configuration Registers

These registers are configured by the initialization and API library. The user does not have to change or read these registers directly. This section is supplied as a reference only.

The ADC is a switched capacitor PSoC block. It is configured to make an analog modulator. To build the modulator, the block is configured to be an integrator with reference feedback that converts the input value into a digital pulse stream. The input multiplexer determines what signal is digitized.

Table 6. Block ADC1: Register CR0

Bit	7	6	5	4	3	2	1	0
Value	1	0	0	1	0	0	0	0

Table 7. Block ADC1: Register CR1

Bit	7	6	5	4	3	2	1	0
Value	ACMux, AMux			0	0	0	0	0

ACMux is used when block is placed in a type ‘A’ block. AMux is used when block is placed in a type ‘B’ block. Both field values depend on how the user connects the input.

Table 8. Block ADC1: Register CR2

Bit	7	6	5	4	3	2	1	0
Value	0	1	1	0	0	0	0	0

Table 9. Block ADC1: Register CR3

Bit	7	6	5	4	3	2	1	0
Value	1	1	1	FSW0	0	0	0	0

FSW0 is used by the PWM interrupt handler and various APIs. A ‘0’ value causes the ADC to be a disabled integrator. A ‘1’ value causes the ADC to be an enabled integrator.

Table 10. Block ADC2: Register CR0

Bit	7	6	5	4	3	2	1	0
Value	1	0	0	1	0	0	0	0

Table 11. Block ADC2: Register CR1

Bit	7	6	5	4	3	2	1	0
Value	ACMux, AMux			0	0	0	0	0

ACMux is used when the block is placed in a type ‘A’ block. AMux is used when the block is placed in a type ‘B’ block. Both field values depend on how the user connects the input.

Table 12. Block ADC2: Register CR2

Bit	7	6	5	4	3	2	1	0
Value	0	1	1	0	0	0	0	0

Table 13. Block ADC2: Register CR3

Bit	7	6	5	4	3	2	1	0
Value	1	1	1	FSW0	0	0	0	0

FSW0 is used by the TMR interrupt handler and various APIs. A ‘0’ value causes the ADC to be a disabled integrator. A ‘1’ value causes the ADC to be an enabled integrator.

The PWM16 is a digital PsoC block that is used to control the integration time of the ADC. The compare value is set to 2^{Bits+2} and the period is set to the CalcTime plus the compare value.

Table 14. Block PWM16_MSB: Register Function

Bit	7	6	5	4	3	2	1	0
Value	0	0	1	Compare Type	Interrupt Type	0	0	1

Compare Type is a flag that indicates whether the capture comparison is “equal to or less than" or “less than." Interrupt Type is a flag that indicates whether to trigger the interrupt on the capture event or the terminal condition. Both parameters are set in the Device Editor.

Table 15. Block PWM16_LSB: Register Function

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	Compare Type	0	0	0	1

Compare Type is a flag that indicates whether the compare function is set to “equal to or less than" or “less than." This parameter is set in the Device Editor.

Table 16. Block PWM16_MSB: Register Input

Bit	7	6	5	4	3	2	1	0
Value	0	0	1	1	Clock			

Clock selects the input clock from one of 16 sources. This parameter is set in the Device Editor.

Table 17. Block PWM16_LSB: Register Input

Bit	7	6	5	4	3	2	1	0
Value	Enable				Clock			

Enable selects data input from one of 16 sources and Clock selects clock input from one of 16 sources. Both parameters are set in the Device Editor.

Table 18. Block PWM16_MSB: Register Output

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	Output Enable	Output Sel	

Output Enable is the flag that indicates the output is enabled. Output Sel is the flag that indicates where the output of the PWM16 will be routed. Both parameters are set in the Device Editor.

Table 19. Block PWM16_LSB: Register Output

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0

Table 20. Block PWM16_MSB: Count Register DR0

Bit	7	6	5	4	3	2	1	0
Value	Count(MSB)							

Count is the PWM16 MSB down PWM. It can be read using the PWM16 API.

Table 21. Block PWM16_LSB: Count Register DR0

Bit	7	6	5	4	3	2	1	0
Value	Count(LSB)							

Count is the PWM16 LSB down PWM. It can be read using the PWM16 API.

Table 22. Block PWM16_MSB: Period Register DR1

Bit	7	6	5	4	3	2	1	0
Value	Period(MSB)							

Period holds the MSB of the period value that is loaded into the Counter register, upon enable or terminal count condition. It can be set by the Device Editor and the PWM16 API.

Table 23. Block PWM16_LSB: Period Register DR1

Bit	7	6	5	4	3	2	1	0
Value	Period(LSB)							

Period holds the LSB of the period value that is loaded into the Counter register, upon enable or terminal count condition. It can be set by the Device Editor and the PWM16 API.

Table 24. Block PWM16_MSB: Pulse Width Register DR2

Bit	7	6	5	4	3	2	1	0
Value	Pulse Width(MSB)							

PulseWidth holds the MSB of the pulse width value used to generate the compare event. It can be set by the Device Editor and the PWM16 API.

Table 25. Block PWM16_LSB: Pulse Width Register DR2

Bit	7	6	5	4	3	2	1	0
Value	Pulse Width(LSB)							

PulseWidth holds the LSB of the pulse width value used to generate the compare event. It can be set by the Device Editor and the PWM16 API.

Table 26. Block PWM16_MSB: Control Register CR0

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	Start/ Stop(0)

Start/Stop is controlled by the LSB control register value, set to zero.

Table 27. Block PWM16_LSB: Control Register CR0

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	Start/ Stop

Start/Stop indicates that the PWM16 is enabled when set. It is modified by using the PWM16 API

The CNT is a digital PSoC block configured as a counter. When the value in DR0 counts down to terminal count, an interrupt is called to decrement a higher value software counter and CNT reloads from DR1. The data is outputted through DR2.

Table 28. Block CNT1: Register Function

Bit	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	1

Table 29. Block CNT1: Register Input

Bit	7	6	5	4	3	2	1	0
Value	Data				Clock			

Data selects the column comparator where the ADC block has been placed. Clock selects the input clock from one of 16 sources and is set in the Device Editor.

Table 30. Block CNT1: Register Output

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0

Table 31. Block CNT1: Register DR0

Bit	7	6	5	4	3	2	1	0
Value	Count Value							

Table 32. Block CNT1: Register DR1

Bit	7	6	5	4	3	2	1	0
Value	1	1	1	1	1	1	1	1

Table 33. Block CNT1: Register DR2

Bit	7	6	5	4	3	2	1	0
Value	Data Out							

Data Out is the register used by the API to get the counter value.

Table 34. Block CNT1: Register CR0

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	Enable

Enable enables the CNT. It is modified and controlled by the DualADC API

Table 35. Block CNT2: Register Function

Bit	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	1

Table 36. Block CNT2: Register Input

Bit	7	6	5	4	3	2	1	0
Value	Data				Clock			

Data selects the column comparator where the ADC block has been placed. Clock selects the input clock from one of 16 sources and is set in the Device Editor.

Table 37. Block CNT2: Register Output

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0

Table 38. Block CNT2: Register DR0

Bit	7	6	5	4	3	2	1	0
Value	Count Value							

Table 39. Block CNT2: Register DR1

Bit	7	6	5	4	3	2	1	0
Value	1	1	1	1	1	1	1	1

Table 40. Block CNT2: Register DR2

Bit	7	6	5	4	3	2	1	0
Value	Data Out							

Data Out is the register used by the API to get the counter value.

Table 41. Block CNT2: Register CR0

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	Enable

Enable enables the CNT. It is modified and controlled by the DualADC API.

Table 42. Register: INT_MSK1

Bit	7	6	5	4	3	2	1	0
Value								

The mask bits corresponding to the TMR block and CNT block are set here to enable their respective interrupts. The actual mask values are determined by the placement position of each block.

Version History

Version	Originator	Description
2.2	DHA	Added DRC to check if: 1. The source clock is different in digital and analog resources. 2. The ADC Clock is higher than CPU Clock.
2.30	DHA	Restored VC3 as the source for the data clock.
2.30.b	MYKZ	Added design rules check for the situation when ADC clock is faster than 8MHz.

Note PSoC Designer 5.1 introduces a Version History in all user module datasheets. This section documents high level descriptions of the differences between the current and previous user module versions.

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