Digital Buffers Datasheet DigBuf V 1.3

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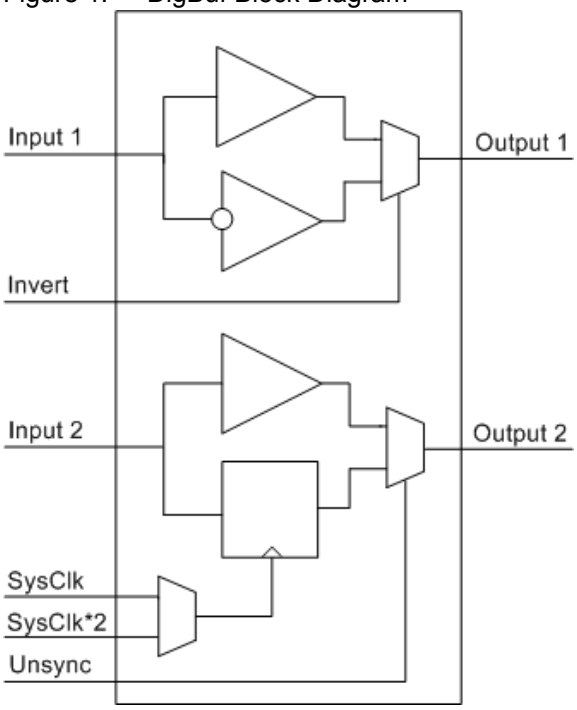
Resources	PSoC® Blocks			API Memory (Bytes)		Pins (per External I/O)
	Digital	Analog CT	Analog SC	Flash	RAM	
CY8C29/27/24/22/21xxx, CY8C23x33, CY8CLED02/04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST110, CY8CTMG110, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8CTMA140, CY8C21x45, CY8C22x45, CY8CTMA30xx, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28xxx						
	0	0	0	25	0	1 to 4
CYWUSB6953	0	0	0	25	0	1 to 4

Features and Overview

- Two digital buffers
- Input1 can be inverted
- Can be used to generate an interrupt on the rising edge of Output1

The DigBuffer User Module is a simple two input two output digital buffer. The output is equivalent to the input signal.

Figure 1. DigBuf Block Diagram



Functional Description

DigBuf is a set of two digital buffers. It can be mapped onto any digital PSoC block. The API provides functions to enable or disable the Output1 interrupt capability.

DC and AC Electrical Characteristics

Table 1. DigBuf DC and AC Electrical Characteristics

Parameter	Conditions and Notes	Typical	Limit	Units
Input F_{max} from Global Bus			12	MHz
Input F_{max} from internal connections			48	MHz
Input to Output Transition		< 25		ns
Output F_{max} to Global Bus			12	MHz
Output F_{max} to internal connections			48	MHz

Timing

The DigBuf User Module is limited to 12 MHz (nominal) transition speeds when the input or output is connected to a global bus. To achieve higher transition speeds, place the DigBuf User Module next to a user module providing the high speed output, that block can then be selected as the source of the Input2 signal.

Placement

The DigBuf may be placed in any digital PSoC block.

Parameters and Resources

Determines whether the block defaults to an enabled or disabled state at the time the user module loads. If this parameter is set to Enable, then there is no need to call the Start function to enable the user module. If it set to Disable, then the buffer functionality is not turned on until the Start function is called.

Input1

The Input1/Output1 digital buffer is an asynchronous buffer.

The number of sources for Input1 varies depending on the digital block the UM is placed. These sources include the Analog Comparator buses and the row input and output buses.

Input2

The number of sources for Input2 varies depending on the digital block the UM is placed. These sources include the 48 MHz oscillator output, lower frequencies (VC1, VC2, and VC3) divided down from the 24-MHz system clock, and other PSoC blocks and external inputs routed through global inputs and outputs.

Input2 ClockSync

If this parameter is set to "Unsynchronized", then the Input2/Output2 digital buffer operates as an asynchronous buffer. If this parameter is set to "Sync to SysClk" or "Sync to SysClk*2" then the Input2/Output2 circuit functions as a flip-flop that is clocked using the respective clock chosen for synchronization.

If the Output2 signal of the DigBuf User Modules is to be used as an input signal or a clock for other blocks within the PSoC it is recommended that Input2 is synchronized with one of the internal system clocks. The choice of clocks depends on where the output is routed internally, which is further explained in the following table.

ClockSync Value	Use
Sync to SysClk	Use this setting when routing the output to blocks using the 24 MHz (SysClk) or a SysClk derived clock source that is divided by two or more. Examples include VC1, VC2, VC3 (when VC3 is driven by SysClk), 32 KHz.
Sync to SysClk*2	Use this setting when routing the output to blocks using the 48 MHz (SysClk*2) or a SysClk*2 based clock.
Unsynchronized	Use when unsynchronized inputs are desired. In general this use is advisable only when planning to feed the output directly to a pin or for interrupt generation.

Output1

The output may be routed to one of four global output signals.

Output2

The output may be routed to one of four global output signals.

InvertInput1

Inverts the value of Input1.

Interrupt Generation Control

There are two additional parameters that become available when the **Enable interrupt generation control** check box in PSoC Designer is checked. This is available under **Project > Settings > Chip Editor**. Interrupt Generation Control is important when multiple overlays are used with interrupts shared by multiple user modules across overlays:

- Interrupt API
- IntDispatchMode

InterruptAPI

The InterruptAPI parameter allows conditional generation of a user module’s interrupt handler and interrupt vector table entry. Select “Enable” to generate the interrupt handler and interrupt vector table entry. Select “Disable” to bypass the generation of the interrupt handler and interrupt vector table entry. Properly selecting whether an Interrupt API is to be generated is recommended particularly with projects that have multiple overlays where a single block resource is used by the different overlays. By selecting only Interrupt API generation when it is necessary the need to generate an interrupt dispatch code might be eliminated, thereby reducing overhead.

IntDispatchMode

The IntDispatchMode parameter is used to specify how an interrupt request is handled for interrupts shared by multiple user modules existing in the same block but in different overlays. Selecting “ActiveStatus” causes firmware to test which overlay is active before servicing the shared interrupt request. This test occurs every time the shared interrupt is requested. This adds latency and also produces a nondeterministic procedure of servicing shared interrupt requests, but does not require any RAM. Selecting “OffsetPreCalc” causes firmware to calculate the source of a shared interrupt request only when an overlay is initially loaded. This calculation decreases interrupt latency and produces a deterministic procedure for servicing shared interrupt requests, but at the expense of a byte of RAM.

Application Programming Interface

The Application Programming Interface (API) routines are provided as part of the user module to allow the designer to deal with the module at a higher level. This section specifies the interface to each function together with related constants provided by the “include” files.

Note

In this, as in all user module APIs, the values of the A and X register may be altered by calling an API function. It is the responsibility of the calling function to preserve the values of A and X prior to the call if those values are required after the call. This “registers are volatile” policy was selected for efficiency reasons and has been in force since version 1.0 of PSoC Designer. The C compiler automatically takes care of this requirement. Assembly language programmers must ensure their code observes the policy, too. Though some user module API functions may leave A and X unchanged, there is no guarantee they will do so in the future.

For Large Memory Model devices, it is also the caller's responsibility to preserve any value in the CUR_PP, IDX_PP, MVR_PP, and MVW_PP registers. Even though some of these registers may not be modified now, there is no guarantee that will remain the case in future releases.

Following are the API programming routines provided for DigBuf.

DigBuf_Start

Description:

Starts the digital buffers within the block.

C Prototype:

```
void DigBuf_Start(void);
```

Assembly:

```
lcall DigBuf_Start
```

Parameters:

None

Return Value:

None

Side Effects:

You can alter the A and X registers by this function.

DigBuf_Stop

Description:

Stops the Digital Buffers within the block. The outputs are driven low.

C Prototype:

```
void DigBuf_Stop(void);
```

Assembly:

```
lcall DigBuf_Stop
```

Parameters:

None

Return Value:

None

Side Effects:

You can alter the A and X registers by this function.

DigBuf_EnableInt

Description:

Enables interrupt mode operation.

C Prototype:

```
void DigBuf_EnableInt(void);
```

Assembly:

```
lcall DigBuf_EnableInt
```

Parameters:

None

Return Value:

None

Side Effects:

You can alter the A and X registers by this function.

DigBuf_DisableInt

Description:

Disables interrupt mode operation.

C Prototype:

```
void DigBuf_DisableInt(void);
```

Assembly:

```
lcall DigBuf_DisableInt
```

Parameters:

None

Return Value:

None

Side Effects:

You can alter the A and X registers may be altered by this function.

Sample Firmware Source Code

The following is assembly language source that illustrates the use of APIs.

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;  Start the Digital Buffers User Module.
;
;  Parameters: None
;  Returns:    None
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

include    "M8C.inc"               ; include the global include file

include    "DigBuf.inc"            ; include the DigBuf API include file

StartBuffers:
    M8C_EnableGInt
    call  DigBuf_EnableInt
    call  DigBuf_Start
    ret
```

The same code in C is as follows.

```
/*****************************************************************************
*  Start the Digital Buffers User Module.
*
*  Parameters: None
*  Returns:    None
*****************************************************************************/

#include    "M8C.h"
#include    "DigBuf.h"

void StartBuffers(void)
{
   M8C_EnableGInt;
   DigBuf_EnableInt();
   DigBuf_Start();
}
```

Configuration Registers

The digital PSoC block registers used to configure the DigBuf User Module are described in the following table. Only the parameterized symbols are explained.

Table 2. Block DigBuf Register Function

Bit	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	1	0

Table 3. Block DigBuf: Register Input

Bit	7	6	5	4	3	2	1	0
Value	Input1 Select				Input2 Select			

Input1 Select sets the input from various sources and is set in the Device Editor. Input2 Select sets the input from various sources and is set in the device Editor

Table 4. Block DigBuf: Register Output

Bit	7	6	5	4	3	2	1	0
Value	Input2 ClockSync Select		Output2 Enable	Output2 Select		Output1 Enable	Output1 Select	

Outputx Enable is a flag that indicates the output is enabled. Outputx Select is a flag that indicates where the output of the DigBuf will be routed. Both parameters are set in the Device Editor.

Table 5. Block DigBuf: LFSR Register DR0

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0

Table 6. Block DigBuf: Polynomial Register DR1

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0

Table 7. Block DigBuf: Seed/Residual Register DR2

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0

Table 8. Block DigBuf: Control Register CR0

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	1	Start

When the Start bit is enabled then the DigBuf functionality is enabled when it is cleared then the outputs of the block are driven low.

Version History

Version	Originator	Description
1.3	DHA	Added Version History
1.3.b	DHA	1. Updated the user module block diagram. 2. Updated the descriptions of "Input1" and "Input2 ClockSync" user modules parameters.

Note PSoC Designer 5.1 introduces a Version History in all user module datasheets. This section documents high level descriptions of the differences between the current and previous user module versions.

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