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Cypress Semiconductor
Product Qualification Report

QTP# 98516 VERSION*B
December, 2014

Low Voltage Synchronous/Asynchronous Dual Port SRAM

R42D Technology, Fab 4 Qualification

CY7C09079V/CY7C09179V	32K x 8/9 Synchronous DP SRAM
CY7C09089V/CY7C09189V	64K x 8/9 Synchronous DP SRAM
CY7C09099V/CY7C09199V	128K x 8/9 Synchronous DP SRAM
CY7C09269V/CY7C09369V	16K x16/18 Synchronous DP SRAM
CY7C09279V/CY7C09379V	32K x 16/18 Synchronous DP SRAM
CY7C09289V/CY7C09389V	64K x 16/18 Synchronous DP SRAM
CY7C008V/CY7C018V	64K x 8/9 Asynchronous DP SRAM
CY7C009V/CY7C019V	128K x 8/9 Asynchronous DP SRAM
CY7C027V/CY7C037V/AV	32K x 16/18 Asynchronous DP SRAM
CY7C028V/CY7C038V	64K x 16/18 Asynchronous DP SRAM

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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PACKAGE/PRODUCT QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date
98368	NEW PRODUCT, 7C038A 5V R42HD IN FAB4	Sep 98
98516	New Product 7C038B, 3.3V, R42D Hot Aluminum In Fab4	May 99

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: To qualify 7C038B, 3.3 Dual Port SRAM and its options in Fab 4, R42D with Hot Al.			
Marketing Part #:	CY7C038V /CY7C037AV		
Package:	100 pins TQFP		
Device Description:	64K x 18 Synchronous Dual Port Static RAM, R42D Technology		
Cypress Division:	Cypress Semiconductor Corporation – Memory Product Division (MPD)		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. B	
Die Size (stepping):	225 mils x 365 mils	What ID markings on Die:	7C038VA

TECHNOLOGY/FAB PROCESS DESCRIPTION – R42D w/ Hot Al			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6000Å Al -5%Cu/1200Å TiW Metal 2: 500Å TiW/8000Å Al -5%Cu/300Å TiW
Passivation Type and Materials:		7000Å SiO_2 + 6000Å Si_3N_4	
Free Phosphorus contents in top glass layer(%):		0%	
Die Coating(s), if used:		N/A	
Generic Process Technology/Design Rule (μ-drawn):		CMOS, Double Metal /0.35 μm	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 70Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor – Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R42D w/ Hot Al	

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	100-pin TQFP		
Mold Compound Name/Manufacturer:	Hitachi CEL 9200		
Lead Frame material:	Copper Alloy 194		
Lead Finish, composition:	Solder Plated, 90%Sn, 10%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Epoxy	Die Attach Material:	Ablestik 8361H
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.0 mil
JESD22-A112 Moisture Sensitivity Level:	Level 3 (previously qualified)		
Name/Location of Assembly (prime) facility:	ASE, Taiwan (TAIWAN-G)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C JESD22-A-108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C JESD22-A-108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110 130°C, 85%RH, 33.3PSIA, 5.5V Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30C/60%RH)	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7 2200V	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	JESD22-C101 750V	P
Latchup Sensitivity	In accordance with JEDEC 17 9V ±200Ma	P
Alpha Particle Sensitivity	2.6V & 4.0V, Room Temperature; 465,116 alpha/cm2-hr	0 FIT

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	1510	0	N/A	N/A	0 PPM
High Temperature Operating Life[2,3] Long Term Failure Rate	142,080 DHRs	0	0.7	170	38 FIT

[1] A production burn-in of 48 Hrs at 150°C, 4.3V is required for the product
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
K = Boltzmann's constant = 8.62×10^{-5} Ev/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

QTP#: 98516

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V)							
CY7C038V-AC	TAIWN-G	4902498	619903202	48	505	0	
CY7C028V-AC	TAIWN-G	4903566	619904225	48	420	0	
CY7C028V-AC	TAIWN-G	4903566	619904225	48	345	0	
CY7C028V-AC	TAIWN-G	4903566	619904225	48	240	0	
STRESS: ESD-CHARGE DEVICE MODEL (750V)							
CY7C028V-AC	TAIWN-G	4903566	619904225	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2200V)							
CY7C028V-AC	TAIWN-G	4903566	619904225	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V)							
CY7C038V-AC	TAIWN-G	4902498	619903202	80	120	0	
CY7C038V-AC	TAIWN-G	4902498	619903202	500	120	0	
CY7C028V-AC	TAIWN-G	4903566	619904225	80	396	0	
CY7C028V-AC	TAIWN-G	4903566	619904225	500	120	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 5.5V, 33.3 PSIA), PRECOND. 192 HRS 30C/60%RH							
***CY7C09389V-AC	CSPI-R	4902498	619903202	128	50	0	(See note)

Note: *** Reliability Monitor data, #93180-92. One reject due to electrical overstress, the reject is not attributable to HAST testing.

DEVICE RELATED RELIABILITY TEST DATA

QTP#: 98368[1]

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
CY7C09389-AC	TAIWN-G	4818845	619806813	48	289	0	
CY7C09389-AC	TAIWN-G	4821104	619808005	48	1234	0	
STRESS: ESD-CHARGE DEVICE MODEL (1,000V)							
CY7C09389-AC	TAIWN-G	4818845	619806221	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (1,100V)							
CY7C09389-AC	TAIWN-G	4818845	619806221	COMP	3	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C09389-AC	TAIWN-G	4818845	619806221	168	44	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH (MSL 3)							
CY7C09389-AC	TAIWN-G	4818845	619806221	300	48	0	
CY7C09389-AC	TAIWN-G	4818845	619806221	1000	48	0	

[1] QTP 98368, Synchronous and Asynchronous Dual Port SRAM (3V and 5V), R42HD Technology, Fab 4 qualification.

Document History Page

Document Title: QTP 98516: LOW VOLTAGE SYNCHRONOUS/ASYNCHRONOUS DUAL PORT SRAM R42D TECHNOLOGY, FAB 4 QUALIFICATION
Document Number: 001-84798

Rev.	ECN No.	Orig. of Change	Description of Change
**	3819942	NSR	Initial Release
*A	4040255	JYF	Added CY7C037AV part no. in the qual report device coverage; Added industry standards of EFR, LFR and HAST in Reliability Tests Performed table.
*B	4583572	JYF	Sunset review: Updated QTP title page for template alignment.

Distribution: WEB

Posting: None