Phase-Shifted Full-Bridge Current-Doubler Implementation with XDPP1100

Application Guide

About this document

Scope and purpose

This document showcases the design and evaluation of XDPP100 digital controller to control a high voltage (380 Vdc) Phase-Shifted Full-Bridge (PSFB) DC/DC converter. The PSFB converter is equipped with 600V GaN FETs which allows high frequency switching at 350 KHz to enable high power density design.

Intended audience

Power supply design engineers who wish to evaluate XDPP1100.

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1 System Description

Phase-Shifted Full-Bridge with Current-Doubler output (PSFB-CDR) DC/DC converter is used in wide range of applications such as telecom and server. With the rising demand of smart and compact power supplies that can deliver as much power as possible, power supply designers are migrating their existing designs to use digital controller and Gallium Nitride (GaN) FETs.

The power converter described in this document uses a digital controller called XDPP1100 from Infineon. This digital controller is designed specifically for DC/DC applications and it offers several benefits from other controllers such as dedicated digital hardware control loop that enables low-latency control as well as dual-loop support for interleaved applications.

Beside XDPP1100, the power converter described in this document uses GaN FETs called IGT60R070G1 to enable high frequency switching. This GaN FETs support up to 600Vdc input voltage and are switched at 350 KHz.

The block diagram of the PSFB-CDR implementation is shown in the following figure.

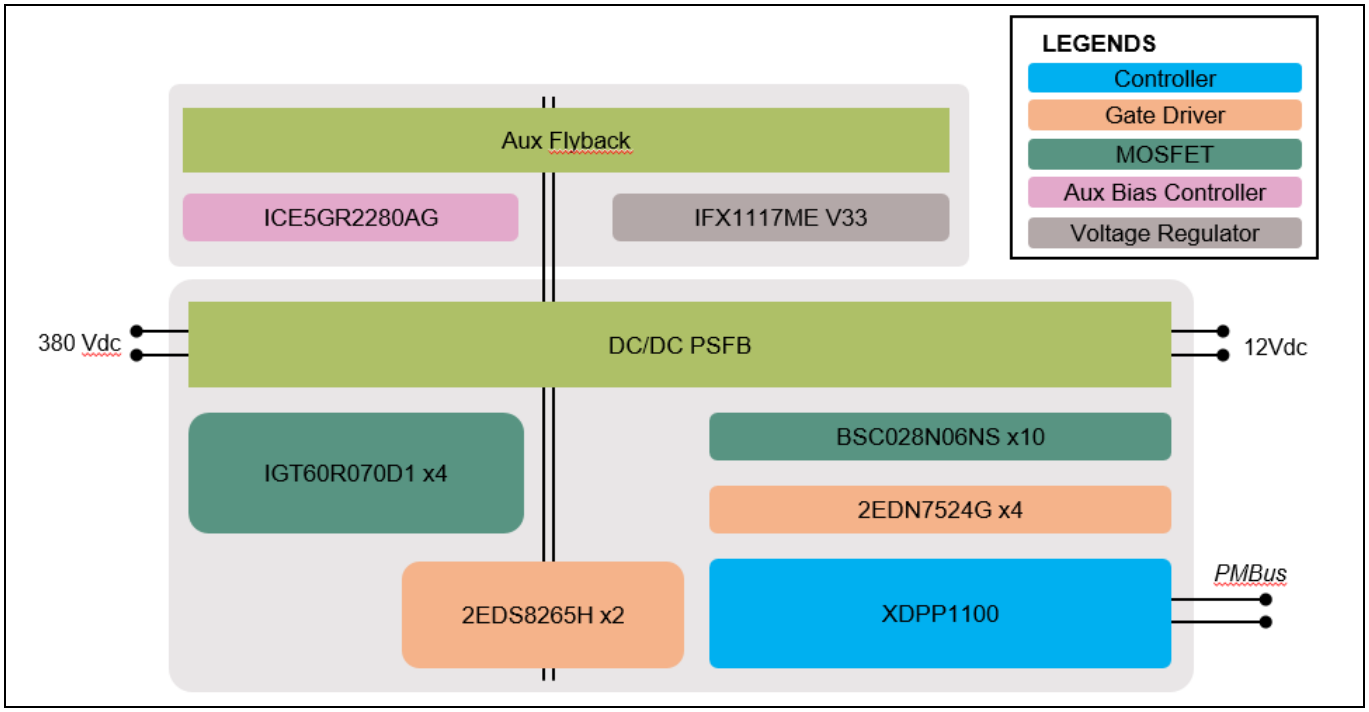


Figure 1 System Block Diagram

The complete board assembly is shown in the following figure.

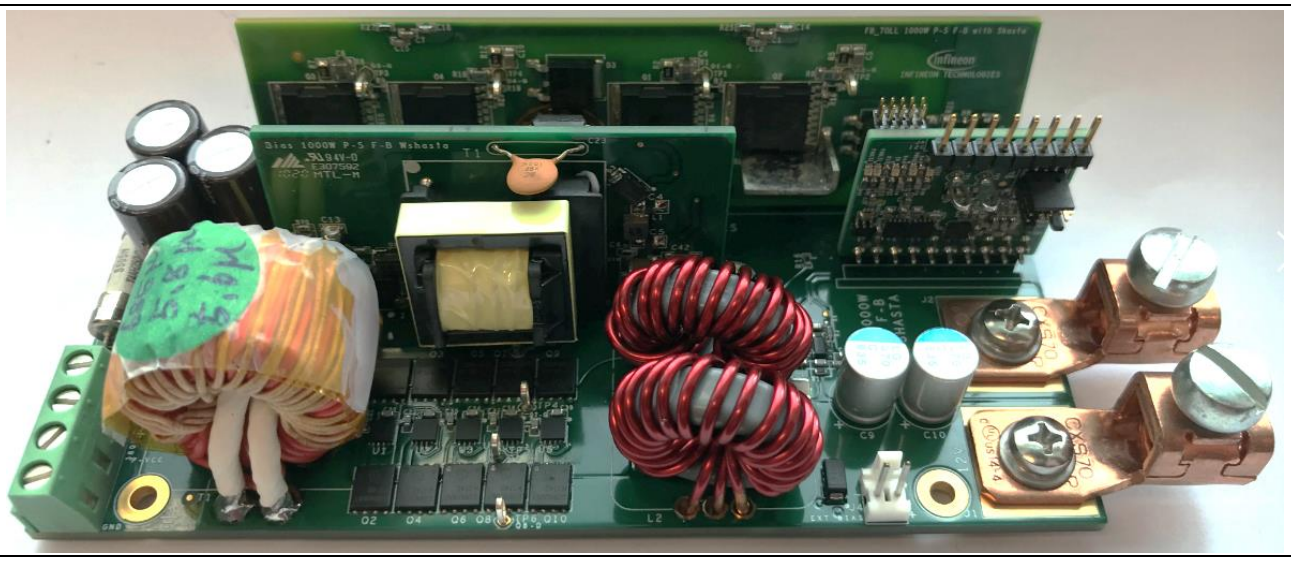


Figure 2 Fully Assembled 1000W PSFB-CDR board

1.1 Specification

The board specification is listed in the following table.

Table 1 Power Board Specification

Parameter	Min	Typ	Max	Unit
Output Voltage (V_{OUT})	-	12	-	V
Output Current (I_{OUT})	-	-	84	A
Input Voltage (V_{IN})	360	380	400	V
Input Current (I_{IN})	-	2.63	2.8	A
Rated Power (P_{OUT})	-	1000	1024	W
Switching Frequency (F_{SW})	-	350	-	KHz
Efficiency	-	-	95.36	%

The PSFB-CDR board is designed to be as modular as possible where each board has a specific functionality. This is done intentionally for the following reasons:

- *Power density*. By assigning a base board and stacking three boards vertically on it, the total volume of the power supply becomes more compact therefore give higher power density.
- *Reusability*. Since each board has a dedicated function, it is possible to reuse some of the boards for future designs.
- *Troubleshooting convenience*. It will be easier to pinpoint and fix any issues.

The following subsections will further elaborate each board.

1.2 Main Board

This is the ‘backbone’ of the whole system, providing the bases for other boards to mount. It also contains the Synchronous Rectification (SR) switches and output filter.



Figure 3 Main Board

The following Infineon components are used in the board:

Table 2 Infineon Components used in Main Board

Part Number	Description	Usage
BSC028N06NS	OptiMOS™ 60V Power-Transistor	PSFB secondary-side Synchronous Rectification (SR) switches
2EDN7524G	EiceDRIVER™ dual-channel gate-driver	Gate driver for SR switches

1.3 Full Bridge Board

This board contains the full bridge circuitry which make use of GaN switches for high-frequency switching as well as resonant inductor to enable Zero Voltage Switching (ZVS).

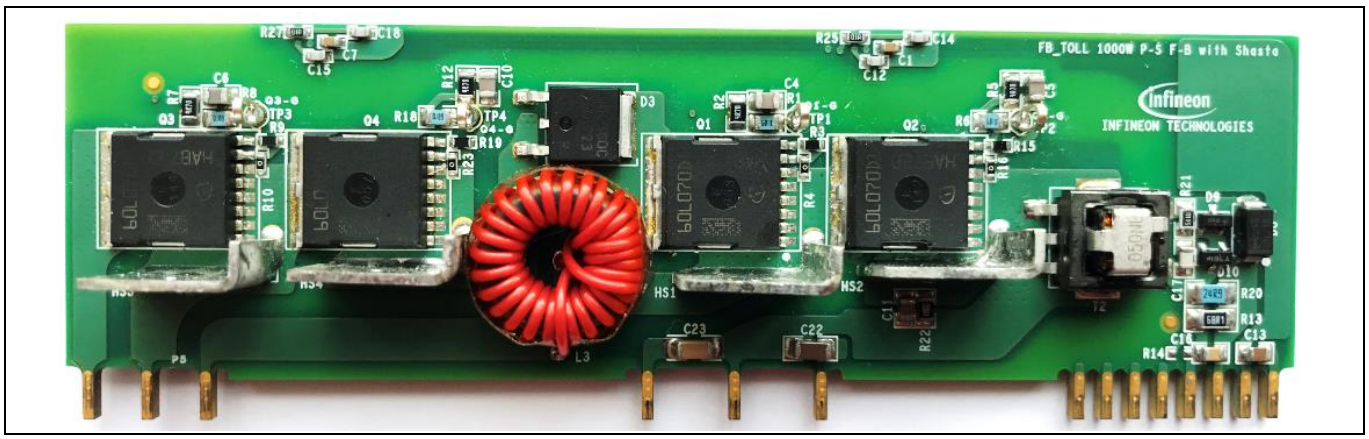


Figure 4 Full-Bridge Board

The following Infineon components are used in the board:

Table 3 Infineon Components used in Full Bridge Board

Part Number	Description	Usage
IGT60R070D1	CoolGaN™ 600V enhancement-mode Power Transistor	PSFB primary-side power switches
2EDS8265H	EiceDRIVER™ dual-channel isolated gate-driver	Gate driver for primary-side switches
IDD09SG60C	thinkQ!™ SiC Schottky Diode	Freewheeling diode for resonant circuit

Combined with the Main Board, both boards make up the power-stage of the PSFB-CDR.

1.4 Control Board

This board contains the XDPP1100 digital controller that acts as the 'brain' of the whole system. Phase-Shifted Full-Bridge Current-Doubler topology and its control algorithms are supported natively.

The Control Board is shown in the following figure.

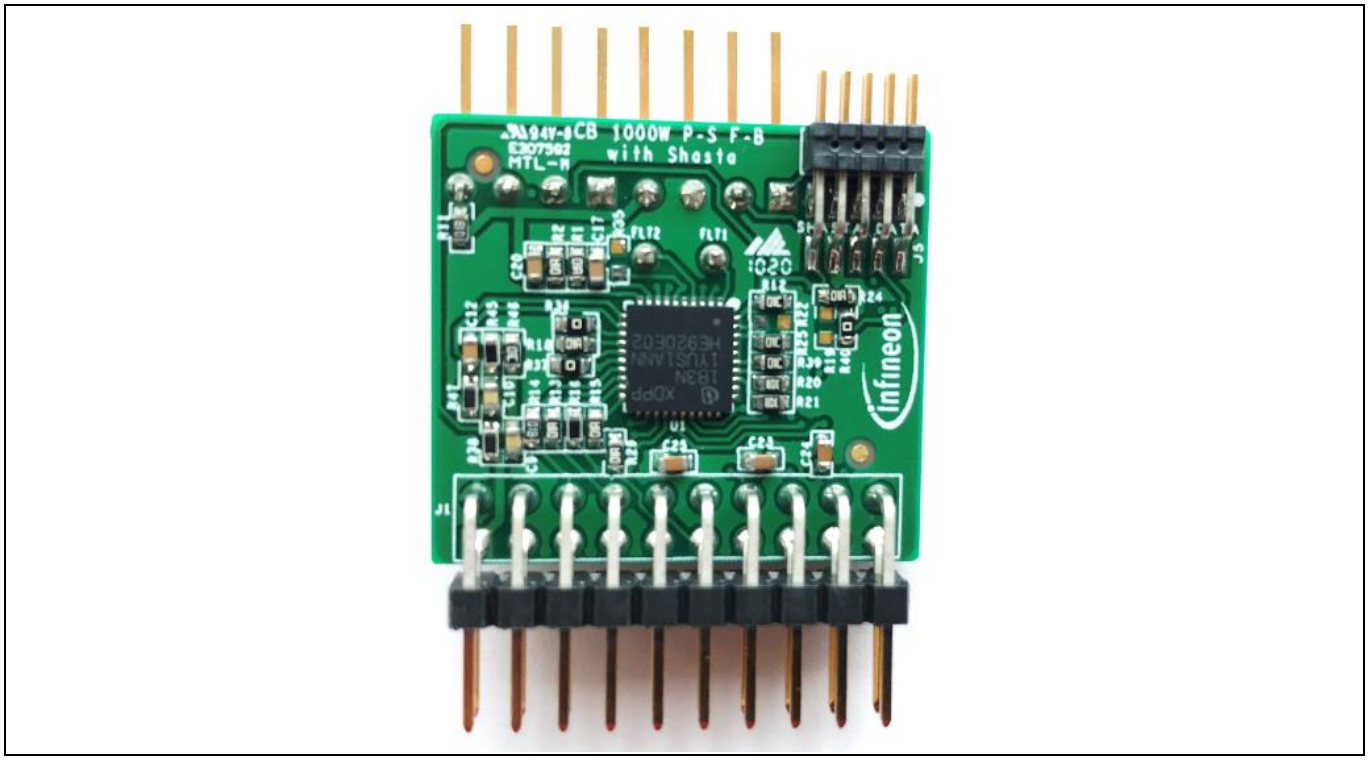


Figure 5 Control Board

There are two ways user can configure the PSFB control and behavior:

- *PMBus setting configuration*. PMBus is a communication protocol that is built on top of another communication protocol called I2C and designed specifically for power management applications. It has become the standardized communication protocol for digital power applications. XDPP1100 is compliant with PMBus Power System Management Protocol Specification, revision 1.3.1.
- *Direct register configuration*. Altough PMBus provides convenience and a standardized way to configure power management applications, direct register configuration is also provided in XDPP1100 for advanced users who seek to further optimize the digital control performance.

Some of the important PMBus settings and register configuration will be highlighted in Section 2. For user convenience, however, both PMBus setting configuration and direct register configuration can be stored in a file for later use on XDPP1100 and therefore removes the hassles of reading through PMBus and register documentations.

The following Infineon components are used in the board:

Table 4 Infineon Components used in Control Board

Part Number	Description	Usage
XDPP1100	XDP™ digital power supply controller	Digital controller for PSFB

1.5 Auxiliary Bias Board

This board implements the auxiliary power supply which are required to supply the gate drivers, signal conditioning circuitry and the digital controller. It uses flyback topology to provide galvanic isolation between primary-side and secondary-side of PSFB-CDR board.

Since the digital controller is placed on the secondary-side along with critical signal conditioning circuits (e.g. current sense Op-Amp), the auxiliary flyback regulation is also implemented on the secondary-side to ensure stable output voltages to both digital controller and signal conditioning circuits.

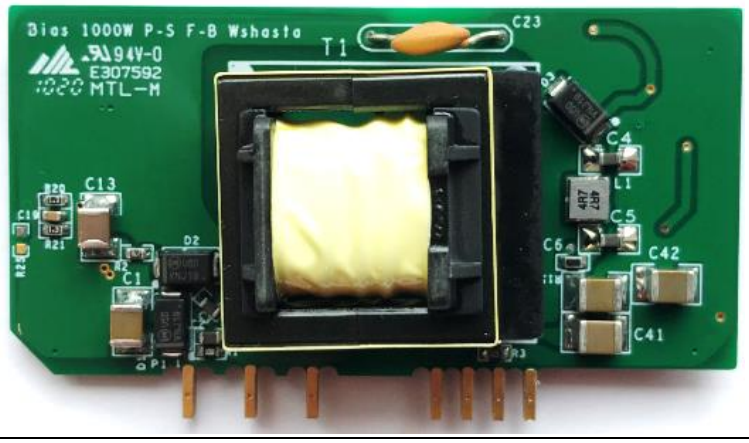


Figure 6 Auxiliary Bias Board

The Auxiliary Bias Board specification is shown in the following table.

Table 5 Auxiliary Bias Board Specification

Parameter	Min	Typ	Max	Unit
Secondary-Side Output Voltage 1 (V_{SEC1})	-	12.0	-	V
Secondary-Side Output Voltage 2 (V_{SEC2})	-	-5.0	-	V
Primary-Side Output Voltage (V_{PRI})	-	12.0	-	V
Input Voltage Range	350.0	380.0	410.0	V
Switching Frequency	-	125	-	KHz

The following Infineon components are used in the board:

Table 6 Infineon Components used in Auxilliary Bias Board

Part Number	Description	Usage
ICE5GR2280AG	CoolSET™ fixed-frequency flyback controller	Auxiliary bias power supply controller
IFX1117ME V33	3.3V_{DC} Linear Voltage Regulators	Voltage supply for XDPP1100

The transformer used is designed by Wurth Electronics with part number of 750344550.

2 Configuration

As highlighted earlier, there are two ways to configure XDPP1100 namely via *PMBus setting configuration* and *direct register configuration*. However, both of these configurations can be stored in a file for later use on XDPP1100.

Some (not all) of the configuration are highlighted in this section to illustrate XDPP1100 configuration process.

2.1 PMBus Setting Configuration

The following table highlights some of the PMBus configuration for the PSFB board. These configurations are easily found in any other PMBus compliant systems.

Table 7 PMBus Configuration

CMD	Name	Value	Description
0x00	PAGE	0	PMBus Page 0. There are two pages in XDPP1100: Loop 0 and Loop 1. This configuration is using Loop 0 and therefore Page is set to 0.
0x01	OPERATION	On	Set to ON to turn on the system immediately
0x02	ON_OFF_CONFIG	0x1F	Respond to operation and EN pin, EN polarity active high
VOUT Configuration			
0x20	VOUT_MODE	-12	Linear Format exponent for VOUT
0x21	VOUT_COMMAND	12.000V	Output Voltage Command/Reference
0x29	VOUT_SCALE_LOOP	0.0986328125	Output Voltage sensing resistor divider ratio
Switching Frequency and Duty Cyle Configuration			
0x32	MAX_DUTY	85%	Maximum duty cycle
0x33	FREQUENCY_SWITCH	350KHz	Switching Frequency
Output OVP Configuration			
0x40	VOUT_OV_FAULT_LIMIT	14.0000V	Fault Threshold for Output Over Voltage
0x42	VOUT_OV_WARN_LIMIT	13.0000V	Warning Threshold for Output Over Voltage
Output UVP Configuration			
0x43	VOUT_UV_WARN_LIMIT	9.000V	Warning Threshold for Output Under Voltage
0x44	VOUT_UV_FAULT_LIMIT	8.000V	Fault Threshold for Output Under Voltage
Output OCP Configuration			
0x46	IOUT_OC_FAULT_LIMIT	85.0A	Fault Threshold for Output Over Current
0x4A	IOUT_OC_WARN_LIMIT	83.0A	Warning Threshold for Output Over Current
Input OVP Configuration			
0x55	VIN_OV_FAULT_LIMIT	440.0V	Fault Threshold for Input Over Voltage
0x57	VIN_OV_WARN_LIMIT	420.0V	Warning Threshold for Input Over Voltage
Input UVP Configuration			
0x58	VIN_UV_WARN_LIMIT	360.0V	Warning Threshold for Input Under Voltage
0x59	VIN_UV_FAULT_LIMIT	350.0V	Fault Threshold for Input Under Voltage
Input OCP Configuration			

Configuration

CMD	Name	Value	Description
0x5B	IIN_OC_FAULT_LIMIT	3.50A	Fault Threshold for Input Over Current
0x5D	IIN_OC_WARN_LIMIT	2.0A	Warning Threshold for Input Over Current
Output OPP Configuration			
0x6A	POUT_OP_WARN_LIMIT	1010.0W	Warning Threshold for Output Over Power
Input OPP Configuration			
0x6B	PIN_OP_WARN_LIMIT	1300.0W	Warning Threshold for Input Over Power
Transformer and sensing configuration			
0xCD	MFR_VRECT_SCALE	0.33	Secondary side Rectified Voltage sensing divider resistor
0xCE	MFR_TRANSFORMER_SCALE	0.091	Transformer scaling (Nsec/Npri)

2.2 Register Configuration

XDPP1100 implements two hardware control blocks namely *PID Filter* and *Feedforward Filter* as the control modules:

- PID Filter is used to compensate Output Voltage against sudden load change (load transient).
- Feedforward Filter is used to compensate Output Voltage against sudden input voltage change (input transient).

The values coming out from both PID Filter and Feedforward Filter blocks are then summed together to make up the output duty cycle that control the PSFB-CDR. It is also important to clamp the summed output of both Filters to prevent overflow.

In XDPP1100 Implementation, both PID Filter and Feedforward Filter reside in a module called *PID Block*, as illustrated in the following figure. For more information on other blocks in XDPP1100, refer to [2].

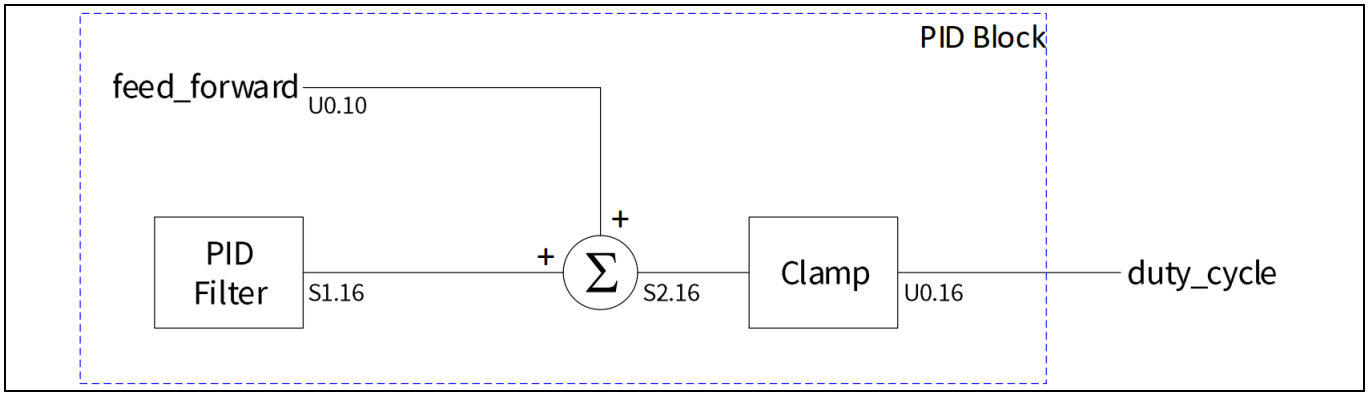


Figure 7 Diagram of PID Block

It is noteworthy that the output of PID Filter is formatted as S1.16, the output of Feedforward Filter is formatted as U0.10 while the output duty cycle is formatted at U0.16. For more information on number format in XDPP1100, refer to [3].

2.2.1 PID Filter Register Configuration

As in the case with standard PID Filter, the configuration of Proportional, Integral and Derivative coefficients K_P, K_I and K_D are done directly via register, as shown in the following table.

Table 8 PID Filter Direct Register Configuration

Register Name	Value	Description
pid0_kp_index_1ph	32	PID proportional coefficient index
pid0_ki_index_1ph	28	PID integral coefficient index
pid0_kd_index_1ph	77	PID derivative coefficient index

2.2.2 Feedforward Filter Register Configuration

Feedforward Filter reads and inverts the Input Voltage (feedforward = $1/V_{IN}$) to produce inverse relationship between input voltage and duty cycle:

- When VIN decreases, Feedforward Filter output increases and therefore, duty cycle will increase
- When VIN increases, Feedforward Filter output decreases and therefore, duty cycle will decrease

In XDPP1100, the Feedforward Filter implementation is shown in the following figure.

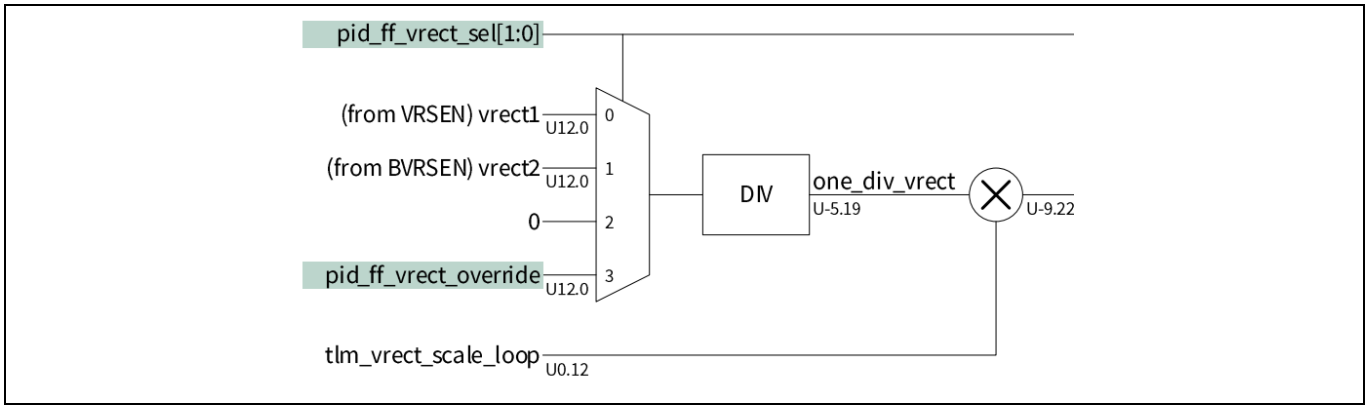


Figure 8 Feedforward Filter in XDPP1100

The two registers highlighted in green are configurable and their descriptions as shown in the following table.

Table 9 Feedforward Filter Register Configuration

Register Name	Value	Description
pid0_ff_vrect_sel	0	Feedforward (FF) Vrect source select
pid0_ff_vrect_override	0	Feedforward (FF) override value

Since pid0_ff_vrect_sel is set to 0, the multiplexer branch 0 "**(from VRSEN) vrect1**" will be used for feedforward calculation. VRSEN is the ADC module used for sensing the PSFB transformer's secondary-side voltage, therefore the name Rectified Sensing. For more information on other modules, refer to [1]. By sensing the transformer's secondary-side voltage and assuming transformer turns ratio is known, the Input Voltage (V_{IN}) at primary side can be derived.

The value of vrect1 is then pass through a DIV block, producing **one_div_vrect**. This is the raw Feedforward Filter output that will be combined with PID Filter output later on.

Since XDPP1100 uses voltage divider resistors to read the PSFB transformer's secondary-side voltage (VRSEN), **tlm_vrect_scale_loop** register must be updated to cater for the voltage divider ratio.

3 Performance

This section showcases system performance and some waveforms to highlight system behavior.

3.1 Efficiency measurement setup

The efficiency measurement and evaluation is illustrated in the following block diagram.

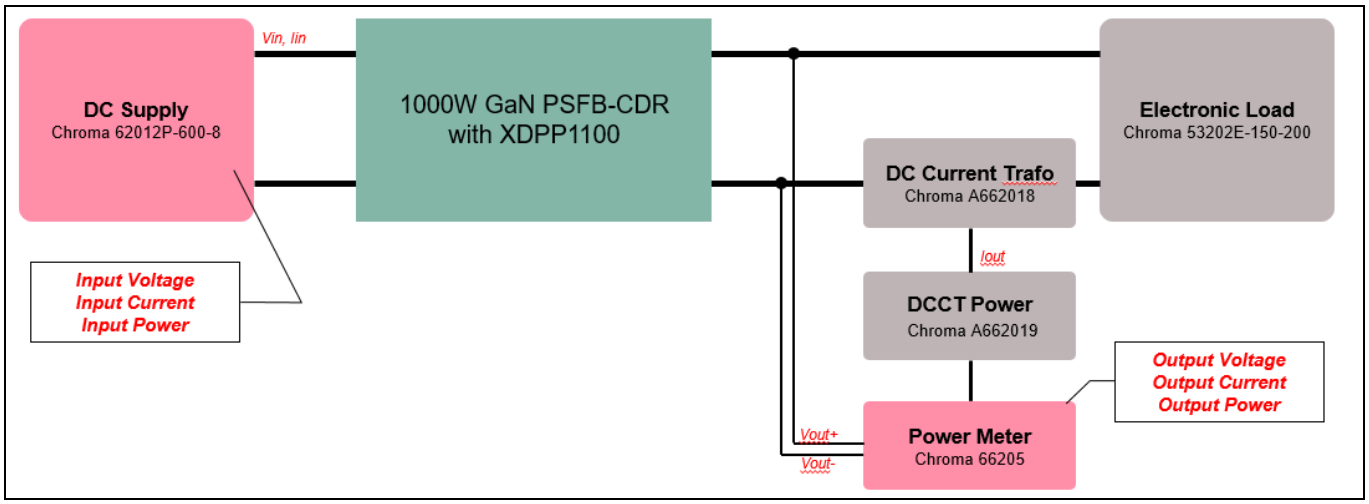


Figure 9 Efficiency Measurement Setup

3.2 Efficiency graph

The PSFB-CDR board efficiency curve at different input voltage range is shown below.

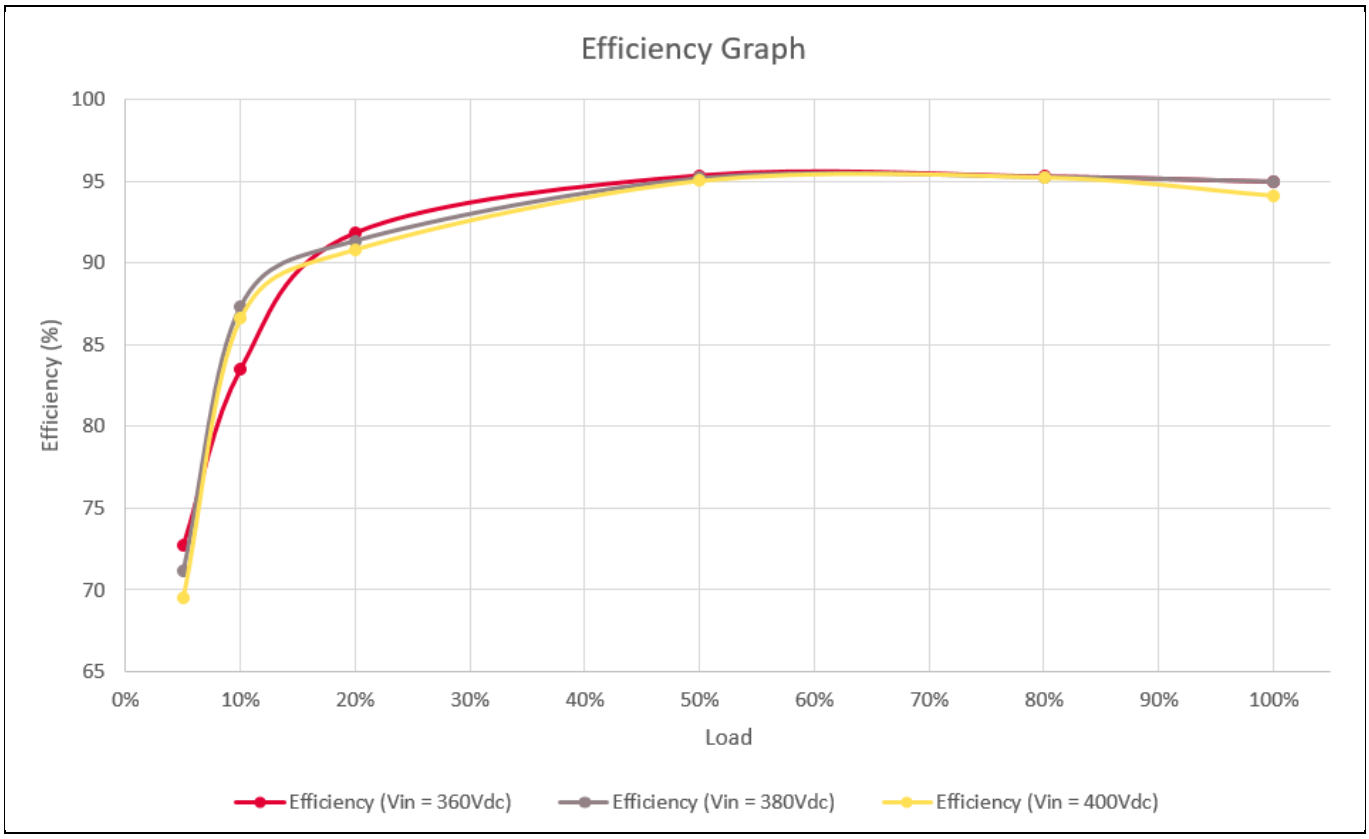


Figure 10 Efficiency graph

Efficiency data summary are shown in the following table.

Table 10 Summary of Efficiency Measurement (in %)

Load	Efficiency (V_{IN} = 360Vdc)	Efficiency (V_{IN} = 380Vdc)	Efficiency (V_{IN} = 400Vdc)
5%	72.74	71.17	69.52
10%	83.52	87.36	86.61
20%	91.85	91.36	90.81
50%	95.36	95.19	95.02
80%	95.29	95.27	95.23
100%	94.97	94.98	94.11

4 Selected waveforms

This section showcases the selected waveforms across different operation.

4.1 Steady-State

The waveforms showcasing PSFB modulation signals when operating in steady-state are shown as following.

Table 11 Steady-State waveform signals description

Signal Name	Color	Resolution	Description
P1	Yellow	200V/div	Leading-leg half-bridge signal, probed at the leading-leg PSFB primary-side transformer after the resonant inductor P1
P2	Pink	200V/div	Lagging-leg half-bridge signal, probed at the lagging-leg PSFB primary-side transformer P2
SR1	Green	20V/div	Synchronous Rectification signal acting on the 1st PSFB Current Doubler (CDR) at secondary-side transformer on the S1 node
SR2	Purple	20V/div	Synchronous Rectification signal acting on the 2nd PSFB Current Doubler (CDR) at secondary-side transformer on the S2 node

The probes for SR1 and SR2 are grounded on the secondary side. P1 and P2 are left floating.

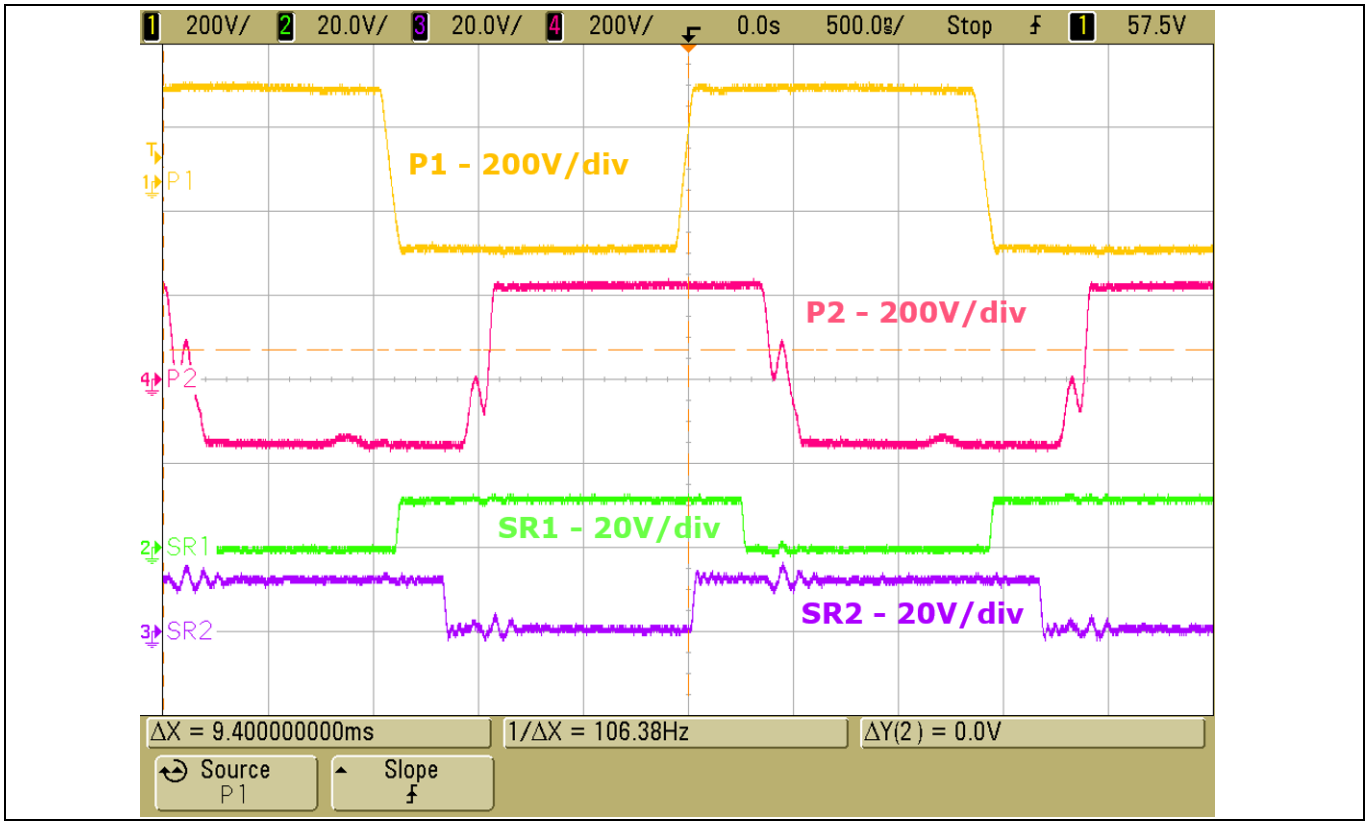


Figure 11 Steady-State waveform at Load = 20%, Vin = 380Vdc

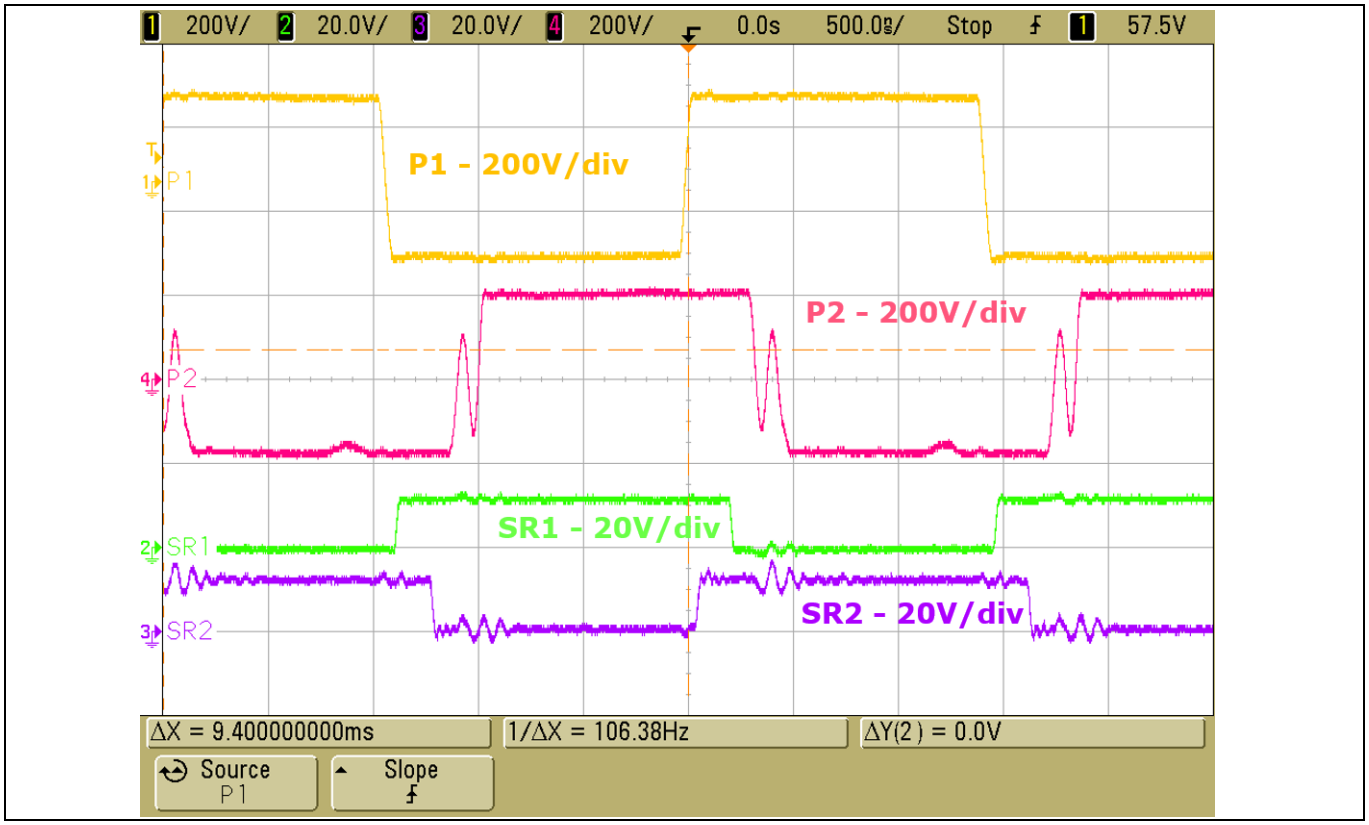


Figure 12 **Steady-State waveform at Load = 50%, Vin = 380Vdc**

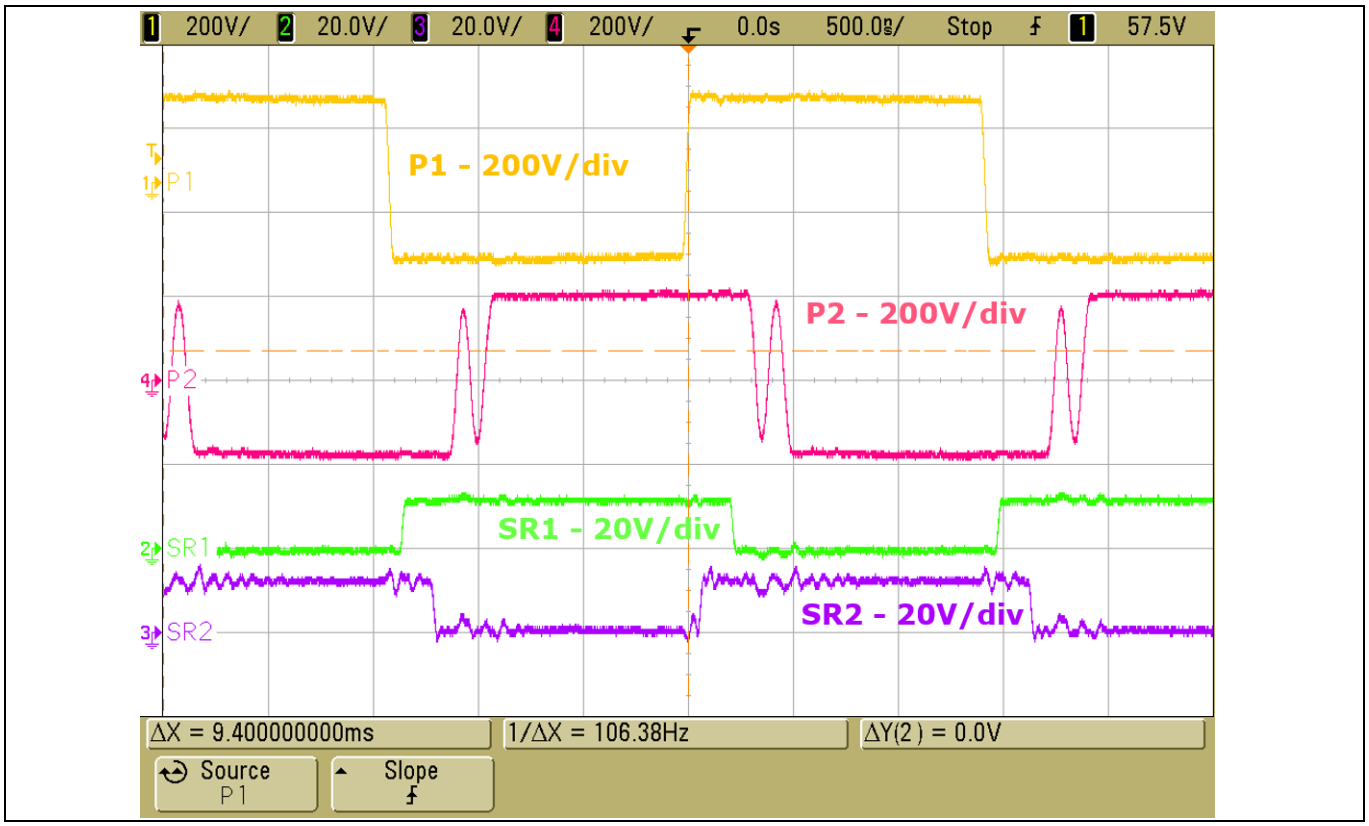


Figure 13 **Steady-State waveform at Load = 100%, Vin = 380Vdc**

4.2 Load Transient

The waveforms showcasing PSFB load transient are shown as following.

Table 12 Load Transient waveforms Signal Description

Signal Name	Color	Resolution	Description
VOUT	Yellow	2V/div	Output Voltage of PSFB-CDR board, controlled at 12Vdc
IOUT	Pink	20A/div	Output Current of PSFB-CDR board, transitioning from 16.66A (20%) to 66.66A (80%)

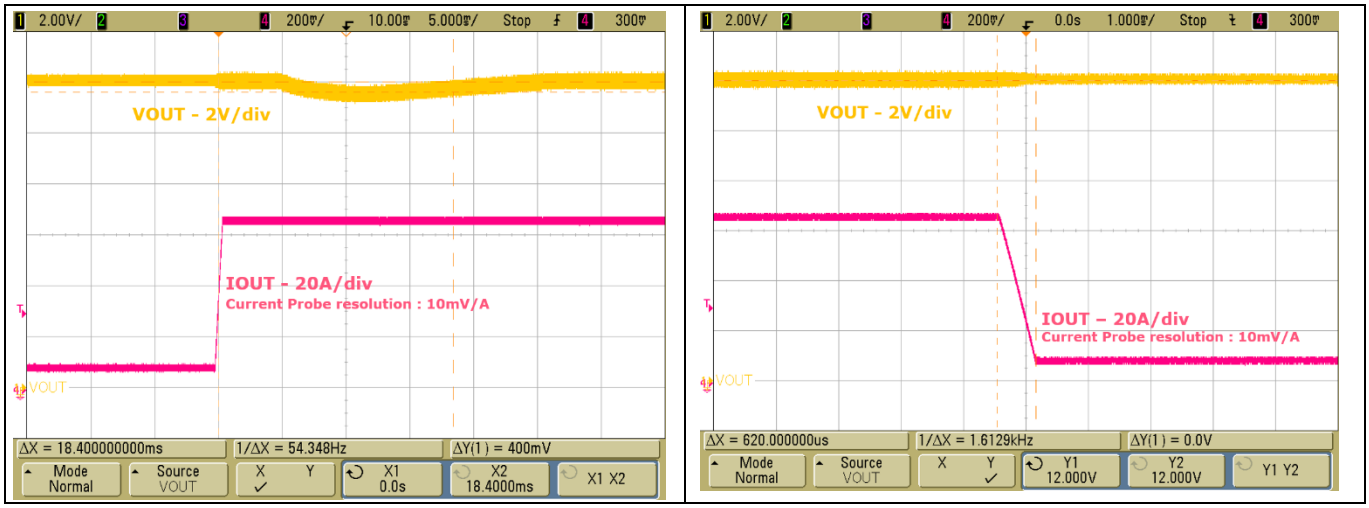


Figure 14 Load Transient Waveform between 20% and 80%, Vin = 380Vdc

4.3 Input Voltage Transient

The waveforms showcasing PSFB input voltage transient are shown as following.

Table 13 Input Voltage Transient waveforms Signal Description

Signal Name	Color	Resolution	Description
VIN	Green	50V/div	Input Voltage of PSFB-CDR board, transitioning between 380Vdc to 360Vdc
VOUT	Yellow	2V/div	Output Voltage of PSFB-CDR board, controlled at 12Vdc
IOUT	Pink	20A/div	Output Current of PSFB-CDR board, at 50% load

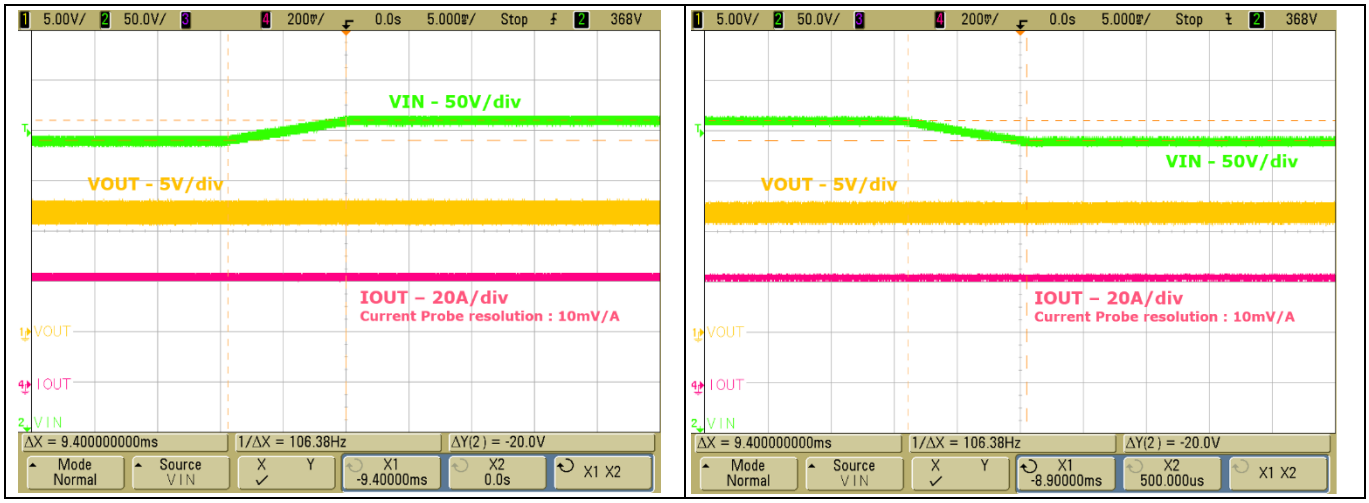


Figure 15 Input Voltage Transient Waveform between 380Vdc and 360Vdc, Load = 50%

4.4 Softstart and Shutdown

The waveforms showcasing PSFB softstart and shutdown are shown as following.

Table 14 Softstart and Shutdown waveforms Signal Description

Signal Name	Color	Resolution	Description
VOUT	Yellow	2V/div	Output Voltage of PSFB-CDR board, controlled at 12Vdc
IOUT	Pink	50A/div	Output Current of PSFB-CDR board, at 50% load

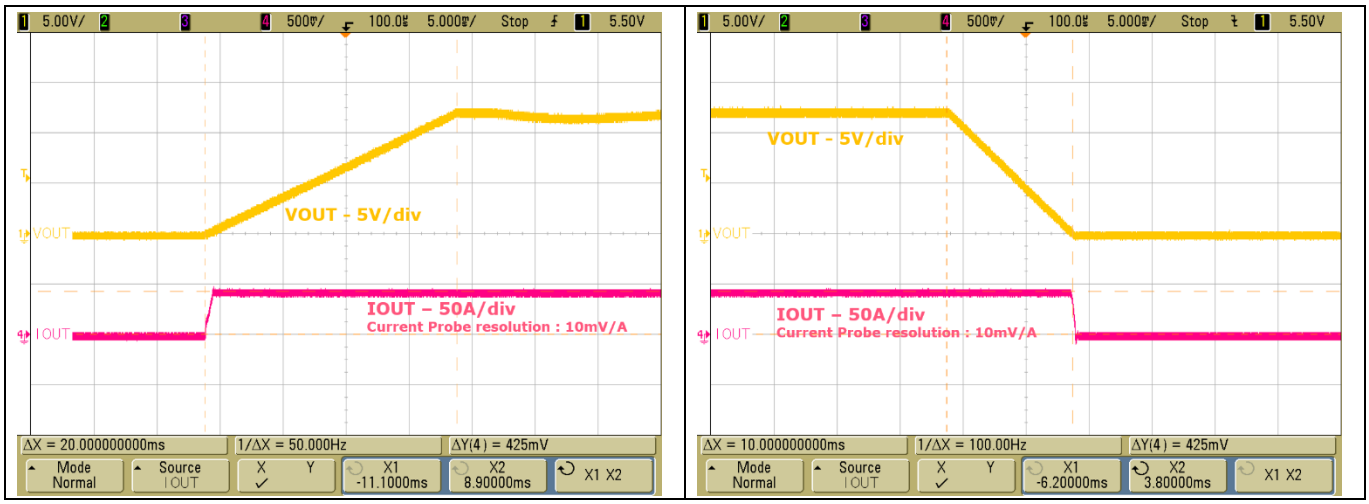


Figure 16 Softstart and Shutdown. Vin = 380Vdc, Load = 50%

5 Summary

This document introduces a complete Infineon system solution for a 1000W PSFB-CDR isolated DC-DC converter achieving 95.36 percent peak efficiency.

XDPP1100 is a highly integrated and programmable digital power supply controller. It has a unique architecture that includes many optimized power-processing digital blocks to enhance the performance of isolated DC-DC converters, reduce external components and minimize firmware development effort. For advanced power conversion and monitoring, the XDPP1100 also provides accurate telemetry and power management bus (PMBus) interface for system communication. These advanced features make it an ideal power controller for modern high-end power systems employed in telecom and server infrastructure.

Specific power management peripherals have been added to enable high efficiency across the entire operating range, high integration for increased power density, reliability and lowest overall system cost and high flexibility with support for the widest number of control schemes and topologies. Such peripherals include: synchronous rectification, input voltage feed-forward, copper trace current sense with temperature compensation, secondary-side input voltage sensing, soft-start with pre-bias, feedback loop open or short-circuit protection and fast load-transient response.

The XDPP1100 supports many commonly used DC-DC topologies such as hard-switched full-bridge and half-bridge, phase-shifted full-bridge, active clamp forward, full-bridge and half-bridge current doubler rectifier, interlaved active clamp forward, interlaved half-bridge, and interleaved full-bridge. A dual-rail version of XDPP1100 also supports pre-buck or post-buck configuration.

When combined with other Infineon’s best-in-class devices such as CoolGaN™, OptiMOS™, EiceDRIVER™ and CoolSET™, this system solution is able to demonstrate the feasibility of using XDPP1100 on a high-voltage 1000W PSFB CDR for telecom and server applications.

6 References

[1] Infineon Technologies, 2020. “XDPP1100 Digital Power Supply Controller” Datasheet.

[2] Infineon Technologies, 2020. “Application Guide – Digital Power Controller XDPP1100”, AN_2003_PL88_2006_221026, Application Guide.

[3] Infineon Technologies, 2020. “Application Note – XDPP1100 Number Format and Conversion”, AN_2005_PL88_2006_073720, Application Note.

[4] Infineon Technologies, 2013. “ZVS Phase Shift Full Bridge CFD2 Optimized Design”, AN 2013-03, Application Note.

Revision history

Document version	Date of release	Description of changes
V0.2	21 July 2020	First draft

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