

87654321

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:

A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-60657-01.ZIP.

B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.

C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.

D. REMOVE ALL BURRS AND BREAK SHARP EDGES. .381 [.015] MAX RADIUS.

E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.

F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:

A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).

B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.

C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.

D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:

A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+ .0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.

B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

C. FILL ALL THRU VIAS USING NON-CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER. .005 [.0002] MINIMUM THICKNESS. DIMPLE DEPTH IN BGA PADS SHALL BE .025 [.001] MAXIMUM. THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.

4. SOLDER MASK:

A. APPLY LPI SOLDER MASK USING PROVIDED DATA.

B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.

C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:

A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:

A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.

B. ALL PCBs SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.

C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7. FINAL FINISH:

A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:

A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.

B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBs SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

10.FOLLOW VIA FILLING METHOD AS PER BELOW NOTES:

A. COMMON FOR ALL VIAS:

I. VIA WALL THICKNESS MIN 35um COPPER

II. FILL ALL VIA HOLES 7.87 MILL, 8 MILL, 10 MILL, 15 MILL WITH NONCONDUCTIVE EPOXY

INTENTIONAL NET SHORT

1. N17416139 & IOUT_CSP

2. VOUT_DC & IOUT_CSN

3. BB_IN & IIN_CSP

4. N17416246 & IIN_CSN

STACK-UP

1.6 mm
+/- 10%

LAYER DESCRIPTION	FINISH COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER
L01 - TOP	(2 OZ) 0.070 mm	50E	0.1879 mm	L02	90E	0.1397/0.1524 mm	L02
L02 - PLANE	(2 OZ) 0.070 mm	--	-----	---	---	----	---
L03 - PWR/SIG	(2 OZ) 0.070 mm	50E	0.1498 mm	L02	90E	0.1143/0.1778 mm	L02
L04 - BOTTOM	(2 OZ) 0.070 mm	50E	0.1879 mm	L03	90E	0.1397/0.1524 mm	L03

SEE BOM
NEXT ASSY

SEE BOM
USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN METRIC
WITH INCHES IN BRACKETS
.XXX .XX ANGLES
±.064 ±.13 ±.5°
[±.005] [±.01]

2

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DO NOT SCALE DRAWING

APPROVALS DATE

HUSA 14/12/23

ENGINEER RVBM 14/12/23

CHECKER

QA

PROJ. ENG.

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SIZE D

CAGE CODE -

CY P/N

600-60657-01

SCALE 1/1

SHEET 1 OF 2

REV 02

Infineon

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TITLE PCB FABRICATION,
EVAL_PMG1_B1_DRP KIT

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

FAB NOTES REV 04/05/17

ALLEGRO FILE: 600-60657-01.BRD