WHITEPAPER

Stackable buck regulators simplify multiphase design

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Abstract

In server and telecom applications, point-of-load (POL) power systems use single-phase integrated DC-DC buck regulators and multiphase converters to efficiently step down a distribution bus (e.g., 12 V) to lower voltages needed by microprocessors, application specific ICs (ASICs), and other digital chipsets. With advanced MOSFET and package technology, the maximum output DC current of an integrated single-phase POL converter such as TDA38740 [1] can reach 40 A.

However, with the increasing power consumption required by modern POL power systems, more power rails need maximum output current beyond the current capability of a single-phase POL converter. Although multiphase converters can be used for these power rails, some drawbacks may be considered.

First, the increased component count associated with a multiphase POL design leads to a higher bill of materials (BOM) cost. Additionally, it means increased design complexity. And then, there's the extra PCB area and layout effort required to accommodate a dedicated multiphase PWM controller and power stages.

On the other hand, in contrast with such a discrete multiphase solution, the same multiphase design goals can be achieved using integrated stackable POL converters. These devices, which are available from Infineon and others, provide a more cost-effective and compact solution when the total phase count is less than four.

In this whitepaper, the benefits of analog stackable integrated DC-DC buck regulators in general, and TDA38540 in particular, are discussed. TDA38540 can operate as a standalone buck regulator, or be configured in a stackable mode for a multiphase operation. It allows system designers to easily expand the output power with repeated layout, simplifying the design efforts. The TDA38540 buck regulator offers good current sharing performance as well as comprehensive protection features to ensure system-level reliability in the event of fault conditions.

Details of TDA38540's performance and operation are discussed here and a design example is presented to illustrate the application of this stackable regulator in a two-phase design.

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1 Benefits of stackable POLs

Stackable POL converters are integrated single-phase POLs that can be paralleled to increase the total output current capability. Since the circuit and layout design of each stackable POL is the same, system designers can design a "common building block" (CBB) in single-phase, and stack different numbers of CBBs per the current requirements of the application, making the design scalable.

Besides the design scalability, stackable POLs can also provide other potential design benefits. First, by distributing the power losses across more MOSFETs, the reduction in conduction losses is more than the increase in switching losses at medium and heavy load, resulting in better efficiency and thermal performance. See the efficiency comparison in Figure 1.

Secondly, stackable POLs offer better transient response than single-phase POLs. As an example, a two-phase operation using stackable POLs can reduce C_{out} by 28%, as compared to a constant on-time (COT) based single-phase POL solution, as shown in Table 1.

Thirdly, they enable reduced input ripple current by interleaved operation. As shown in Figure 2, going from a single-phase operation to a two-phase operation, the input capacitor current is reduced from 12 A to 8 A at 40 A output current. This allows the total number of input capacitors to be reduced from four to three, if the RMS current of an input capacitor is rated for 3 A. As a result, a stackable POL improves the overall performance for applications with a medium or heavy load.

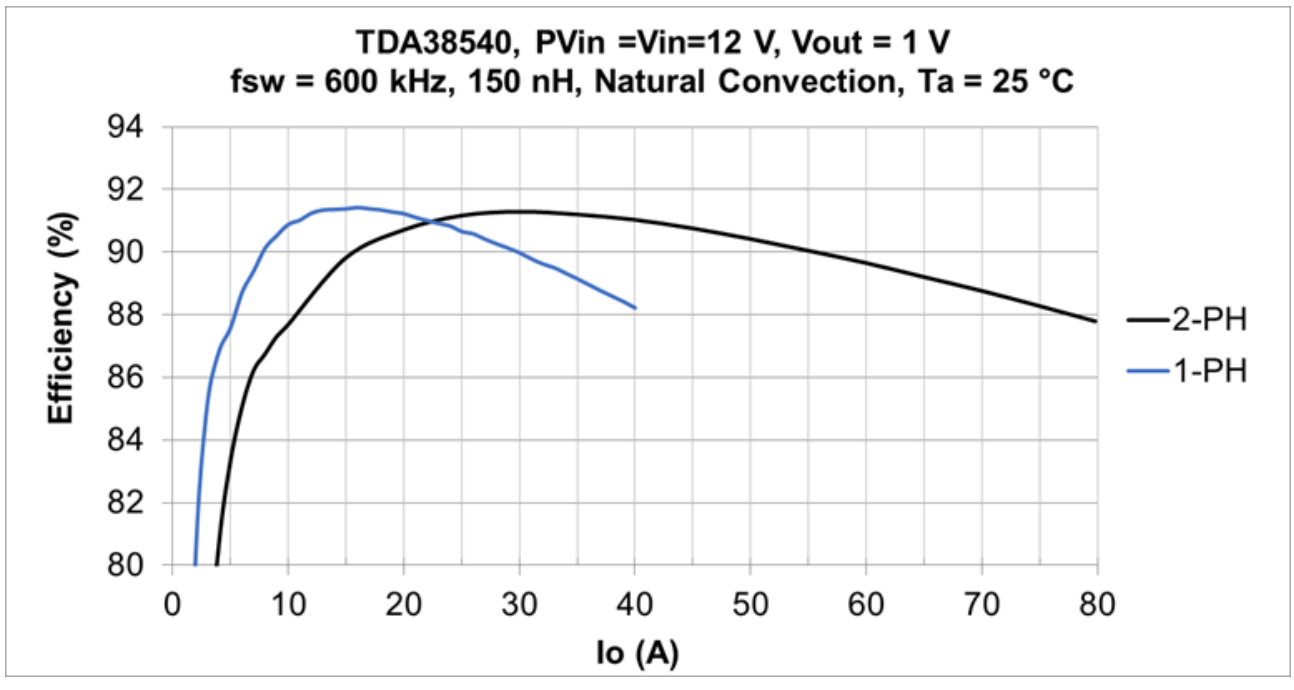


Figure 1 Efficiency comparison between single-phase and two-phase configuration

Table 1 Comparison of C_{out} between single-phase POL and two-phase stackable POL for transient load response

Design specifications	COT-based single-phase POL	Two-phase TDA345C0
V_{in} = 12 V, V_{out} = 0.79 V, f_{sw} = 1 MHz, load step = 15 A, AC + DC tolerance = 3%	C_{out_total} = 2350 µF	C_{out_total} = 1692 µF

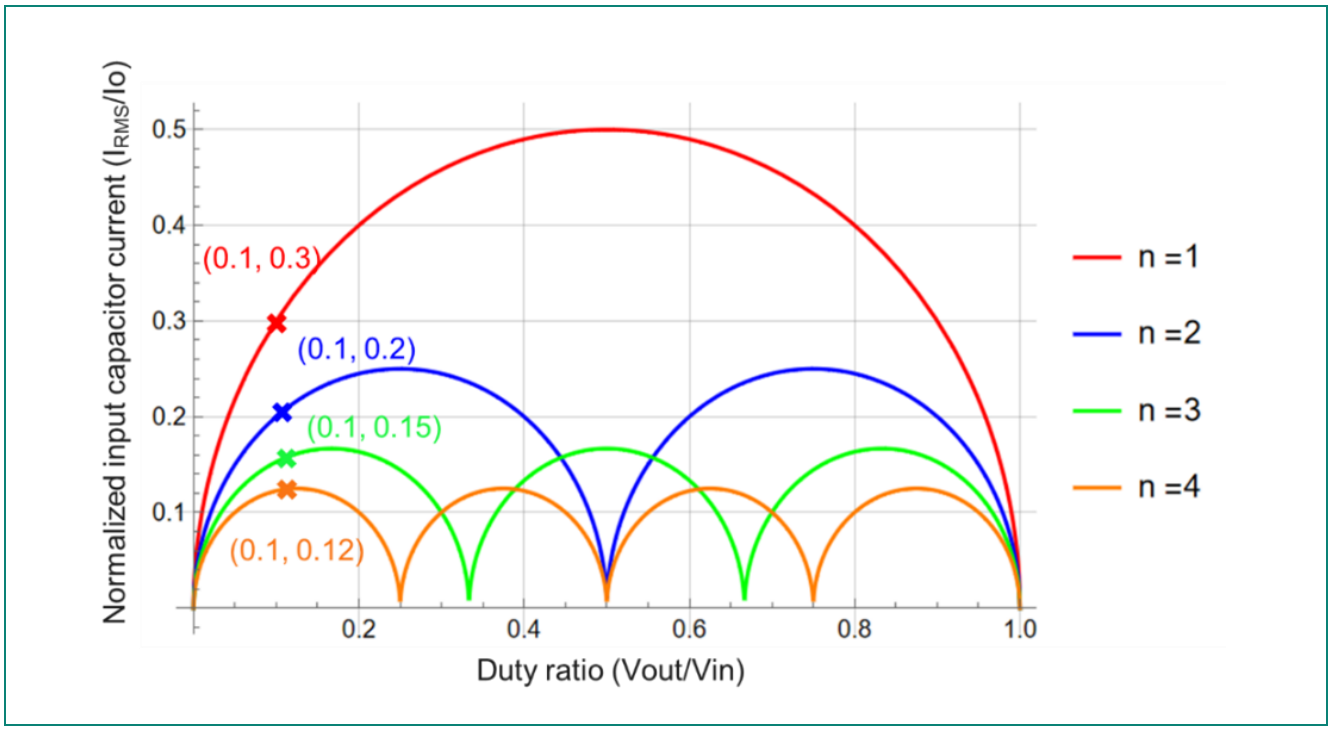


Figure 2 Normalized input capacitor current (I_{rms}/I_o) vs. duty ratio where n is phase count

In this whitepaper, a new stackable integrated DC-DC synchronous buck regulator, TDA38540 [2] is discussed. It integrates a PWM controller with high- and low-side MOSFETs in a small, 5 mm × 6 mm PQFN package. Thanks to Infineon OptiMOS™ 5 technology combined with robust packaging, TDA38540 offers high system efficiency, low switching losses, and improved MOSFET roughness. In addition, TDA38540 has been qualified for operation at a junction temperature up to 150°C.

Table 2 Comparison of key specifications between TDA38540 and a competitor

	TDA38540	Competitor's part
PV_{in} range	4.5 V to 17 V with int LDO 3 V to 17 V with ext VCC	4 V to 16 V
V_{out} range	0.6 V to 6 V	0.6 V to 5.5 V
Max I_{out}	40 A	40 A
f_{sw} range	400 kHz to 2 MHz (8 options)	300 kHz to 2 MHz (standalone) 300 kHz to 1 MHz (stackable mode)
Recommended operating T_j	-40°C to 150°C	-40°C to 125°C
Maximum phase count	4	2
Package size	5 mm × 6 mm	5 mm × 7 mm

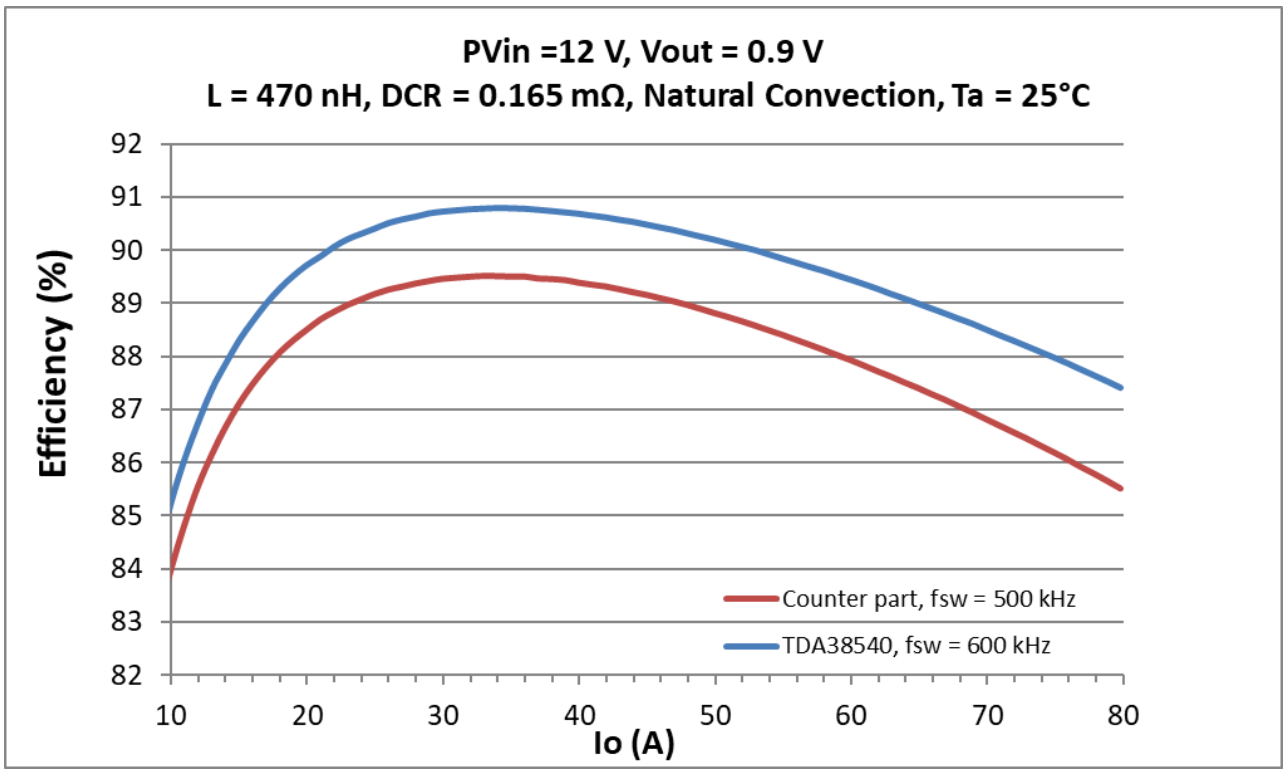
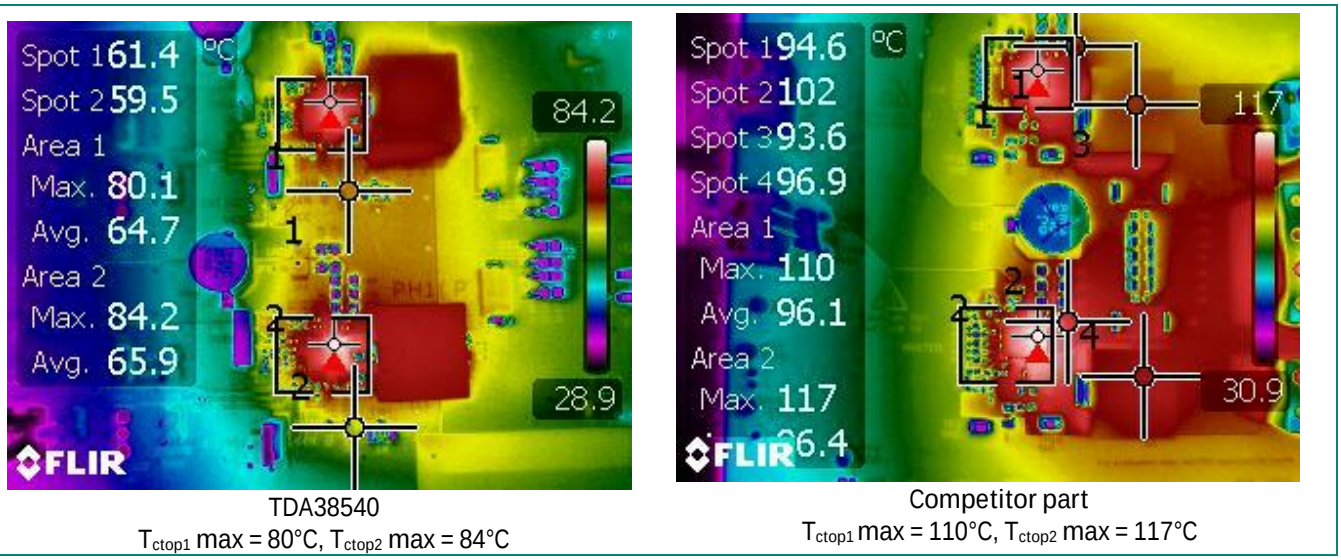


Figure 3 Two-**phase efficiency comparison between TDA38540 vs. a competitor's part**



TDA38540
T_{ctop1} max = 80°C, T_{ctop2} max = 84°C

Competitor part
T_{ctop1} max = 110°C, T_{ctop2} max = 117°C

Figure 4 Two-phase thermal comparison. TDA38540 and a competing part are tested under these conditions: V_{in} = 12 V, V_{out} = 0.9 V, f_{sw} = 500 kHz (counterpart), and f_{sw} = 600 kHz (TDA38540) with natural convection and no heatsink

2 Control architecture

TDA38540 implements a proprietary emulated-peak-current-mode control [3] including one voltage loop and two current loops. In a multiphase operation, one TDA38540 is configured as a primary phase, and the rest are secondary phases. The voltage loop of the primary phase senses the output voltage and feeds it to an internal transconductance error amplifier. Its output, VSHARE, is then shared with all secondary phases to set the reference for the “peak” current of each phase.

An internal ramp compensation is added to the inner current loop to enhance the loop stability. In addition, an ISHARE signal is generated from the primary phase and is shared with all other phases. The ISHARE signal helps balance the average phase current, mitigating the impact of the internal ramp variation and inductance tolerance. A typical two-phase configuration and the simplified control block diagrams are shown in Figure 5 and Figure 6.

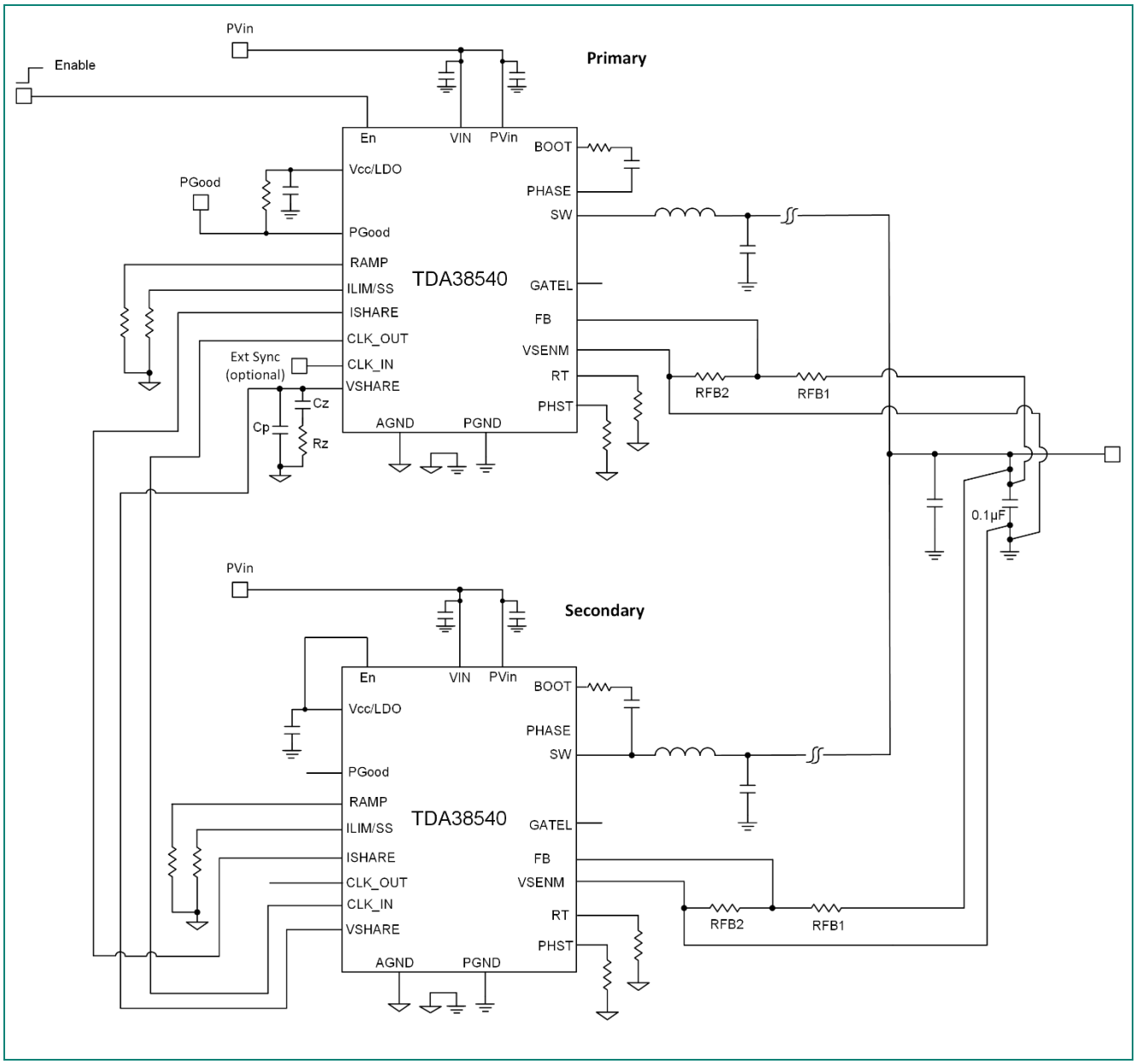


Figure 5 Typical application circuit for a two-phase configuration of TDA38540

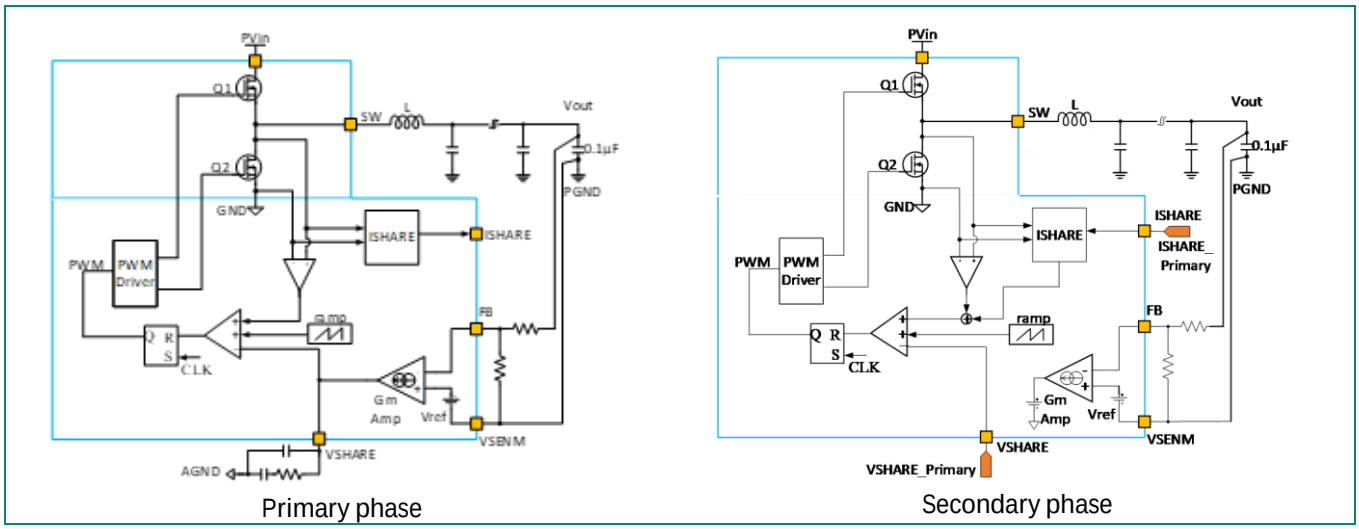


Figure 6 Control block diagram for TDA38540

3 Design example

Designing with TDA38540 can be as easy as a single-phase POL converter. When expanding the single-phase operation to multiphase, loop compensation can remain the same as long as the output capacitance is increased proportionally to the phase count. This is useful for a modular design. The detailed design procedure is explained with an example below.

The design specifications are: PV_{in} = 12 V ± 10%, V_{out} = 1 V, I_{out_total} = 80 A, f_{sw} = 800 kHz, V_{out} ripple voltage = ±1% of V_{out}, transient load response = ±4% of V_{out}, at load step = 40 A and load slew rate = 10 A/µs.

3.1 Configuring a two-phase operation

TDA38540 uses the PHST (phase shift) pin to set the phase shift. To configure a two-phase operation, the PHST pin of the primary phase can be left floating or be connected to a quiet ground (AGND or PGND) through a 120 kΩ resistor, as shown in Table 3. The PHST of the secondary phase should be connected to the ground through a 33 kΩ resistor, to obtain a 180° phase shift.

To synchronize each phase, the CLK_OUT pin of the primary phase must be connected to CLK_IN of the secondary phase, as shown in Figure 5. In addition, the VSHARE and ISHARE pin of each phase must be tied together respectively.

Table 3 Configuration table of PHST pin

PHST resistor (kΩ) ± 10%	Standalone/primary/secondary config	Phase shift (degrees)
0	Standalone mode	0
120	Primary phase in stackable mode	0
Floating		0
10	Secondary phases in stackable mode	90
18		120
33		180
56		240
82		270

3.2 Output LC filter design

Similar to a single-phase buck regulator design, the selection of inductance value is determined by the desired peak-to-peak inductor ripple current, usually in the range of 20% to 60% of the maximum output current per phase.

$$L = (1 - \frac{V_0}{PV_{in(\max)}}) \times \frac{V_0}{\Delta i_{Lpp} \times F_{sw}}$$

Equation 1 Inductance value calculation

In this example, design Δi_{Lpp} equal to 20% of the phase current, 40 A. The resulting inductance is around 150 nH.
Two design criteria are usually considered when selecting the output capacitance:
– Satisfy output ripple voltage requirement
– Meet output voltage overshoot and undershoot specifications during the load transient

For server and AI applications, the second criterion is usually more stringent and requires more output capacitance than the first criterion. In addition, due to the interleaved operation, the inductor ripple of each phase can be partially cancelled out when combined at the output, leading to a smaller output ripple voltage. Therefore, for simplicity, only the second criterion is considered here.

The following two formulas are usually used for single-phase POLs to calculate the minimum C_o (C_{omin}) required to meet output voltage overshoot and undershoot specifications during a load transient.

$$C_{omin_overshoot} > \frac{L \times \Delta I_o^2}{2 \times \Delta V_{oL} \times V_{out}}$$

$$C_{omin_undershoot} > \Delta I_o \times \frac{(1-D)}{\Delta V_{oL} \times f_{sw}} + \frac{\Delta I_o^2 \times L}{2 \times \Delta V_{oL} \times (V_{in} - V_{out})}$$

Equation 2 Minimum C_o calculation

where, ΔV_{oL} is the requirement of V_{out} overshoot and undershoot during a load transient, and ΔI_o is the transient load step.

In a stackable operation with multiple TDA38540 devices, the C_{omin} calculated in the above equations can be considered as the minimum output capacitance required per phase. ΔI_o is also the transient load step per phase, i.e., $\Delta I_{o_total}/n$. ΔI_{o_total} is the total transient load step at the output, and n is the phase count.

In this case, to meet the transient load requirement (i.e., ΔV_{oL}= 40 mV, ΔI_{o_total} = 40 A), each phase needs at least 750 µF and 641 µF to handle the overshoot and undershoot respectively. Then the total output capacitance should be higher than 1500 µF for a two-phase operation.

Please note that the calculations do not consider the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency. Extra capacitance should be considered in the design, which is usually quantified through simulation or bench tests.

3.3 Voltage loop design

With peak current-mode control, the LC double pole is separated by the inner current loop, resulting in a low-frequency pole and a high-frequency pole. Therefore, a type II compensator, as shown in Figure 5, can be used for the output voltage loop. Refer to the TDA38540 datasheet for the design details.

3.4 Selection of internal ramp compensation

TDA38540 implements a proprietary internal ramp, which emulates the inductor ripple current with additional ramp compensation for loop stability. To provide flexibility to adjust the current loop response, TDA38540 implements eight selectable internal ramp compensation gains, Kramp, which can be selected by connecting a resistor from RAMP pin to AGND, as shown in Table 4.

Table 4 Configuration table for RAMP pin

RAMP resistor (kΩ) ±10%	Kramp
0	20 x 10^{-3}
10	40 x 10^{-3}
18	60 x 10^{-3}
33	80 x 10^{-3}

56	100 x 10^{-3}
82	130 x 10^{-3}
120	160 x 10^{-3}
Floating	200 x 10^{-3}

To ensure the inner current loop stability, Kramp is recommended to satisfy the following criterion:

$$K_{ramp} \geq \frac{10^{-2} \times (2 - D)}{2 f_{sw} L} = \frac{10^{-2} \times \left(2 - \frac{1}{12}\right)}{2 \times 800k \times 150n} = 80 \times 10^{-3}$$

Equation 3 Kramp calculation

Higher Kramp can help improve noise immunity and switching node jitter, but reduces the bandwidth of the inner current loop.

A two-phase evaluation board, EVAL_TDA38540_1Vout_2P, has been developed to demonstrate the performance [3]. As can be seen in Figure 7, current sharing performs very well during both steady-state operation and the transient loads.

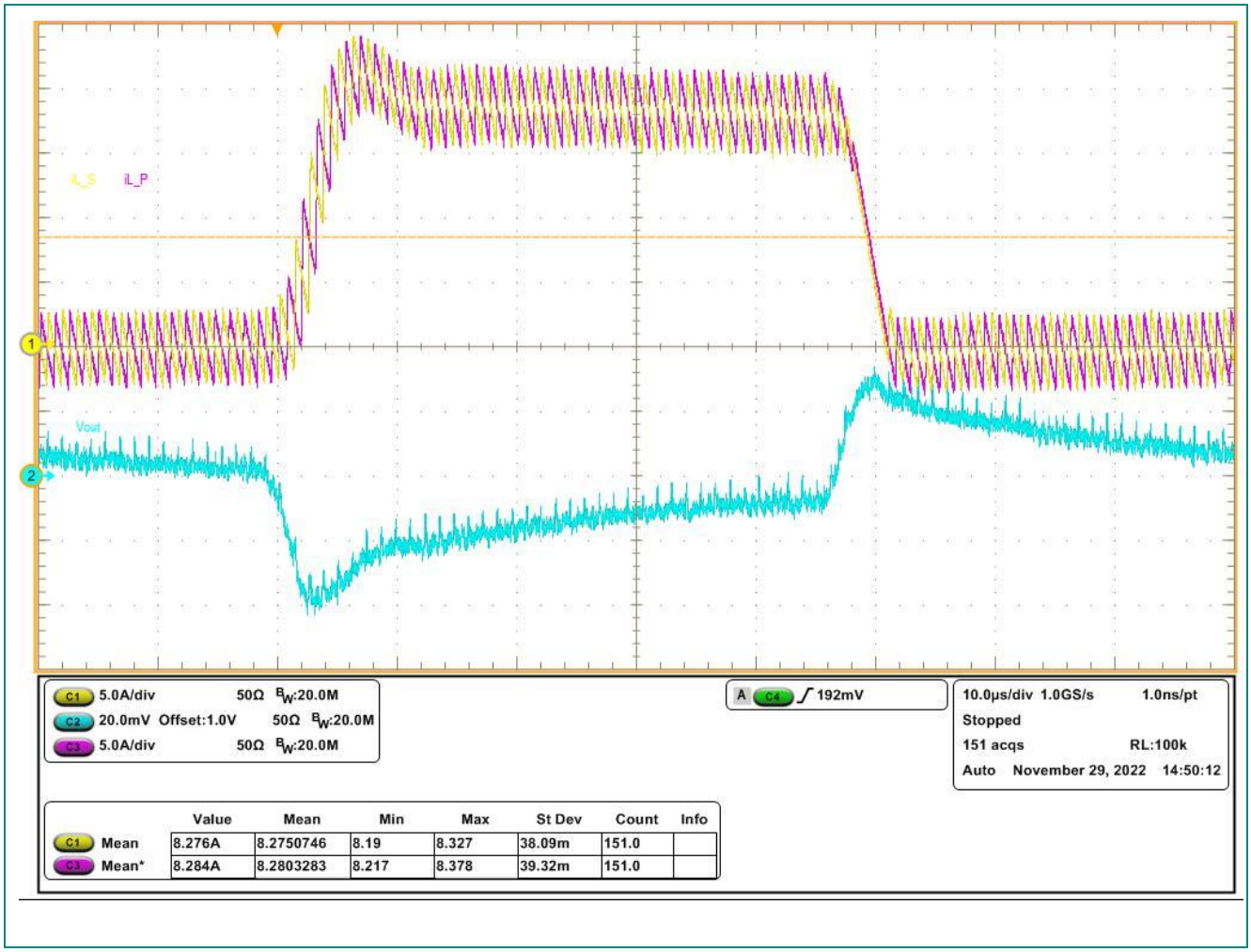


Figure 7 Transient response with 40 A step-load current at 10 A/µs slew rate: I_{out} = 0 A to 40 A, f_{sw} = 800 kHz, overshoot = 30 mV, and undershoot = 40 mV. (Ch1: iL_s, Ch3: iL_p, Ch2: V_{out})

3.5 Fault protections

TDA38540 offers necessary fault protections to ensure system-level security in the event of fault conditions, as listed in Table 5. For most faults, when a fault is detected, ISHARE is actively pulled high by the faulty phase. All phases are then shut down and enter hiccup mode.

In hiccup mode, a new soft-start sequencing is initiated, after a 20 ms blanking time. If the faults are no longer detected, all phases resume the normal operation. Otherwise, TDA38540 stays off for another 20 ms and repeats the cycle until the cause of the fault is resolved. Hiccup mode is usually preferred for telecom applications. With this implementation, TDA38540 provides a clean shutdown and restart during fault events. In addition, PGOOD of primary phase is an indicator of power good for both primary and secondary phases.

Table 5 List of fault protections offered by the TDA38540

Fault protection	Response
Positive low-side overcurrent protection	Primary: Enter hiccup mode and auto recover Secondary: Pulse skipping
Output overvoltage protection	Q2 is turned on to discharge V_{out}. Enter hiccup mode and auto recover
Output under voltage protection (for primary only)	Enter hiccup mode and auto recover
Overtemperature protection	Enter hiccup mode and auto recover
Negative low-side overcurrent protection	Q2 is turned off for ~200 ns when NOCP is detected
VCC undervoltage lockout	Shut down and auto recover

4 Summary

With the increasing power demands of modern microprocessors, TDA38540 offers a robust yet flexible power solution with superior efficiency and thermal performance. It allows system engineers to easily expand a single-phase design to a multiphase solution with the same loop compensation and the repeated layout, simplifying the design efforts and the bill of materials. With programmability through pin-strapping and on-board protection features, TDA38540 provides a versatile, robust, and compact solution for telecom, server and storage applications.

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