WHITEPAPER

Infineon DFN2020 Small-Signal MOSFETs for Automotive Applications

AEC-Q101 qualification, 175°C rating, and side-wettable flanks for easy AOI

Abstract

To meet the demand for component miniaturization and increased power density, Infineon Technologies AG introduces a new family of automotive-qualified Small-Signal MOSFETs in the DFN2020 package. These n-channel and p-channel devices combine high electrical performance with a compact footprint, addressing the evolving requirements of modern automotive and industrial electronics where board space, thermal robustness, and reliability margins are increasingly critical. The new DFN2020 Small-Signal MOSFET family is planned for start of production (SOP) in Q4 2026, further expanding Infineon's automotive MOSFET portfolio.

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1 Introduction

The continuous electrification of vehicles, the proliferation of advanced driver assistance systems (ADAS), and the growth of zonal architectures are redefining expectations for discrete semiconductors. Small-Signal MOSFETs, once considered commodity components, are now required to operate in harsh environments, withstand elevated junction temperatures, and contribute to overall system efficiency and power density.

Infineon's new DFN2020-based portfolio is automotive-grade and qualified for operation in applications where junction temperatures reach up to 175°C. This extended temperature capability is particularly relevant in under-hood applications, battery management systems, and high-density control units where ambient temperatures are rising due to increased functional integration.

Operating reliably at 175°C not only provides additional design headroom but also improves lifetime robustness by reducing thermal stress under nominal operating conditions. The DFN2020 package (see Figure 1) features side-wettable flanks, enabling straightforward automated optical inspection (AOI). In safety relevant automotive electronics, inspecting solder joints is mandatory, and side-wettable flanks allow clear optical verification of solder fillets even in leadless packages. This simplifies manufacturing processes and supports compliance with stringent automotive quality standards.

Efficiency improvements are driven by reduced parasitic resistances and inductances inherent to the leadless dual flat no lead (DFN) structure. The shorter current paths and the direct die-to-leadframe connection contribute to low package resistance and reduced switching losses. As a result, designers benefit from improved conduction performance, lower voltage drops, and enhanced switching behavior, particularly in high frequency applications.

The compact 2.0 mm × 2.0 mm form factor enables significant space savings compared to legacy packages such as SOT-223 and SOT-89. In applications where dozens of discrete MOSFETs are deployed — such as load switches, level shifters, motor drivers, or LED control circuits — the cumulative board space reduction is substantial. This directly contributes to higher functional density and reduced PCB cost.

Thermally, despite its small size, the DFN2020 offers strong performance thanks to its exposed pad concept and efficient thermal path to the PCB. When mounted on appropriately designed copper areas with thermal vias, the package can dissipate considerable power relative to its footprint. This makes it suitable not only for logic-level switching but also for moderate power tasks traditionally served by larger packages.

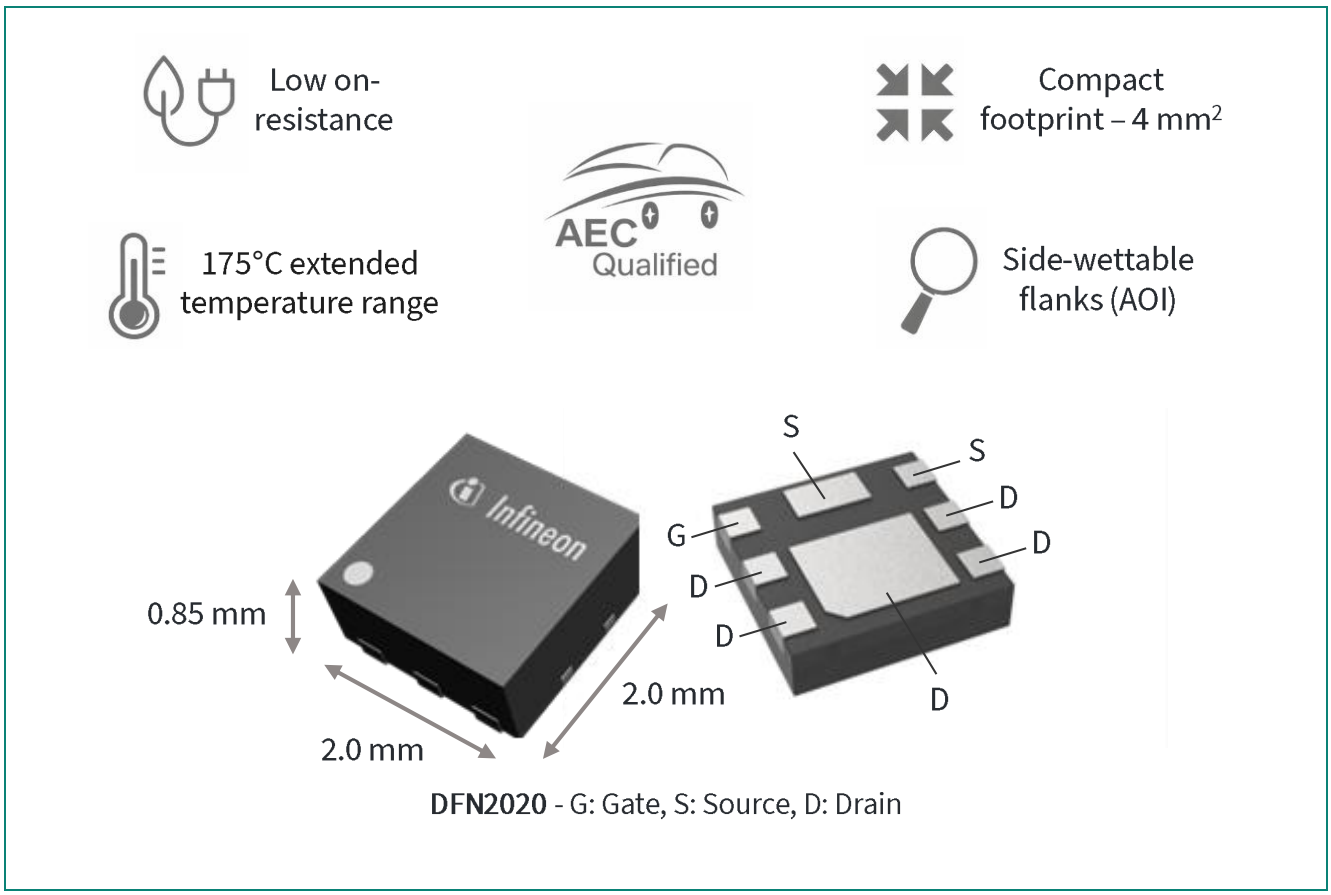

Figure 1 Key features of Infineon's DFN2020 package for high-density automotive designs

2 Infineon DFN2020 Small-Signal MOSFET portfolio

Infineon's DFN2020 portfolio comprises both n-channel and p-channel Small-Signal MOSFETs, enabling flexible use in high-side and low-side configurations. The devices are optimized for low $R_{DS(on)}$ at logic-level/super logic-level gate voltages, making them compatible with modern microcontrollers (MCUs) and low voltage control ICs commonly used in automotive electronics. A complete overview of the part numbers and key electrical parameters is summarized in Table 1, providing a clear guide for system-level selection.

The n-channel variants target low-side switching and general-purpose load control. Their low on-resistance reduces conduction losses, while minimized gate charge supports efficient high-frequency switching [1]. The p-channel devices complement the portfolio for high-side switching without the need for complex gate driver circuitry, simplifying system design in automotive domains.

In addition to conventional/auxiliary functions, the portfolio is also well suited for core DC-DC voltage regulators powering high-performance automotive MCUs such as the Infineon AURIX™ family. In these applications, fast load transients and steep current steps demand responsive power stages. The DFN2020 MOSFETs combine low $R_{DS(on)}$ with high switching speed, enabling efficient synchronous Buck operation [2] while maintaining stable output voltages under dynamic conditions.

All devices are developed under automotive quality processes, including AEC-Q101 qualification [3]. This ensures robustness against temperature cycling, humidity, mechanical stress, and electrical overstress conditions typical in vehicle environments.

The 175°C rating further distinguishes this portfolio from standard 150°C devices, offering additional safety margins for thermal excursions and extended lifetime reliability under demanding mission profiles.

By combining optimized electrical performance, compact footprint, and high-temperature capability, the DFN2020 portfolio provides a technically focused solution for discrete automotive power stages. It enables designers to increase functional density without compromising reliability, while maintaining the flexibility required for evolving zonal and domain-based vehicle architectures.

The DFN2020 Small-Signal MOSFET portfolio is scheduled for SOP in Q4 2026, adding a new automotive-qualified package option to Infineon's Small-Signal MOSFET portfolio.

Table 1 Infineon DFN2020 Small-Signal portfolio: Key electrical ratings and parameters

Part Number	Polarity	$V_{(BR)DSS}$	$R_{DS(on)_max}$ at 10 V	$R_{DS(on)_max}$ at 4.5 V	$R_{DS(on)_max}$ at 2.5 V	I_{D_max}	Package
ISK165N02KMA*	N	20 V	–	16.5 mΩ	27 mΩ	26 A	DFN2020 (PG-VSON-6-6) 2.0 x 2.0 x 0.85 (mm)
ISK500N02KMA*			–	50 mΩ	80 mΩ	11.1 A	
ISK170N03LMA**		30 V	17 mΩ	28 mΩ	–	26 A	
ISK500N03LMA**			50 mΩ	85 mΩ	–	11 A	
ISK400P02KMA*	P	-20 V	–	40 mΩ	90 mΩ	-22 A	
ISK12DP02KMA*			–	120 mΩ	250 mΩ	-8.5 A	

*Super-logic level **Logic-level

3 Package technology and design considerations

DFN2020 is a leadless package that eliminates the traditional gull-wing leads found in SOT-type packages. This structural difference directly impacts electrical, mechanical, and thermal behavior.

Electrically, the absence of long leads reduces parasitic inductance and resistance. Lower parasitics improve switching waveforms, reduce voltage overshoot, and minimize electromagnetic interference (EMI) [4]. In fast-switching applications, this supports more precise timing of switching events, enhancing circuit reliability.

Mechanically, the compact outline enhances vibration robustness, which is particularly important in automotive environments. The low profile contributes to improved mechanical stability and better resistance to board flex stress when properly mounted.

From a manufacturing perspective, side-wettable flanks represent a key innovation. Although the package is leadless, the refined leadframe geometry allows solder to climb up the sides, creating visible fillets. Automated optical inspection systems can therefore verify solder quality without requiring X-ray inspection for every joint. This improves production capacity and reduces inspection costs while maintaining high quality standards.

Thermally, the exposed pad and internal die attach configuration enable efficient heat transfer from the silicon to the PCB. Compared to legacy packages with limited thermal conduction paths, the DFN2020 allows designers to extract more performance from a smaller footprint. When combined with proper PCB thermal design, the effective thermal resistance can approach or outperform larger packages in certain operating conditions. A consolidated overview of these structural and system-level benefits is provided in Table 2.

Table 2 Engineering benefits of the DFN2020 leadless package

Aspect	Leadless DFN2020 advantage	System-level benefit
Electrical performance	No gull-wing leads, shorter current paths	Lower parasitic inductance and resistance, reduced overshoot, improved switching waveforms, lower EMI
Switching behavior	Compact current loop geometry	Cleaner transitions and improved signal integrity in high-speed applications
Mechanical robustness	Compact outline and low-profile structure	Enhanced vibration resistance and improved tolerance to board flex stress
Manufacturability	Side-wettable flanks enabling visible solder fillets	Reliable AOI inspection, higher production throughput, reduced reliance on X-ray
Thermal performance	Exposed pad with refined die attach	Efficient heat transfer to PCB, improved power dissipation in small footprint
Power density	Small 2 mm × 2 mm footprint	Higher functional integration and reduced PCB area

4 Comparison with legacy packages

Traditional Small-Signal and medium-power MOSFETs in packages such as SOT-223 and SOT-89 have served the industry reliably for decades. However, these packages occupy significantly more board area and exhibit higher parasitic elements due to their leaded construction.

To better understand the practical implications of this structural difference, it is useful to compare representative package options in terms of footprint size and occupied PCB area:

- **DFN2020:** Optimized for ultracompact layouts with a large bottom-side thermal/electrical pad and side-wettable flanks to allow AOI. The effective loop inductance is low because the current path is short and board-coupled
- **SOT-89:** A familiar option for higher dissipation than SOT-23, SOT-89 typically occupies a substantially larger footprint than DFN2020 and stands taller. Its leaded architecture introduces more package inductance than a leadless DFN and typically requires more board space for thermal relief, though it can still be a good fit when assembly familiarity is essential
- **SOT-223:** A much larger, leaded package with an exposed tab for heat, SOT-223 has historically been used when thermal headroom dominates. In many modern designs, however, a DFN2020 with good copper and via-in-pad design can approach or surpass the thermal performance of a SOT-223 solution of comparable silicon, while occupying only a small fraction of the area and delivering significantly lower parasitics

As illustrated in Figure 2, which compares the relative package dimensions and resulting PCB footprint area of DFN2020, SOT-89, and SOT-223, the size differences become immediately clear. DFN2020 dramatically reduces occupied board area compared to traditional leaded alternatives, enabling significantly higher power density in space-constrained designs.

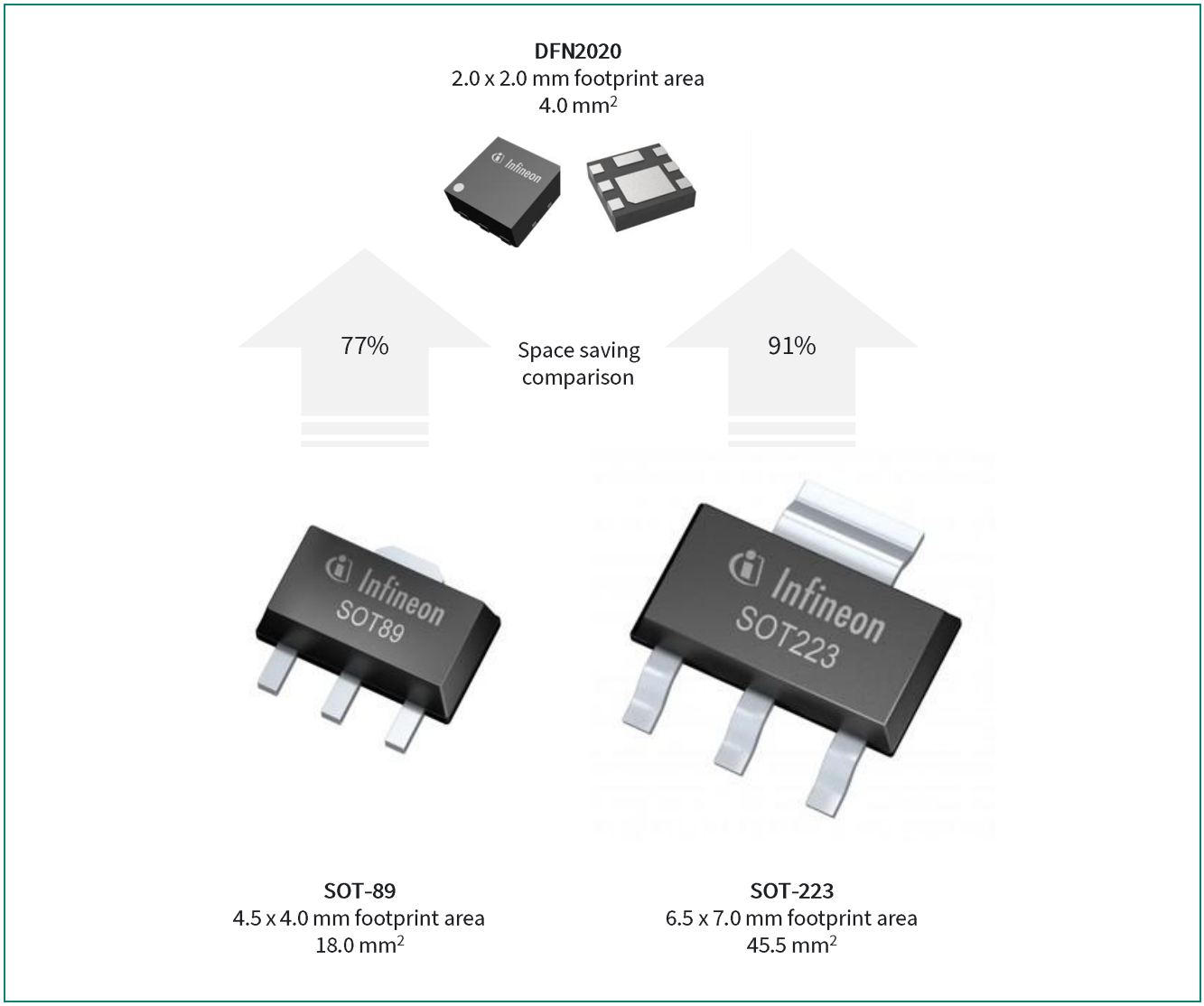

Figure 2 Physical package size comparison of DFN2020, SOT-89, and SOT-223 - relative PCB footprint area

5 Infineon DFN2020 Small-Signal MOSFETs for AURIX™ core voltage regulation

As automotive electronic architecture continues to evolve towards higher compute density, enhanced safety, and domain centralization, the power stage supporting the MCU becomes a defining element of overall system performance. With the introduction of AURIX™, core voltage regulation must address increasingly dynamic load conditions, tighter tolerances, and higher efficiency expectations.

At the center of this power architecture sits the synchronous Buck converter, where Infineon's DFN2020 Small-Signal MOSFETs provide an effective solution. As shown in Figure 3, the same Buck architecture principle applies to both AURIX™ TC4x and AURIX™ TC3x platforms, with performance scaling driven primarily by MOSFET selection and load profile.

5.1 Enabling high-performance core regulation

The AURIX™ TC4x family integrates high-performance multi-core processing, advanced safety concepts, hardware security modules, high-speed communication interfaces, and accelerator blocks. These capabilities translate into dynamic current profiles with fast load transients and stringent voltage stability requirements, typically around sub-1.2 V core rails. Within this application:

- Conduction/switching losses directly impact thermal headroom
- Switching behavior affects EMI robustness
- Package parasitics influence voltage overshoot and ringing

Every milliohm and every nanohenry matters. Infineon's DFN2020 MOSFET portfolio addresses these challenges by combining ultra-compact size with strong electrical and thermal performance.

5.2 DFN2020 benefits for AURIX™

The DFN2020 leadless package is engineered for high power density and low parasitic behavior. Its exposed drain pad enables efficient heat spreading into the PCB, while the leadless construction minimizes stray inductance compared to traditional leaded packages.

For AURIX™-based Buck converters, this translates into:

- Cleaner switching transitions
- Reduced overshoot and ringing
- Improved EMI behavior
- Higher efficiency at high switching frequencies
- Compact layout suitable for dense electronic control units (ECUs)

Additionally, the small footprint of the DFN2020 supports highly compact layouts, helping maximize routing flexibility and minimize trace inductance. Its low thermal resistance and short current paths reduce junction-to-board temperature rise, improving reliability under high switching frequencies and thermal cycling. In modern zonal and domain controllers, where PCB area is at a premium and thermal constraints are tight, DFN2020 becomes a strong enabler of optimized power design.

5.3 Portfolio selection for AURIX™ TC4x

For designs based on AURIX™ TC4x, low $R_{DS(on)}$ n- and p-channel DFN2020 MOSFETs can be used in synchronous Buck converters supplying the core rail. Table 3 provides an overview of representative DFN2020 MOSFETs for TC4x core voltage regulation.

Table 3 DFN2020 MOSFETs for AURIX™ TC4x core voltage regulation

Part Number	Polarity	$V_{(BR)DSS}$	$R_{DS(on)_max}$ at 10 V	$R_{DS(on)_max}$ at 4.5 V	$R_{DS(on)_max}$ at 2.5 V	I_{D_max}	Package
ISK165N02KMA*	N	20 V	–	16.5 mΩ	27 mΩ	26 A	DFN2020 (PG-VSON-6-6) 2.0 x 2.0 x 0.85 (mm)
ISK400P02KMA*	P	-20 V	–	40 mΩ	90 mΩ	-22 A	

*Super-logic level

N-channel devices are typically preferred in high-efficiency synchronous topologies due to their very low $R_{DS(on)}$, enabling reduced conduction losses and improved thermal margins under peak load conditions. P-channel variants offer design flexibility for high-side configurations where topology simplicity or driver considerations are prioritized. Together, these devices enable a compact, high-performance power stage for TC4x-based designs.

5.4 Portfolio solutions for AURIX™ TC3x

The AURIX™ TC3x family represents a highly established and widely deployed generation of AURIX™ MCUs. With proven performance across powertrain, chassis, and body applications, TC3x platforms continue to require reliable and efficient core voltage regulation. Representative devices and specifications are summarized in Table 4.

Table 4 DFN2020 MOSFETs for AURIX™ TC3x core voltage regulation

Part Number	Polarity	$V_{(BR)DSS}$	$R_{DS(on)_max}$ at 10 V	$R_{DS(on)_max}$ at 4.5 V	$R_{DS(on)_max}$ at 2.5 V	I_{D_max}	Package
ISK500N02KMA*	N	20 V	–	50 mΩ	80 mΩ	11.1 A	DFN2020 (PG-VSON-6-6) 2.0 x 2.0 x 0.85 (mm)
ISK12DP02KMA*	P	-20 V	–	120 mΩ	250 mΩ	-8.5 A	

*Super-logic level

DFN2020 MOSFETs are also applicable to these systems, supporting:

- Stable synchronous Buck architectures
- Compact PCB implementations
- Robust automotive qualified designs

While current and performance profiles may differ between TC3x and TC4x generations, the DFN2020 package provides a consistent mechanical and electrical platform across both families. This allows design scalability and footprint harmonization within product portfolios.

TC3x remains a widely adopted series and can also take advantage of the DFN2020 package technology and recent Small-Signal MOSFET developments, enabling compact and reliable core voltage regulation solutions across a wide range of automotive applications.

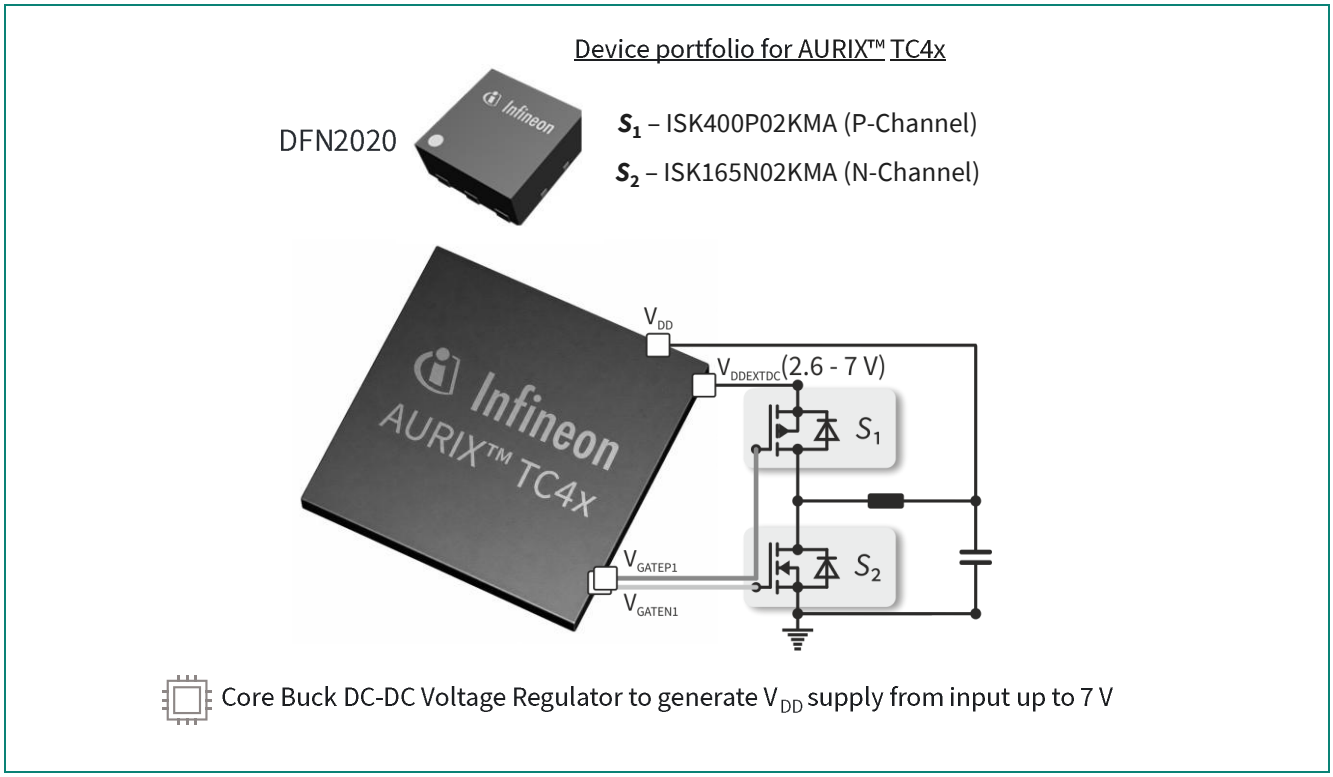

Figure 3 Generic synchronous Buck design for AURIX™ core voltage, applicable across TC4x and TC3x generations

5.5 System-level synergy

The combination of DFN2020 Small-Signal MOSFETs and AURIX™ MCUs delivers system-level advantages that go beyond discrete component specifications:

- Improved efficiency under dynamic load conditions
- Reduced thermal stress in compact enclosures
- Enhanced power integrity for safety-critical functions
- Lower EMI through minimized parasitic inductance
- Support for higher switching frequencies and smaller magnetics

This synergy is particularly relevant in architectures where compute, communication, and safety functions converge within increasingly compact ECUs.

Whether supporting the high dynamic demands of TC4x or the established performance envelope of TC3x, Infineon's DFN2020 Small-Signal MOSFETs provide a compact and efficient solution for AURIX™ core voltage regulation.

6 Conclusion

The ongoing evolution of automotive electronics, driven by electrification, zonal architecture, ADAS integration, and increasing compute-density, is redefining the expectations placed on discrete power semiconductors. Small-Signal MOSFETs are no longer simple commodity components, they are critical enablers of efficiency, robustness, and power integrity in safety-relevant systems.

Infineon's DFN2020 Small-Signal MOSFET portfolio directly addresses these demands by combining a compact 2 mm × 2 mm footprint with strong electrical performance, low parasitic behavior, and efficient thermal capability. The leadless architecture with exposed pads and side-wettable flanks supports both improved switching characteristics and manufacturing excellence through reliable AOI inspection. With AEC-Q101 qualification and a 175°C junction-temperature rating, the portfolio provides the thermal headroom and reliability margins required for modern automotive mission profiles.

When applied to synchronous Buck converters supplying AURIX™ core rails within the broader AURIX™ ecosystem, the benefits become particularly tangible. Low $R_{DS(on)}$, reduced package inductance, and efficient heat transfer contribute to higher efficiency, cleaner switching transitions, improved EMI behavior, and enhanced thermal stability under dynamic load conditions. The DFN2020 platform enables scalable solutions across both TC4x and TC3x generations, supporting footprint harmonization and design reuse within ECU portfolios.

By uniting a compact form factor, high-temperature capability, and automotive-qualified robustness, Infineon's DFN2020 Small-Signal MOSFETs provide a future-ready foundation for high-density power design. They empower system designers to increase functional integration, optimize PCB utilization, and maintain stringent reliability standards — all while meeting the growing performance expectations of next-generation automotive architectures.

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