PCB Layout Rules
- XDP™ digital power XDPS2221E

Dr. Jing Hu

1 System design
- Board development

- Design and review
  - Schematic draft
    - Component selection
      - Voltage and current rating
      - Package, dimension of bulk devices
  - PCB development
    - Board floor plan and component placement
      - Controller IC outside of any loops with pulse current
      - Bus capacitor position enabling short ground connections
      - Varistor close to input terminals and small loop area
      - Separation and proper distance of the input filter and others
      - Small signal components close to the IC, including the lower one of the bus voltage divider high-side resistors
    - Key signals and cautions
      - PFC: CS/ZCD, bus voltage sense
      - HFB: CS, FB, and ZCD
      - CS: Differential pair routing vs. short & width ground
      - FB: Differential pair routing and small loop
      - Proper distance to signals with high dv/dt or high di/dt
    - Grounding concept
      - Bus capacitor ground as the potential reference
      - Star-connection of all ground connections
      - Short and wide ground connections
      - Separate tracks for different stages: input, PFC and HFB
      - Using Kelvin grounding for driving signal if applicable
      - Short and wide ground connection of the Y-capacitor at both sides
    - High di/dt loops: Small area for power loops, gate driver
    - high dv/dt signals: Short trace and distance to other signals, no overlap of the half bridge highside driver circuitry and other signals
    - Thermal and EMC metal cover
      - Grounding: primary vs. secondary side (safety ad insulation, EMC and thermal distribution)
      - Recommendation: No overlap with the controller HV pin and its external resistors, and half-bridge switching node
- Board assembly
  - Polarity and terminals
  - Soldering temperature and solder paste
  - ESD protection measures

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Overview

- Introduction
- Switching noise coupling
- General layout rules to minimize the noise generation
- Counter measures at IC pins to improve system Electromagnetic Compatibility (EMC)
- Other considerations

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Introduction

- Switching mode power supply (SMPS) system employing
  - High-speed switching to minimize switching losses
  - Switching at non-zero voltage and/or current causing fast changing voltage (high dv/dt) and/or current (high di/dt)

- Switching noise in a SMPS system due to
  - Non-ideal device
    - Terminal inductance
    - Junction capacitance of switching devices
  - PCB trace impedance
  - Not optimal component placement, and
  - Poor PCB layout

- Focus of this document
  - PCB layout guidelines to
    - minimize the generated noise
    - improve system EMC

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Switching noise coupling

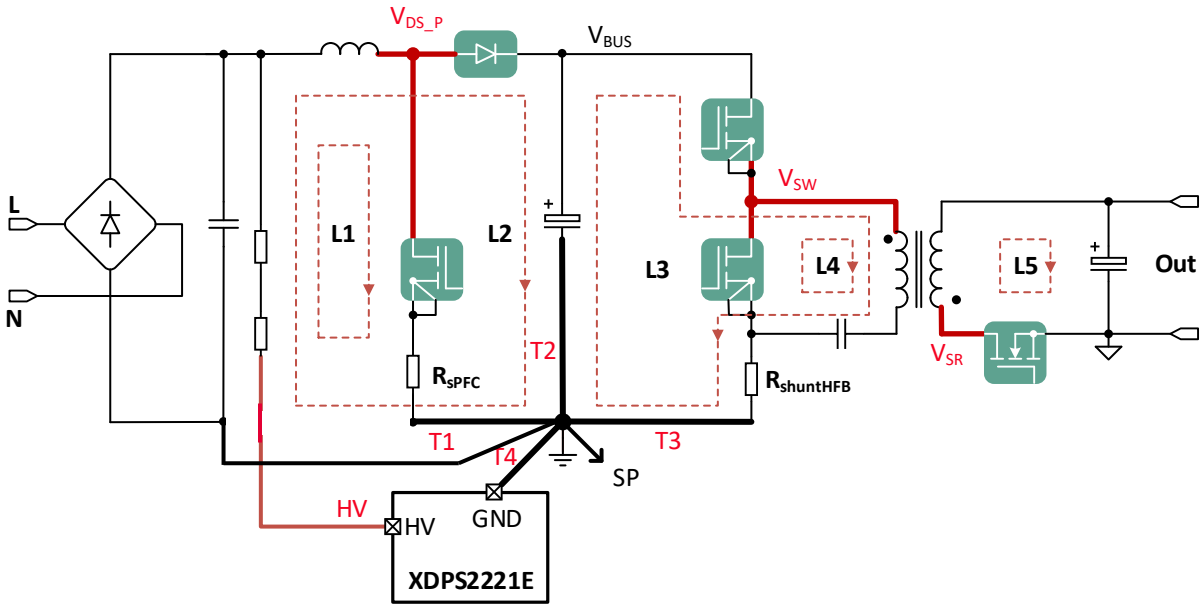
- Switching noise coupled to the sensitive controller pins via
  - Capacitive coupling
  - Inductive coupling
  - Resistive/inductive coupling , and
  - Magnetic leakage field
    - Grounding the magnetic cores
    - Flux band around the magnetic core air gap
  - Measurement setup

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Switching noise sources
- Capacitive coupling

- PCB traces/polygons with high dv/dt transient
- Coupled via the parasitic capacitance between
  - the respective PCB trace/polygon, and
  - PCB trace and signal pin
- Sources on board
  - V_{DS_P}: valley but non-zero voltage turn-on
  - V_{SW}: due to floating HS gate driver domain
  - V_{SR}: drain voltage transient
  - PFC choke: parasitic capacitance
  - HFB transformer: parasitic capacitance
- Observation
  - Voltage spike at the switching moment



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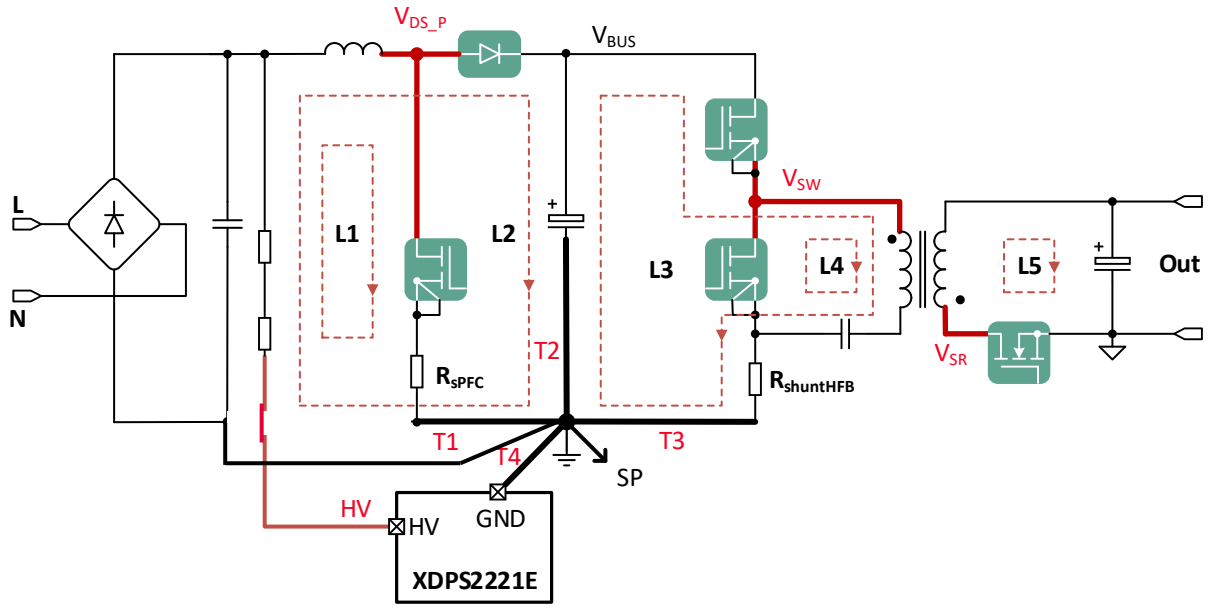
Switching noise sources
- Inductive coupling

› Loops with high di/dt

› Coupled to the signal pins via the inductance inside the current flowing loop and magnetic field

› At and after the switching transition
- Loop L1: PFC switch turn-on
- Loop L2: PFC switch turn-off
- Loop L3: HFB high-side (HS) switch turn-on
- Loop L4: HFB low-side (LS) switch turn-on
- Loop L5: SR switch on-time
- Loops of the gate driver circuit
- Loop of the VCC supply rectifier with pulse current

› Observation
- Voltage ringing up the switching moment



Traces with high dv/dt

Critical GND PCB tracks

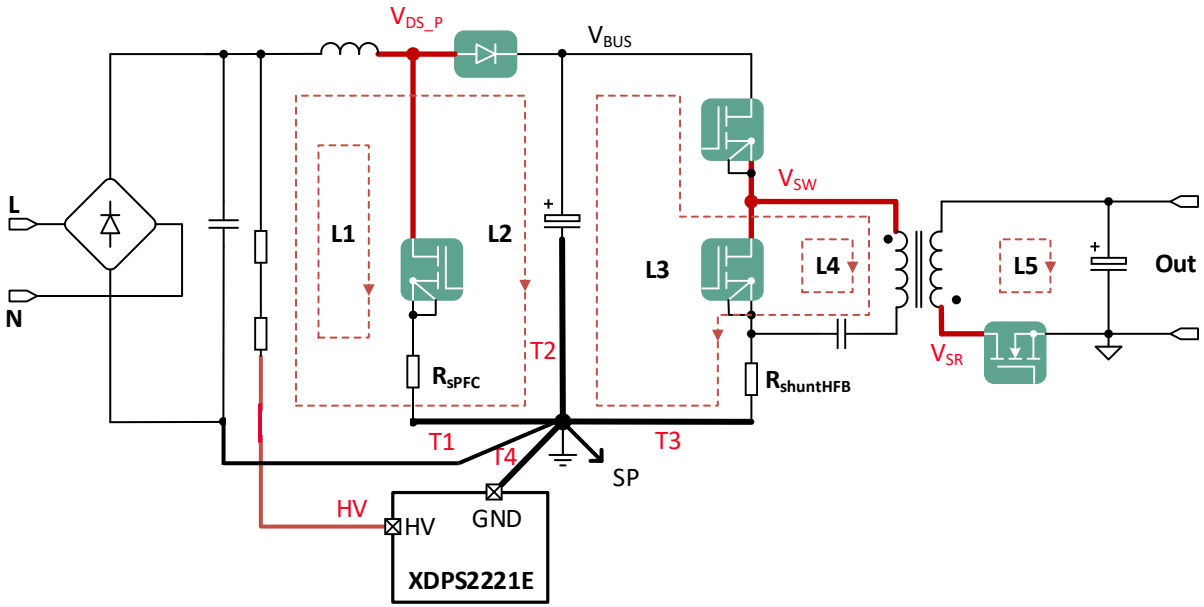
Loop with high di/dt

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Switching noise sources
- Resistive/inductive coupling

- PCB traces with pulse current
- Coupled to the signal pins via the PCB trace resistance and inductance
- Critical paths
  - To the ground star-connection from
    - Trace T1: PFC shunt resistor
    - Trace T2: bus capacitor
    - Trace T3: HFB shunt resistor
    - Trace T4: IC GND pin
- Observation
  - Ground bouncing or even signal level shifting



Traces with high dv/dt

Critical GND PCB tracks

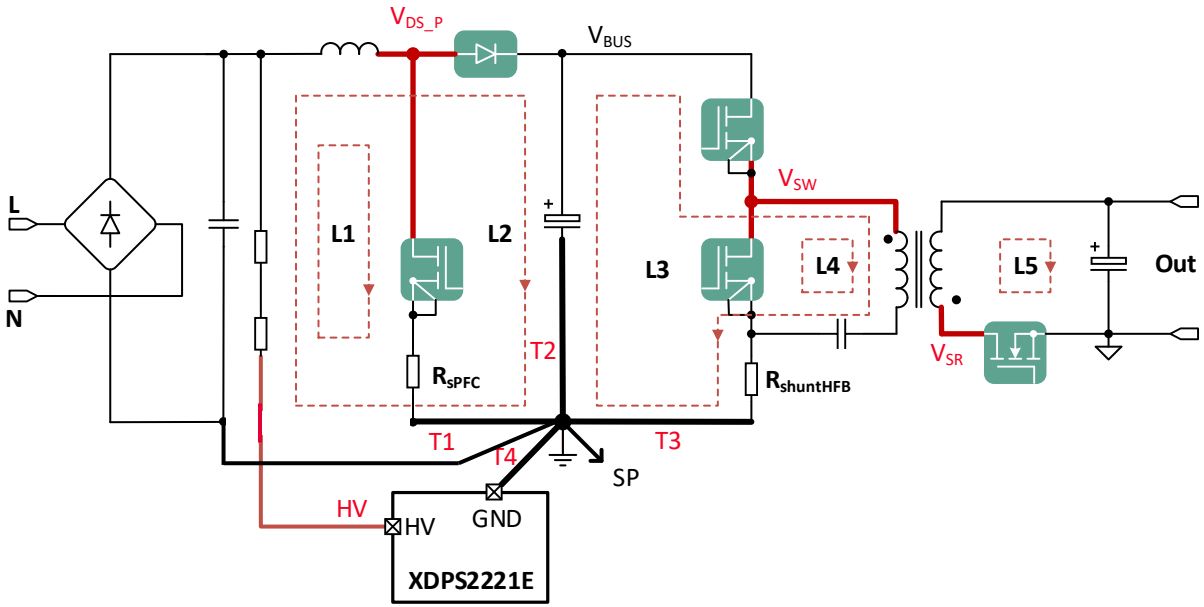
Loop with high di/dt

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General layout rules
- Traces / components with high dv/dt

- Short PCB trace for high dv/dt signals
- Proper distance between the PCB trace with high dv/dt and other PCB traces, especially that of small signal
- Disturbed PFC operation with overlapped HS driver domain and the IC ground: ➔ No overlapping of the HS driver domain and the IC ground, including the boost strap circuit
- Proper distance between the HS driver domain and other PCB components
- Grounding the PFC choke and HFB transformer core

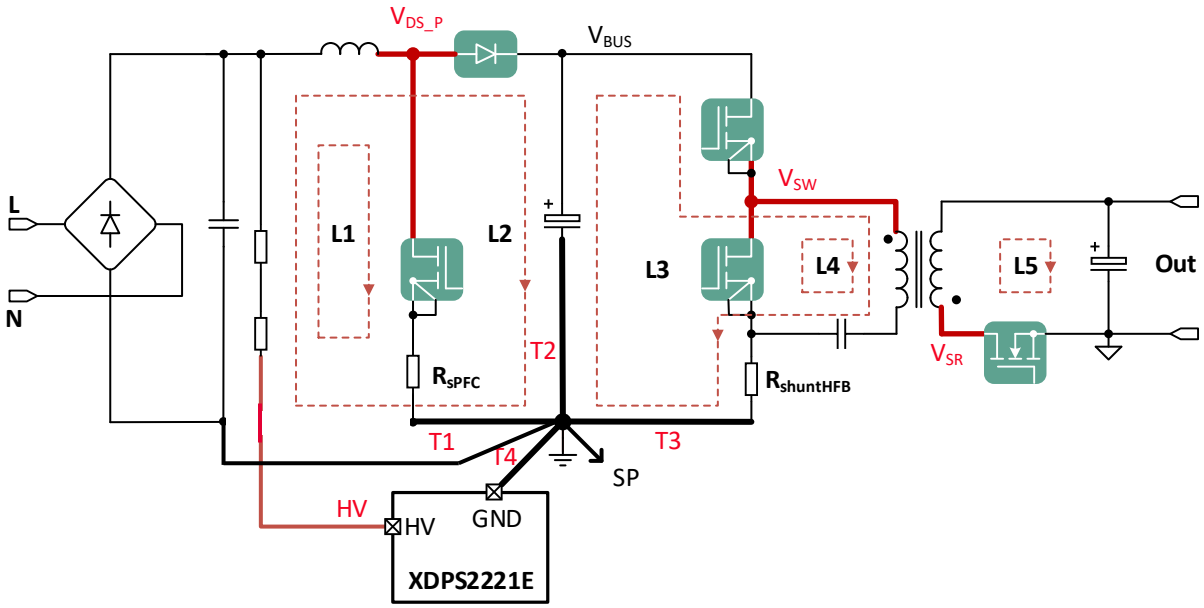


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General layout rules
- Loops with high di/dt

- Loop area with high di/dt as small as possible
  - Loops L1 to L5
  - Loops of the gate driver circuit, even low current level
  - Loop of the VCC supply, especially with charge pump
- Additional ceramic or film capacitors in parallel to the electrolytic capacitor, i.e.: bus, VCC and output capacitor, to
  - reduce the equivalent impedance of the capacitor, and
  - bypass the high frequent current
- Keep the film capacitor after the rectifier bridge close to the PFC
- IC and its small signal components NOT inside these current loops



Traces with high dv/dt

Critical GND PCB tracks

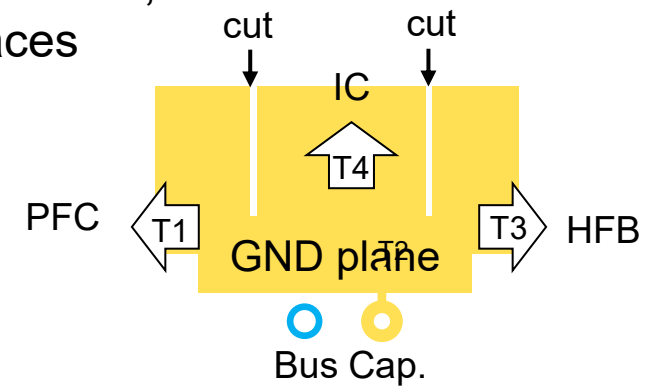
Loop with high di/dt

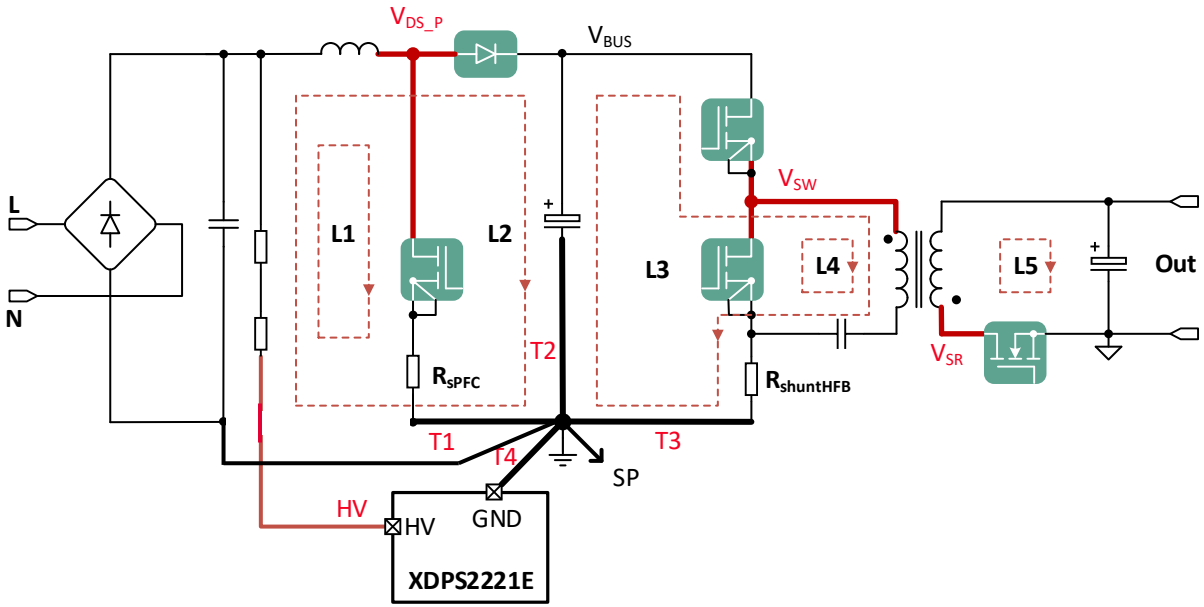
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General layout rules
- Resistive coupling/Grounding

- Star-connection for ground traces
  - Ground polygon with cuts, or
  - Separated PCB traces





- Short and thick traces for T1-T4 and VCC supply winding ground (SP)
- Small signal components around the IC
  - Close to the IC pin, and
  - Only connected to the IC ground
  - At lease one of the high side resistor of the PFCvs sensing close to IC
- VCC supply ground connected to bus ground directly

Traces with high dv/dt

Critical GND PCB tracks

Loop with high di/dt

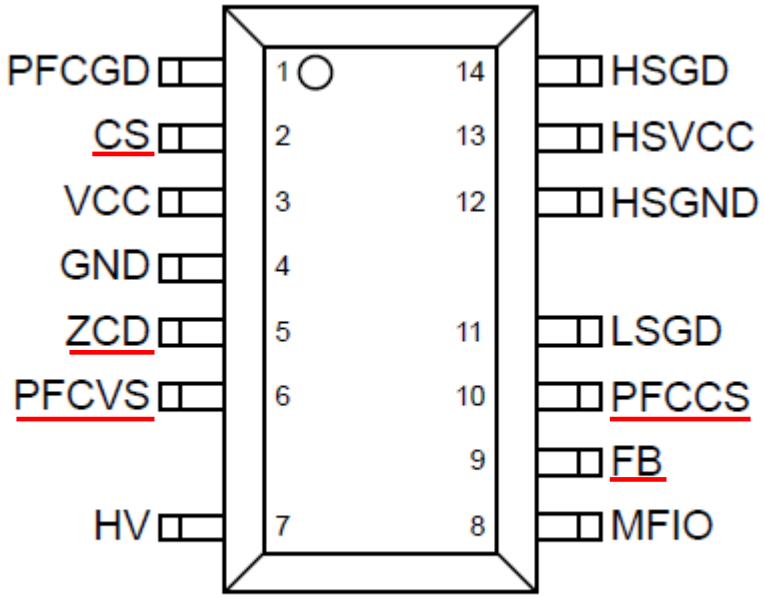
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Pins requiring attention

- PFCCS pin
  - PFC switch w/o current sensing
    - Combined function of the PFC ZCD and OCP
  - PFC switch with current sensing
    - PFC ZCD functionality, PFC OCP taken over by the switch
- PFCVS pin
  - Sensing the bus voltage for bus voltage regulation and bus OVP
- HFB CS pin
  - Sensing the HFB current during Q_{HS} on-time
  - For both regulation and OCP protection
- HFB ZCD pin
  - Utilized for
    - Output voltage level sensing during on-time of Q_{LS}
    - HFB valley detection
- HFB FB pin
  - Utilized for peak current control

XDPS2221E



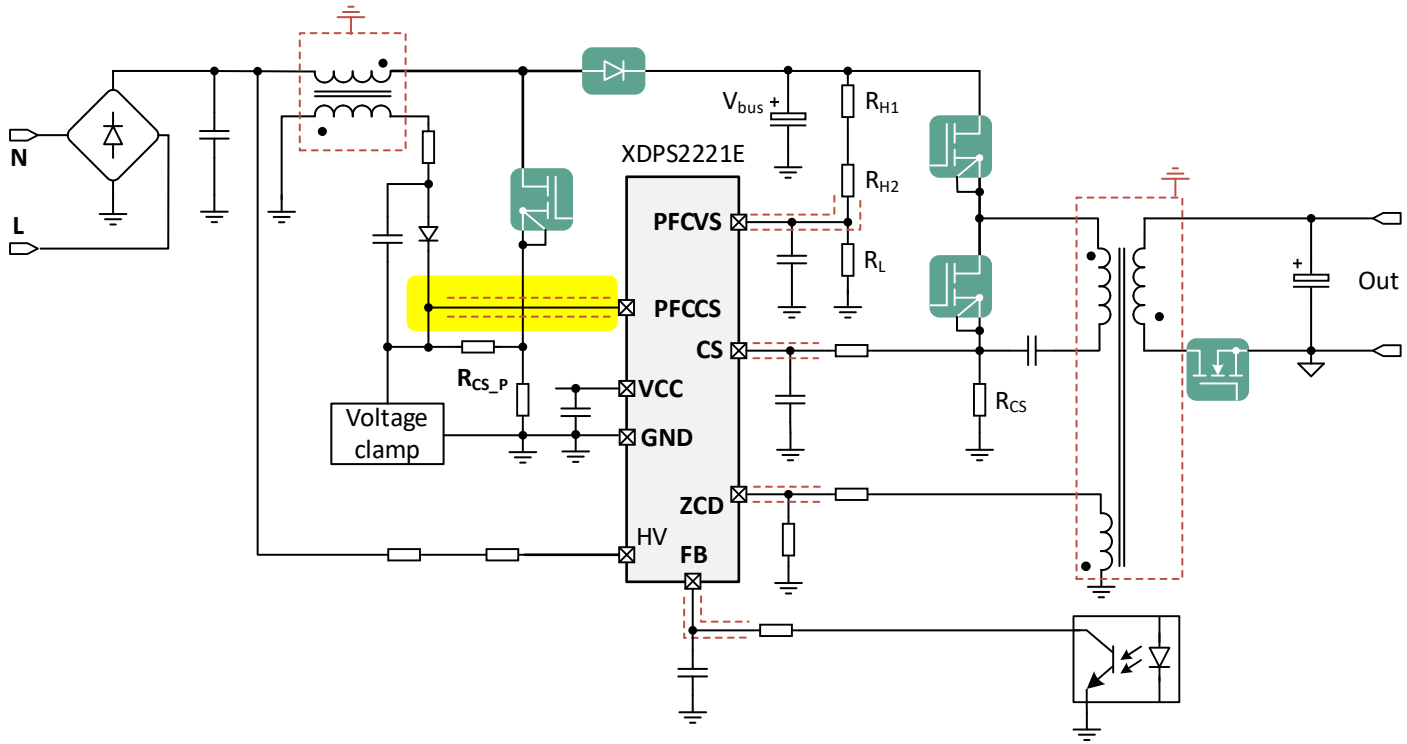
PG-DSO-14 (150mil)

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Pins requiring attention
- PFCCS pin

- Keep distance to noise sources with high dv/dt:
  - HB switching node, V_{DS} node, HV pin and PFC choke
- GND shielding around this signal PCB
- Not direct probing the pin
  - Probing directly the Vaux for ZCD information, or
  - PFC shunt resistor for the PFC current

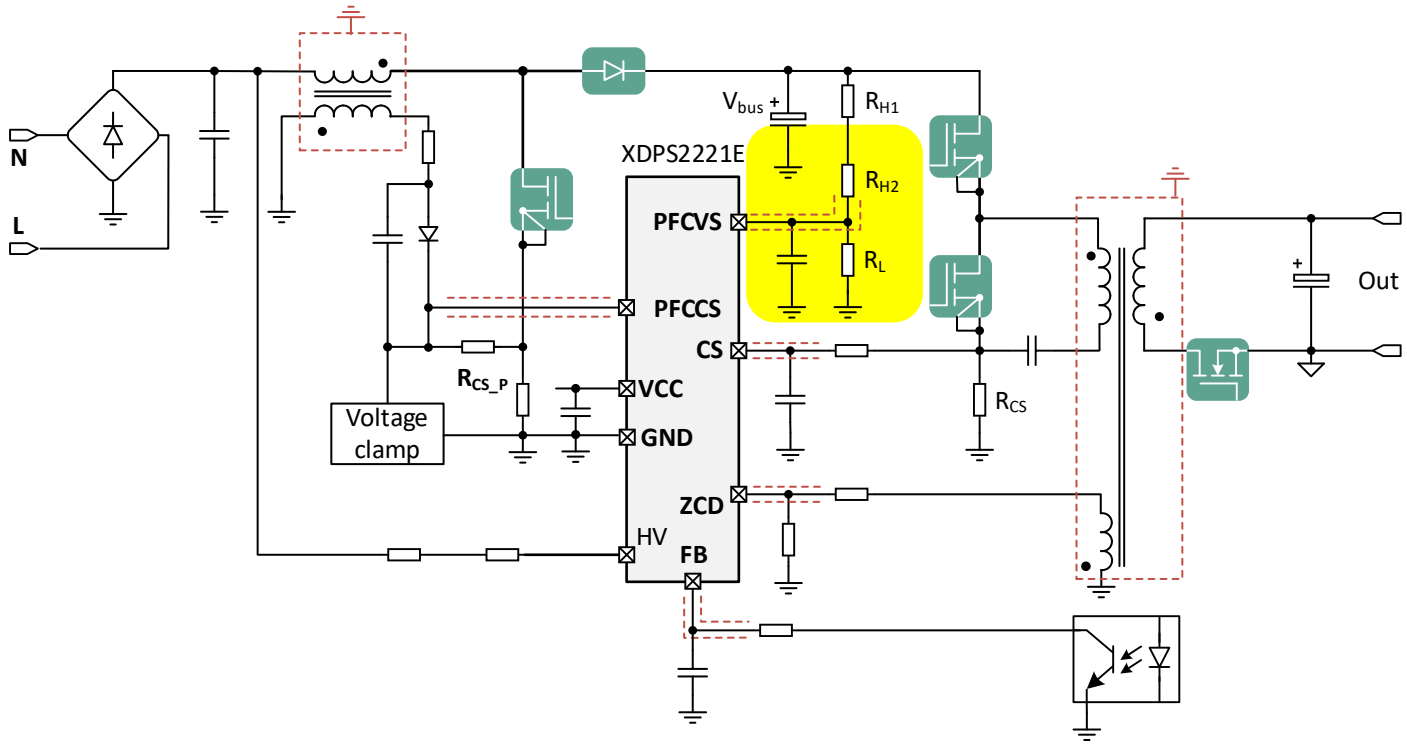


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Pins requiring attention
- PFCVS pin

- Keep distance to noise sources with high dv/dt:
  - HB switching node, V_{DS} node, HV pin and transformer cores
- GND shielding around this signal PCB
- At least one of the high side resistor close to the low side components and then to the IC
- RC filter with a corner frequency around 1/10 of the minimal switching frequency

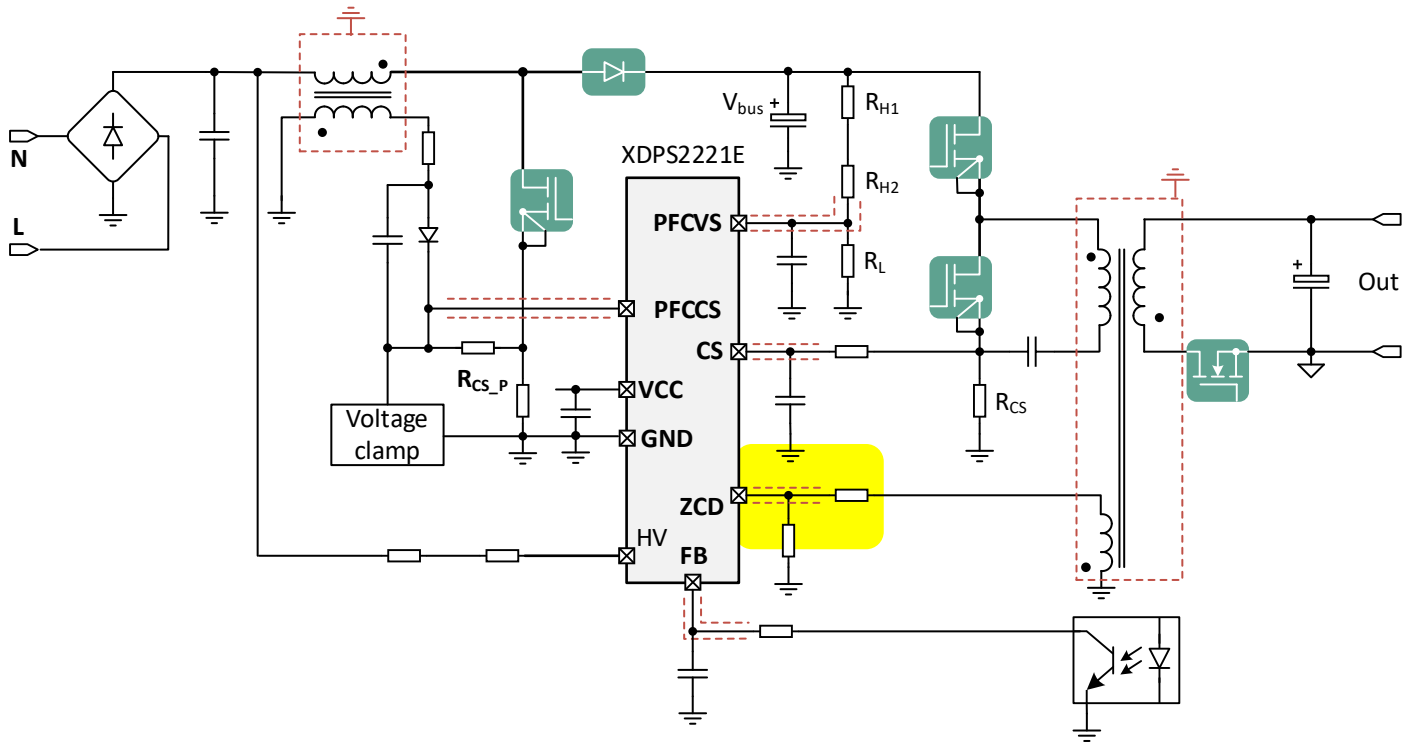


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Pins requiring attention
- ZCD pin

- Divider resistors close to the IC
- Short and shielded PCB trace
- No filter capacitor, or very low value of that, to avoid additional delay to the ZCD signal
- Probing directly the V_{aux} instead of the ZCD pin for ZCD information

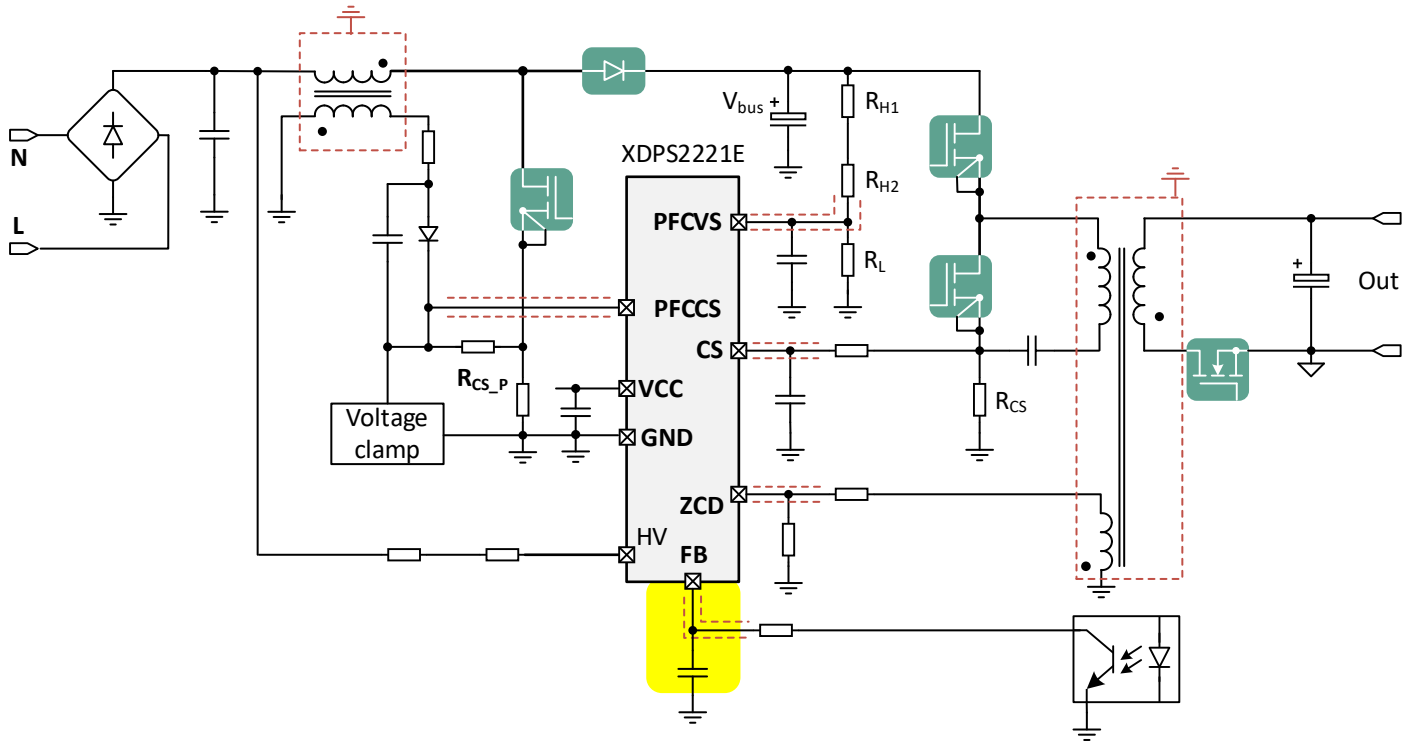


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Pins requiring attention
- FB pin

- Short PCB trace
- Keep distance to the noisy traces/components
- Shield the feedback trace with GND plane
- Using IC ground connection for the opto-coupler and filter elements
- A RC filter
  - with low time constant just to filter out the high frequency disturbance
  - RC filter components close to the pin

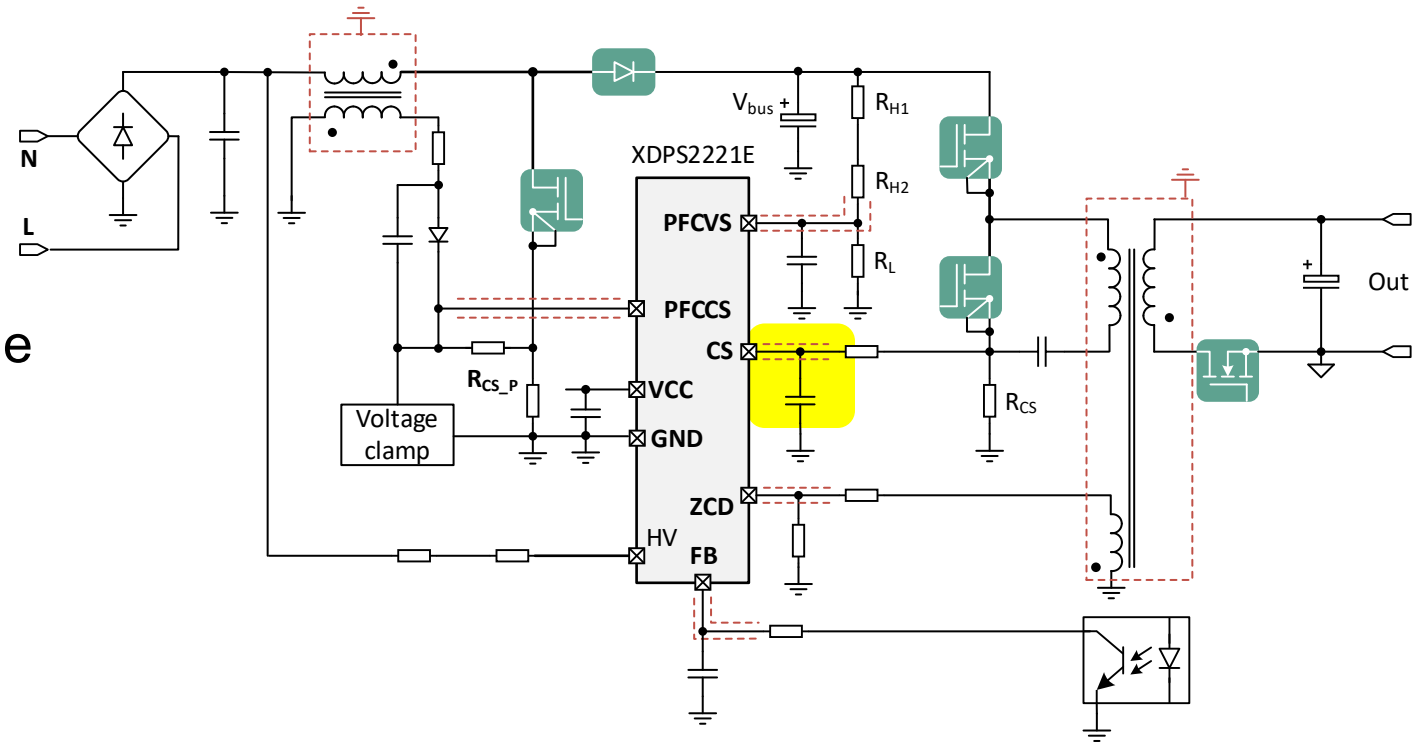


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Pins requiring attention
- CS pin

- Short PCB trace
- Proper distance to the noisy traces/components
- Shield the feedback trace with GND plane
- Using IC ground connection for the filter elements
- A RC filter
  - with low time constant just to filter out the high frequency disturbance
  - RC filter components close to the pin

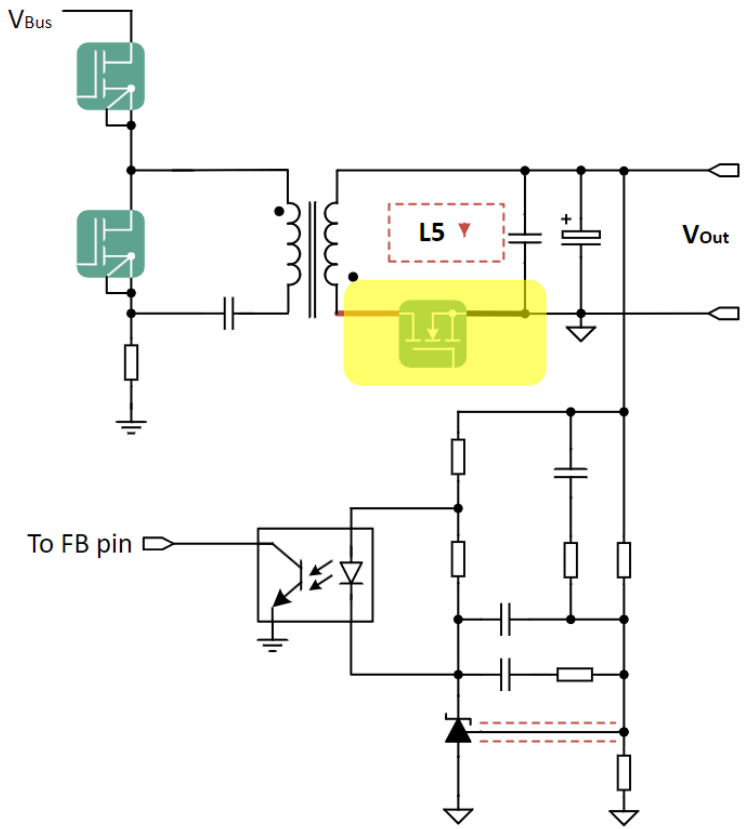


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Other consideration
- Synchronous rectification (SR)

- Short and thick PCB trace of the MOSFET drain and source connection
- Small area for the loop L5, i.e.: via a ceramic capacitor electrically in parallel to the output electrolytic capacitors
- SR controller close to the SR MOSFET and short PCB traces for the sensing paths
  - Big influence of the PCB trace inductance for the SR turn-off determination

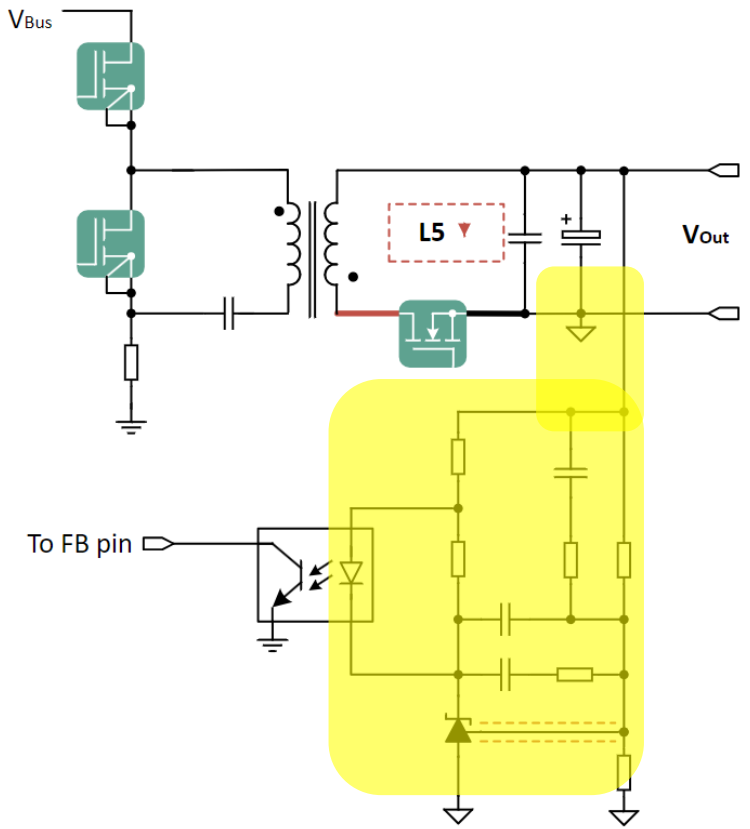


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Other consideration
- Secondary side control circuit

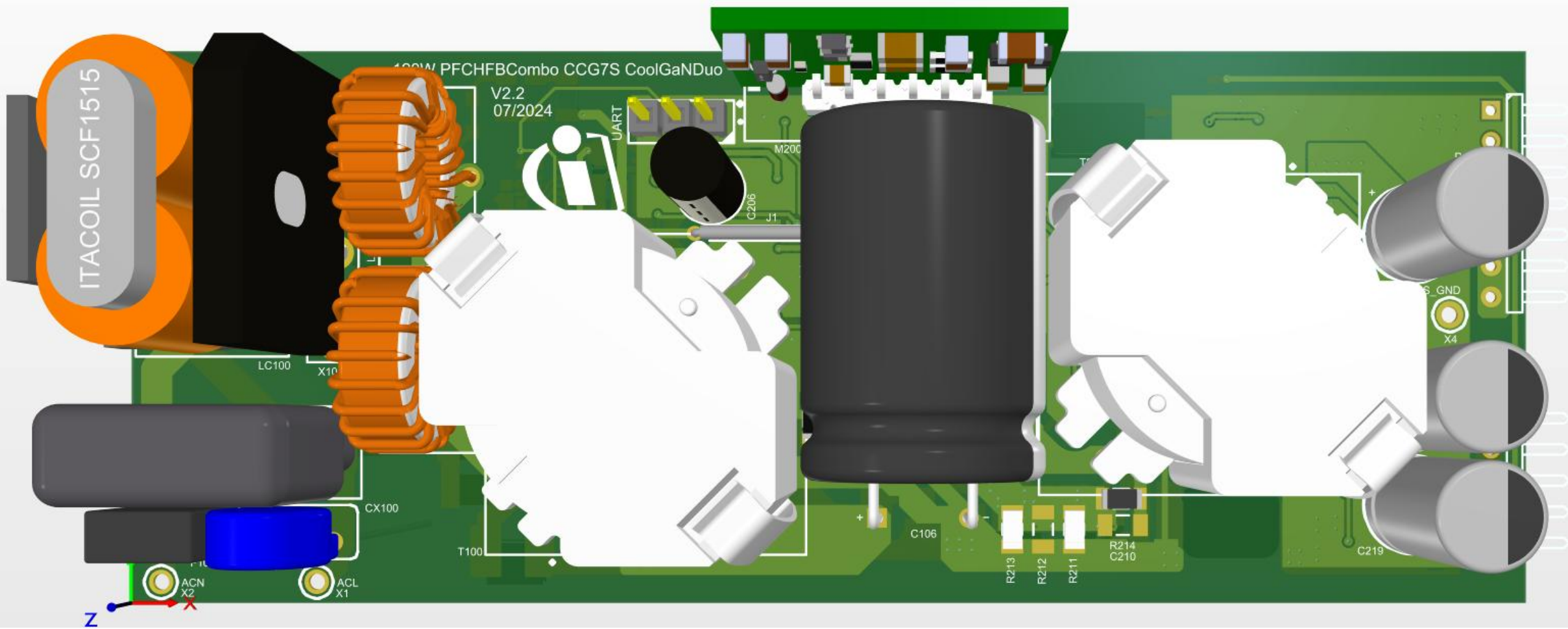
- Voltage reference IC with low reference current preferred to meet low standby power requirement
- Compact design of the entire secondary side regulator circuit recommended
- Keep distance of the entire secondary side regulator circuitry from the SR MOSFET drain and HFB transformer core
- Separated regulator ground polygon
  - For the entire to the secondary side regulator circuitry
  - Single line connection to the output electrolytic capacitor ground



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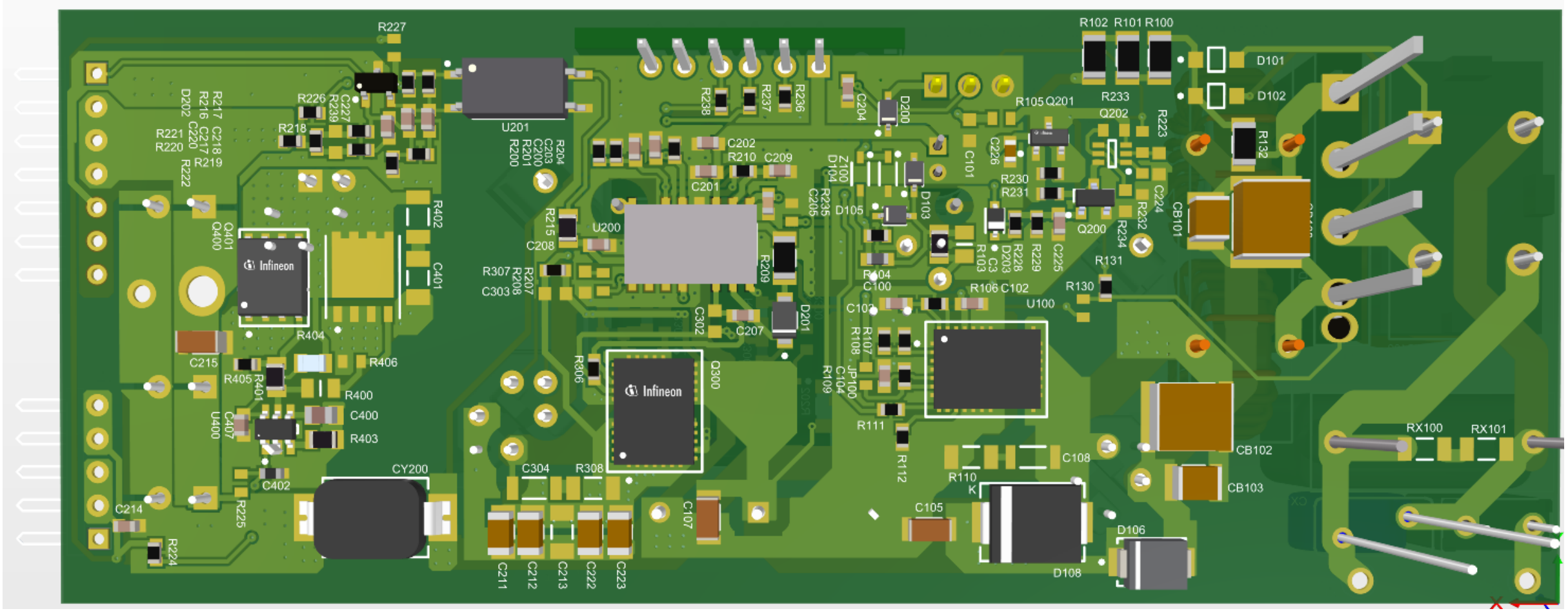
One design example
- 120 W board with connector for different evaluation purpose



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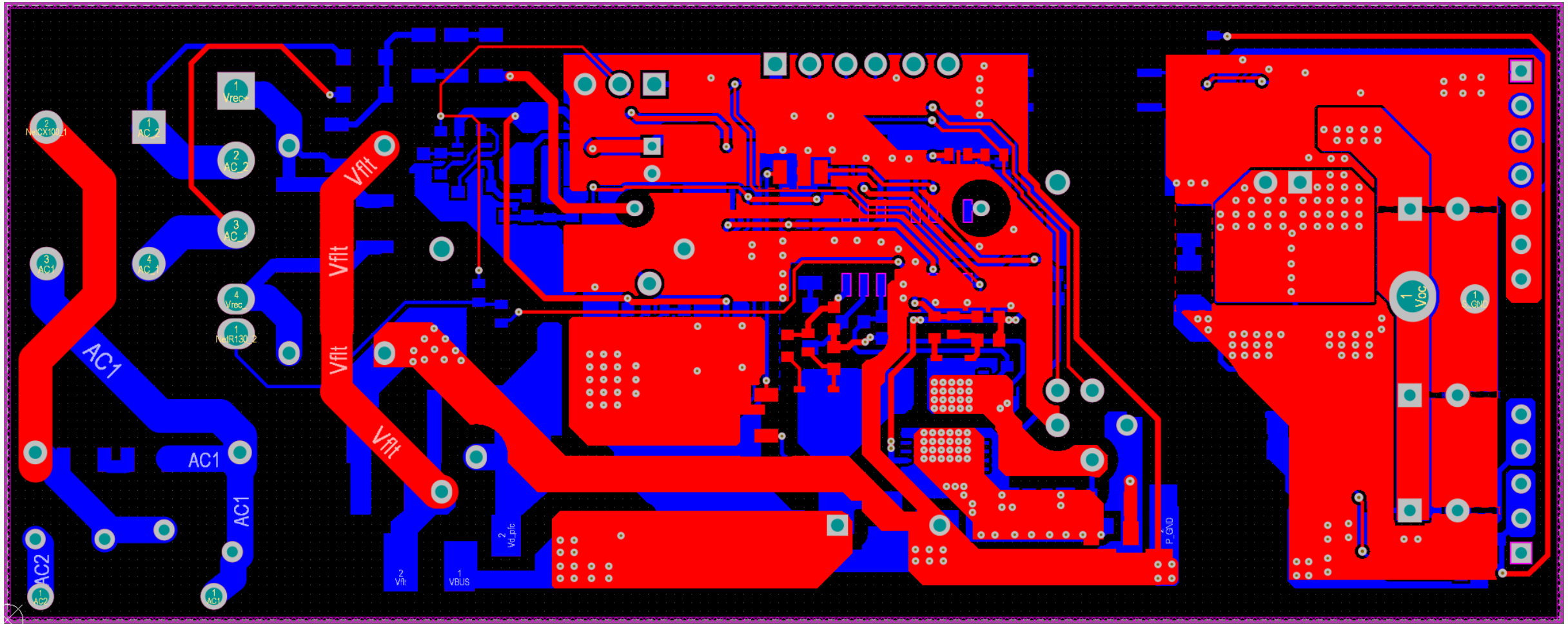
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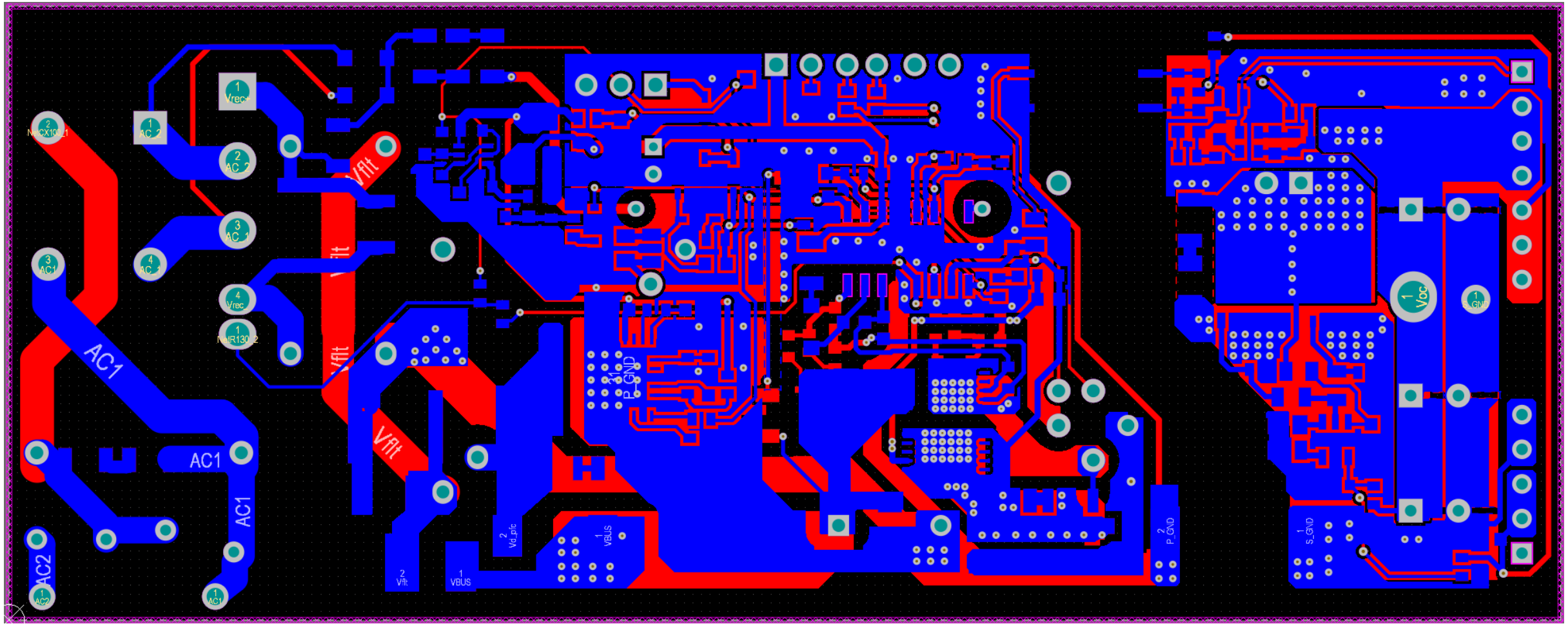
One design example
- 120 W board top



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One design example
- 120 W board bottom



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Change History

- V1.0.0
  - Minimum layout change
- V0.2.0
  - Apdated bridge rectifier ground connection, page 5 to 10
- V0.1.0
  - Initial release

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Important Safety Instructions and Legal Notes

The final setup needs to be tested according to all relevant normative requirements. This means that the following actions are mandatory, please also refer to the Documentation for further information:

1. Every combination of parameter sets/configurations needs to be fully evaluated by a technical expert. Make sure that the combination of parameters used matches your application's needs. It is the customer's responsibility to make sure that the chosen parameters meet all requirements, including safety-related requirements.
2. Before using a parameter set, make sure that the system - including any programming/ OTP burning hardware- is fully tested and working as expected.
3. Every parameter set is only valid for the dedicated evaluated hardware configuration, including PCB, Layout, used topology and all used electronic components (e.g. MOSFET, Transformer, ...)

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