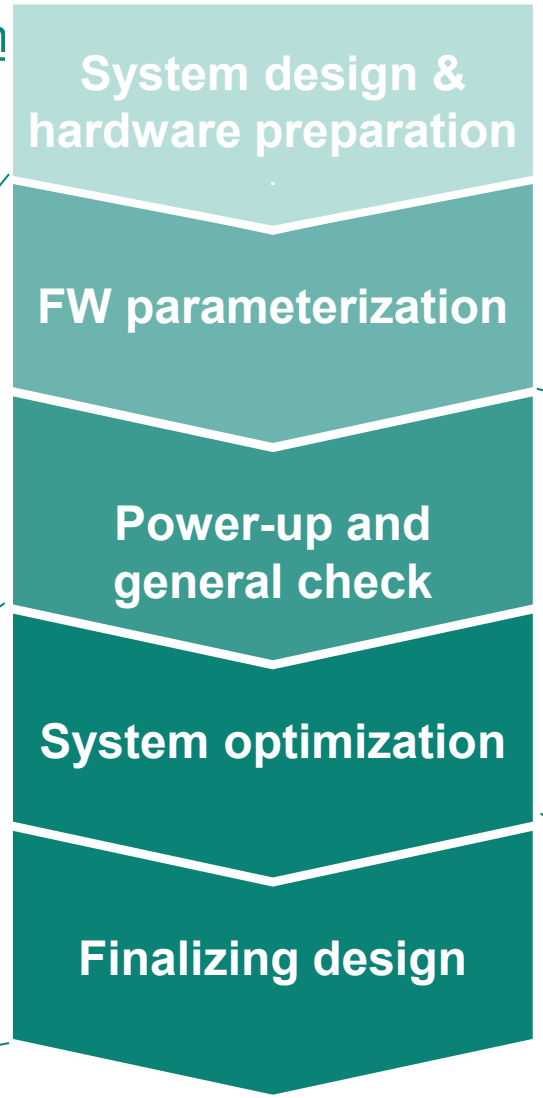


Hybrid Flyback Controller XDPS22-Series
- Design cookbook

Overview

1. System design & hardware preparation
   - Input
     - Application specific parameters
     - Design intention
   - Outcome as proposal
     - Hardware value
     - .csv parameters
   - Board design



2. FW parameterization
   - Interface board required
   - dpVision tool, .csv file and images required
   - FW parameter value update in dpVision
   - Download parameter value to IC

3. First power-up and general tests
   - First system cold power-up
   - General operation check

4. System optimization
   - Hardware update
   - Parameter finetune
     - To achieve desired performance and operating behavior
     - Individual protection settings

5. Finalizing the design
   - Fix hardware
   - Burn .csv parameters
   - Production release

[Owner: Dr. J. Hu Doc ID: Vers.: V1.0.0]

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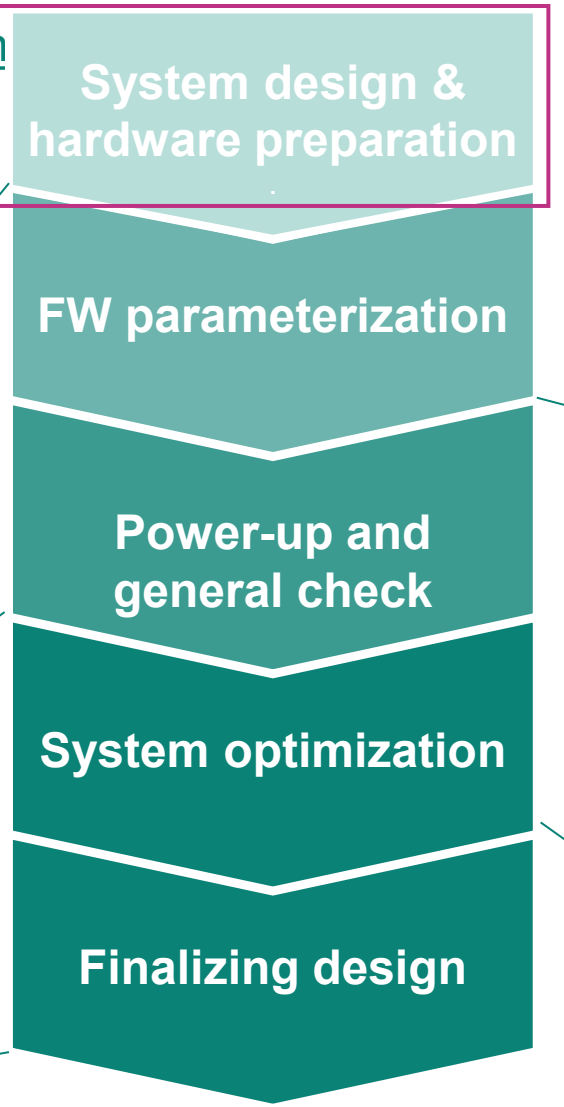

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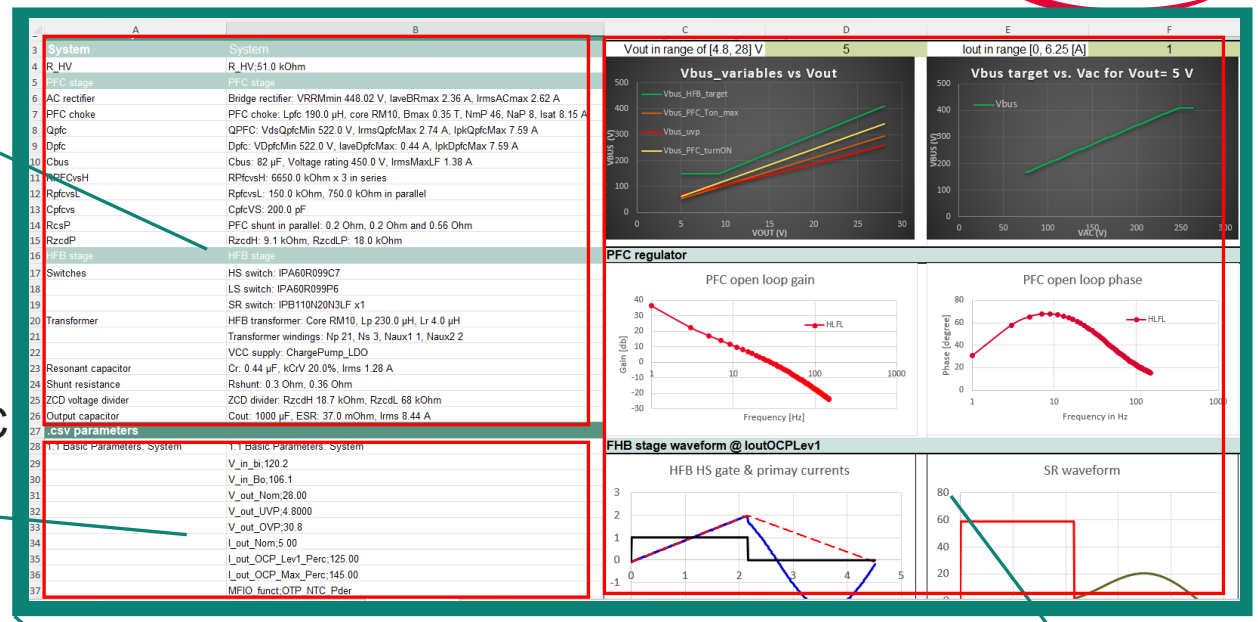
1 System design
- Information: Structure

- Two design tools available
  - HFB stage only
  - PFC+HFB combo
- Design tool layout
  - Separated sheets, example with design tool for combo-IC

Components

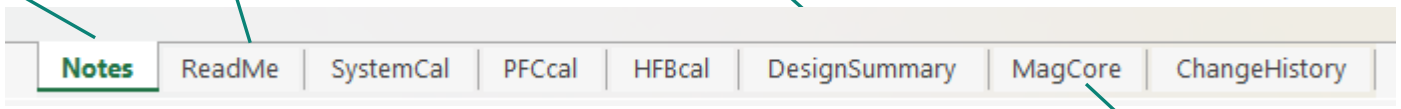


Important notes

How to use the design sheet

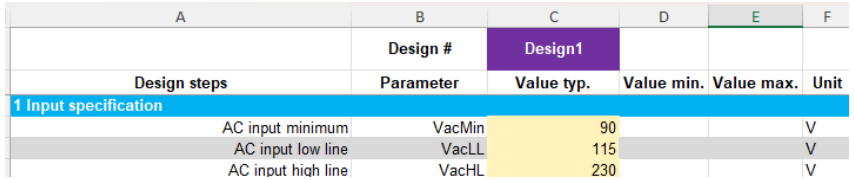
Parameters

Illustration curves



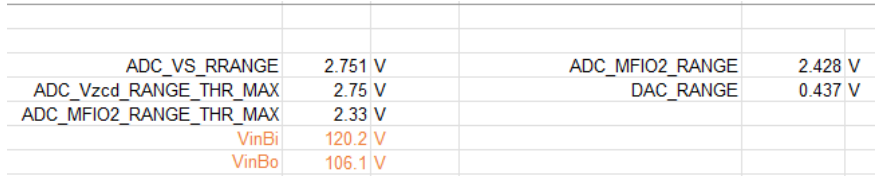
Ferrite core parameters

Main calculation



	Design #	Design1			
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit
1 Input specification					
AC input minimum	VacMin	90			V
AC input low line	VacLL	115			V
AC input high line	VacHL	230			V

Assistant calculation, design recommendation and information



ADC_VS_RRANGE	2.751 V	ADC_MFIO2_RANGE	2.428 V
ADC_Vzcd_RANGE_THR_MAX	2.75 V	DAC_RANGE	0.437 V
ADC_MFIO2_RANGE_THR_MAX	2.33 V		
VinBi	120.2 V		
VinBo	106.1 V		

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1 System design
- Information: Color index

Copied input value

Key design input, Col. G-P

Current design

Selectable value

	A	B	C	D	E	F	G
1			Design1				Design1
2	Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	140 W
15	Low side switch	QLS	IPA60R099P6				IPA60R099P6
16		CoTr_QLS	40			pF	40
17		Type_QSR	LVSi				LVSi
18		Vds_QSR	Si300V				Si300V
19	SR switch	QSR	IPB110N20N3LF				IPB110N20N3LF
20		kVds_QSR	0.8				0.80
21		Coss_QSR	630			pF	630
22		N_QSR	1			piece	1
23	9.3 Negative magnetizing current for ZVS						
24	Choosen transformer turns ratio	Ni	7.00	2.72	8.04		7.00
25	S required negative magnetizing current amplitude	IMagNegR	0.082			A	0.082
26	Selected negative magnetizing current amplitude	IMagNegS	0.20			A	0.20
27	Percentage of the negative magnetizing current	IMagNegPerc	14			%	14

Calculation result

csv parameter info

Assistant calculation

Modifiable recommendation

DS info

Assistant information

Q		R	S	T		U	V
	PoutFL	140.00	W		PinVacHLFL	148.15	W
	PinVacMaxIoutOcp1	183.25	W		PinVacLLFL	152.17	W
	PoutOcp1	175.00	W		IbusOcp1	0.44	A
	PinVacBoloutOcp1	194.44	W		IrmsVacBoloutOCp1	2.62	A
	Rhv	51.0	kOhm		VVCConMax	22	V
					IHVMinAvg	1	mA
					IHVmax	9.6	mA
	ACT_EN	OTP_NTC	OTP_NTC_	VoutTog			

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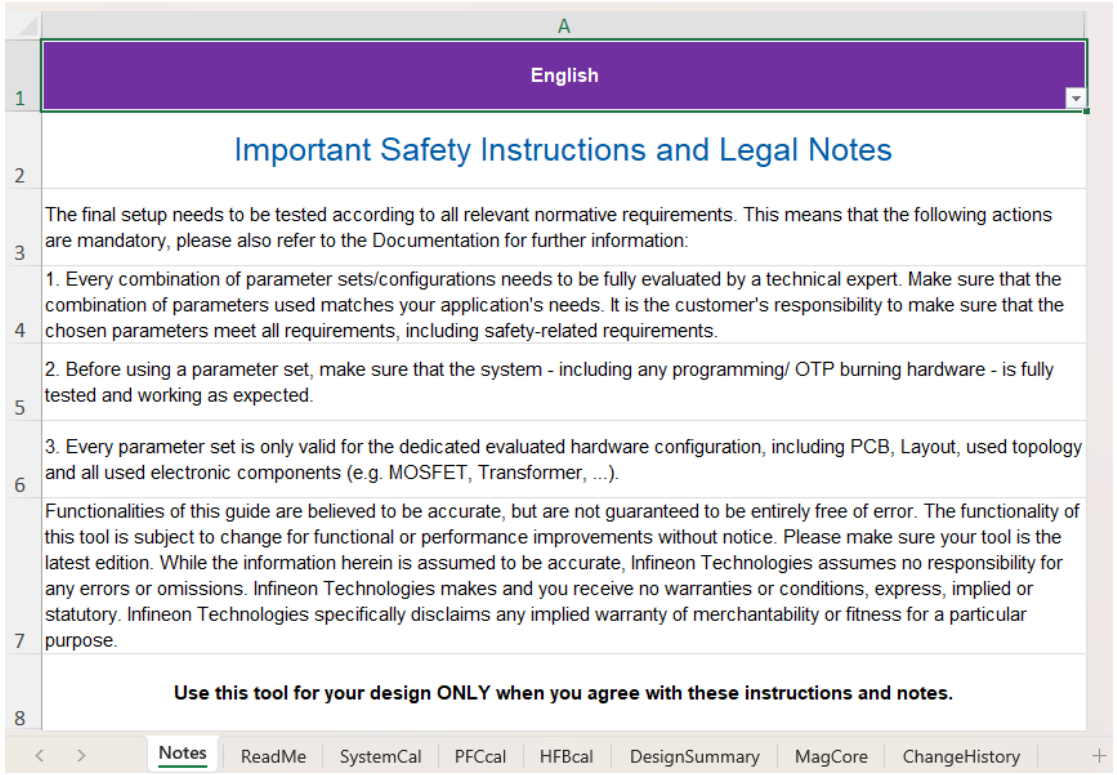
1 System design
- Information: Note and read me sheet

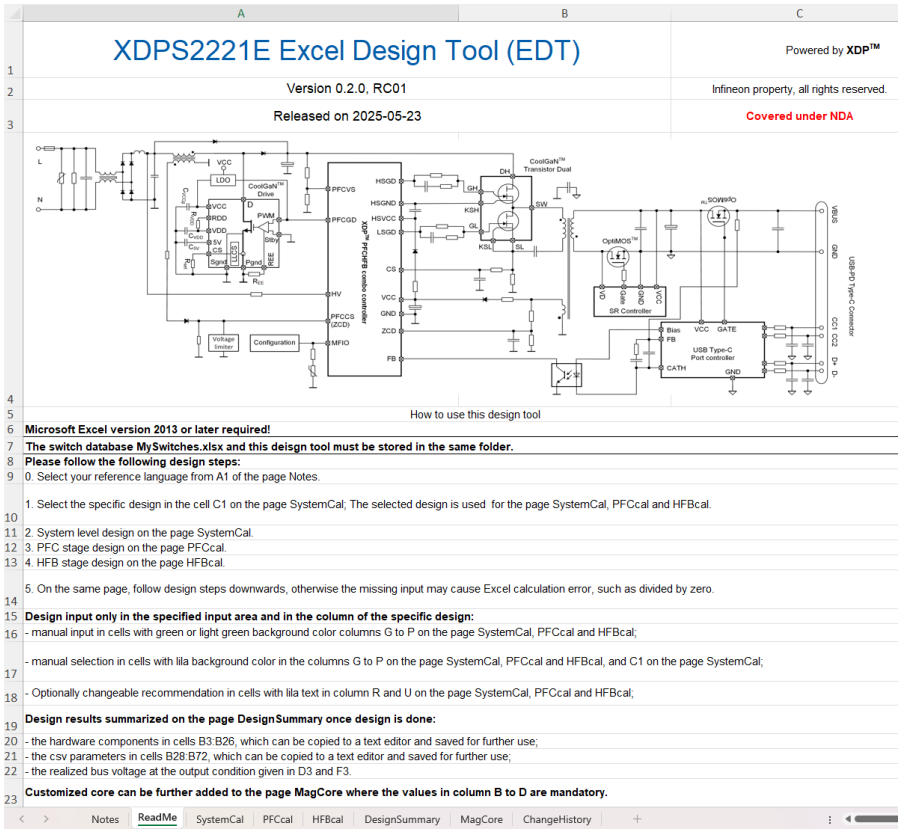
- **Notes sheet** with safety instruction and legal notes
  - Selectable language “English” or “Chinese” at A1



	A
1	English
2	Important Safety Instructions and Legal Notes
3	The final setup needs to be tested according to all relevant normative requirements. This means that the following actions are mandatory, please also refer to the Documentation for further information:
4	1. Every combination of parameter sets/configurations needs to be fully evaluated by a technical expert. Make sure that the combination of parameters used matches your application's needs. It is the customer's responsibility to make sure that the chosen parameters meet all requirements, including safety-related requirements.
5	2. Before using a parameter set, make sure that the system - including any programming/ OTP burning hardware - is fully tested and working as expected.
6	3. Every parameter set is only valid for the dedicated evaluated hardware configuration, including PCB, Layout, used topology and all used electronic components (e.g. MOSFET, Transformer, ...).
7	Functionalities of this guide are believed to be accurate, but are not guaranteed to be entirely free of error. The functionality of this tool is subject to change for functional or performance improvements without notice. Please make sure your tool is the latest edition. While the information herein is assumed to be accurate, Infineon Technologies assumes no responsibility for any errors or omissions. Infineon Technologies makes and you receive no warranties or conditions, express, implied or statutory. Infineon Technologies specifically disclaims any implied warranty of merchantability or fitness for a particular purpose.
8	**Use this tool for your design ONLY when you agree with these instructions and notes.**

Notes | ReadMe | SystemCal | PFCcal | HFBcal | DesignSummary | MagCore | ChangeHistory

- **ReadMe sheet**
  - Instruction about the step-by-step approach
  - Jump certain step may cause error, such as “divided by zero”



	A	B	C
1	XDPS2221E Excel Design Tool (EDT)		Powered by XDP™
2	Version 0.2.0, RC01		Infineon property, all rights reserved.
3	Released on 2025-05-23		Covered under NDA
4			
5	How to use this design tool		
6	**Microsoft Excel version 2013 or later required!**		
7	**The switch database MySwitches.xlsx and this deisgn tool must be stored in the same folder.**		
8	**Please follow the following design steps:**		
9	0. Select your reference language from A1 of the page Notes.		
10	1. Select the specific design in the cell C1 on the page SystemCal; The selected design is used for the page SystemCal, PFCcal and HFBcal.		
11	2. System level design on the page SystemCal.		
12	3. PFC stage design on the page PFCcal.		
13	4. HFB stage design on the page HFBcal.		
14	5. On the same page, follow design steps downwards, otherwise the missing input may cause Excel calculation error, such as divided by zero.		
15	**Design input only in the specified input area and in the column of the specific design:**		
16	- manual input in cells with green or light green background color columns G to P on the page SystemCal, PFCcal and HFBcal;		
17	- manual selection in cells with lila background color in the columns G to P on the page SystemCal, PFCcal and HFBcal, and C1 on the page SystemCal;		
18	- Optionally changeable recommendation in cells with lila text in column R and U on the page SystemCal, PFCcal and HFBcal;		
19	**Design results summarized on the page DesignSummary once design is done:**		
20	- the hardware components in cells B3:B26, which can be copied to a text editor and saved for further use;		
21	- the csv parameters in cells B28:B72, which can be copied to a text editor and saved for further use;		
22	- the realized bus voltage at the output condition given in D3 and F3.		
23	**Customized core can be further added to the page MagCore where the values in column B to D are mandatory.**		

Notes | ReadMe | SystemCal | PFCcal | HFBcal | DesignSummary | MagCore | ChangeHistory

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1 System design
- Design process: overview

- System Calculation
  1. Input specification
  2. HFB output specification
  3. Desing assumption
  4. HV design
  5. MFIO function

- PFC calculation
  6. Bus voltage setting and PFC on-, off-control
  7. PFC design
     - 7.1) Choke design
     - 7.2) PFC switch
     - 7.3) PFC boost diode
     - 7.4) PFC bus capacitor
     - 7.5) bus voltage divider
     - 7.6) PFC ZCDCS circuit
  8. Input bridge rectifier

- HFB calculation
  - 9.1) Design starting point
  - 9.2) HFB switches
  - 9.3) Negative current for ZVS
  - 9.4) Transformer inductance and resonant tank
  - 9.5) Transformer main windings
  - 9.6) VCC supply, auxiliary winding and ZCD network
  - 9.7) Shunt resistor
  - 9.8) Output capacitor

- Additional system level parameter setting
  - 10.1) mode transition voltage
  - 10.2) ZVS pulse width setting
  - 10.3) Optional PCB trace and winding resistance

- Design outcome
  - Hardware component
  - .csv parameters

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1 System design

- Desing process (1/3)

Taking the current Excel design sheet V0.2.0 as example

1. SystemCal

	A	B	C	D	E	F	G
1		Design #	Design1				Design1
2	Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
3	1 Input specification						
4	AC input minimum	VacMin	90			V	90
5	AC input low line	VacLL	115			V	115
6	AC input high line	VacHL	230			V	230
7	AC input maximum	VacMax	264			V	264
8	AC brown-in level	VacBi	85			V	85
9	AC brown-out level	VacBo	75		85	V	75
10	Line frequency minimum	facMin	47			Hz	47
11	2 HFB output specification						
12	Nominal output voltage maximum	VoutNom	28.00	0		V	28.00
13	Output under voltage level	VoutUVP	3.50			V	3.50
14	Output over voltage level	VoutOVP	30.80	28		V	30.80
15	Nominal output current	IoutNom	5.00	0.001		A	5.00
16	Output lower overcurrent protection threshold	IoutOCPLev1Perc	125	100	145	%	125.0
17	Output maximum overcurrent protection threshold	IoutOCPMaxPerc	145	125	200	%	145.0
18	3 Design assumption						
19	Power factor at low line and nominal load	PF	0.99				0.99
20	System efficiency at max line and nominal load	EtaSysVacMax	95.5%				95.5%
21	System efficiency at high line and nominal load	EtaSysVacHL	94.5%				94.5%
22	System efficiency at low line and nominal load	EtaSysVacLL	92.0%				92.0%
23	System efficiency at VacBo and IoutOCPLev1	EtaSysVacBo	90.0%				90.0%
24	HFB efficiency at the nominal condition	EtaHFB	98.0%				98.0%
25	4 Rhv					kOhm	
26		Rhv1	27.0			kOhm	27
27		Rhv2	24.0	49.8	52.5	kOhm	24
28		Rhv3	0.0			kOhm	
29	5 MFIO function						
30		MFIO_funct	OTP_NTC				OTP_NTC
31		R_MFIO_OTP_trig	7.70			kOhm	7.70
32		R_MFIO_OTP_rel	51.40	7.7		kOhm	51.40
33		N_OTP_ev_max	2		255		2
34							
35							
36	Design output						
37	Hardware components						
38	R_HV;51.0 kOhm	R_HV					R_HV;51.00
39	.csv parameters						
40		1.1 Basic Parameters: Sy					
41	V_in_bi;120.2	V_in_bi					
42	V_in_Bo;106.1	V_in_bo					
43	V_out_Nom;28.00	V_out_nom					
44	V_out_UVP;3.5000	V_out_UVP					
45	V_out_OVP;30.8	V_out_OVP					
46	I_out_Nom;5.00	I_out_nom					
47	I_out_OCP_Lev1_Perc;125.00	I_Out_OCP_lev1_perc					
48	I_out_OCP_Max_Perc;145.00	I_Out_OCP_max_perc					
49	MFIO_funct;OTP_NTC	MFIO_funct					
50		2.1 Advanced parameter					
51	R_HV;51.00	R_HV					
52		V_out_MFIO_goL					
53		V_out_MFIO_goH					
54		2.4 Advanced parameter					
55	N_OTP_ev_max;2	N_OTP_ev_max					
56	R_MFIO_OTP_trig;7.70	R_MFIO_OTP_trig					
57	R_MFIO_OTP_rel;51.40	R_MFIO_OTP_rel					

Notes | ReadMe | SystemCal | PFCcal | HFBcal | DesignSummary | MagCore | ChangeHistory

2. PFCcal

	A	B	C	D	E	F	G
1		Design #	Design1				Design1
2	Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
3	6 Bus voltage setting and PFC on-, off-control						
4	Bus capacitor voltage rating	VbusCapRvMin	450.00	410.7		V	450.00
5	Divider ratio (RvsH+RvsL)/RvsL	kPFCvs	160.71	155.17	166.67		160.71
6	Bus OVP level	VbusOvp	435.00	419.46	450.54	V	435.00
7	Target bus voltage maximum	VbusTargetMax	410.00	392.02	435	V	410.00
8	Target bus voltage minimum	VbusTargetMin	150.00	117	390	V	150.00
9	Additional PFC stage control	P_PFC_enable	60.0			W	60.0
10		P_PFC_disable	45.0		60	W	45.0
11		V_bus_PFCstop	430.0	410.0	435.0	V	430.0
12		V_bus_PFCresume	410.0	150.0	430.0	V	410.0
13	7 PFC design						
14	7.1 Choke design						
15	PFC switching frequency minimum	fswMin	56.00			kHz	56.00
16	PFC choke inductance design value	LPfc	180.00		191	µH	180.00
17	Oscillation period of the PFC Vds	Tosc_P	0.88			µs	0.880
18	PFC tonMax with impact of valley switching	tPfcOnMax	12.76			µs	12.76
19	switchign frequency at VacBo peak and IoutOCP1	fswAcBoPkOCP1	56.64			kHz	56.64
20	Core selected	Core_P	RM10				RM10
21	Core flux maximum	Bmax_P	0.35			T	0.35
22	Turns count of the PFC choke main winding	NM_p	46	24.80			46
23	Turns count of the PFC choke auxiliary winding	NA_P	8	2.28			8
24	Choke RMS current maximum over AC cycle	IrmsLPFCmax	3.02			A	3.02
25	7.2 PFC switch						
26	Voltage rating minimum	VdsMin_Qpfc	522			V	522
27	Switch peak current maximum	IpkMax_Qpfc	4.85			A	4.85
28	Switch rms current maximum over AC cycle	IrmsMax_Qpfc	1.75			A	1.75
29	Type of the selected PFC switch	Type_Qpfc	With OCP				With OCP
30	Ratio of Ids/Ics	kI_Qpfc	3520.00				3520.00
31	OCP threshold	Vtrip	1.90			V	1.90
32	7.3 PFC boost diode						
33	Voltage rating minimum	VrrmMin_Dpfc	522			V	522
34	Peak current maximum	IpkMax_Dpfc	4.85			A	4.85
35	Average current maximum over AC cycle	IaveMax_Dpfc	0.44			A	0.44
36	RMS current maximum over AC cycle	IrmsMax_Dpfc	0.93			A	0.93
37	7.4 PFC bus capacitor						
38	Bus voltage ripple at VacBo and Iout Ocp1	VbusRppl	20.00			V	20.00
39	Bus capacitance selected	Cbus	82	81		uF	82
40	Low frequent bus RMS current maximum	IrmsLF_Cbus	0.82			A	0.82
41	7.5 Bus voltage divider						
42	1st resistor at lowside	RPfcvsL1_Base	1.5		53,033	kOhm	1.50
43		RPfcvsL1_Factor	100k				100k
44	2nd parallel resistor at lowside, optional	RPfcvsL2_Base	7.5			kOhm	7.50
45		RPfcvsL2_Factor	100k				100k
46	Number of in-series connected same resistors	NRpfcvsH	2				2
47	Resistance of the single high-side resistor	RPfcvsH_Base	1.05	9,760.00	9,760.00	kOhm	1.05
48		RPfcvsH_Factor	10Meg				10Meg
49	kPFCVS design error	kpfcvs_DE	-5.16%				-5.16%
50	PFCVS filter capacitance proposal	Cpfcvs			229	pF	200
51	7.6 PFCZCDCS circuit						
52	7.6.1 PFC zcd divider						
53	Highside divider resistor	RzcdH_P_Base	9.1		92.69	kOhm	9.10
54		RzcdH_P_Factor	1k				1k
55	Lowside divider resistor	RzcdL_P_Base	1.8	5.86		kOhm	1.80
56		RzcdL_P_Factor	10k				10k
57	Diode Dzcd blocking voltage rating minimum	VrrmMin_DzcdP	76			V	76
58	Diode Dzcd current rating mamimum	IfMin_DzcdP	48			mA	48
59	7.6.2 PFC CS						
60	Required PFC shunt resistance	RCSpR	1,379.985			Ohm	1,379.985
61							
62							
63							
64							
65							
66	Selected sense resistance	RcsPFC_base	1.37				1.37
67		RcsPFC_factor	1k				1k
68	7.7 PFC control parameters						
69		PFC_CoefA	128	128	2047		128
70		PFC_CoefB	256	256	2047		256
71		PFC_CoefT1	6	4	6		6
72	8 Input bridge rectifier						
73	Voltage rating minimum	VrrmMin_DBR	448			V	448

Notes | ReadMe | SystemCal | PFCcal | HFBcal | DesignSummary | MagCore | ChangeHistory

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1 System design

- Desing process (2/3)

3. HFBcal

	A	B	C	D	E	F	G
1		Design #	Design1				Design1
2	Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
3	9 HFB design						
4	9.1 Design starting point conditions						
5	Desired switching frequency	fswD	205.0		400	kHz	205.0
6	Maximum duty at VbusBoNom and nominal load	Dmax	75%				75%
7	Bus brownout at nominal output voltage	VbusBoNom	300.0	261		V	300.0
8	9.2 Selection of switches						
9	9.2.1 High side switch						
10	Product for the HS switch	QHS	IPD60R600P7				IPD60R600P7
11	CoTr of the selected HS switch	CoTr_QHS	30			pF	30
12	9.2.2 Low side switch						
13	Product for the LS switch	QLS	IGLD60R190D1				IGLD60R190D1
14	CoTr of the selected LS switch	CoTr_QLS	30			pF	30
15	9.2.3 2nd side rectifier						
16	Type of the 2nd side rectifier	Type_2ndRect	SR				SR
17	Voltage derating factor of the 2nd side rectifier	kVdr_2ndRect	0.8				0.80
18	SR switch	QSR	BSC160N15NS5				BSC160N15NS5
19	Coss of the SR switch	Coss_QSR	340			pF	340
20	Number of the SR switches in parallel	N_QSR	2			piece	2
21							
22	9.3 Negative magnetizing current for ZVS						
23	Choosen transformer turns ratio	Ni	7.00	3.63	8.04		7.00
24	ZVS required negative magnetizing current amplitude	IMagNegR	0.066			A	0.066
25	Selected negative magnetizing current amplitude	IMagNegS	0.16			A	0.16
26	Percentage of the negative magnetizing current	IMagNegPerc	11			%	11
27	Magnetizing current positive peak value at IoutNom	IMagPosNom	1.589			A	1.589
28	Magnetizing current positive peak value at IoutOCPLev1	IMagPosOcp1	1.946			A	1.946
29	9.4 Transformer inductance and resonant tank						
30	Output power level for HFB optimization	Psel	IoutOCPLev1				IoutOCPLev1
31	Magnetizing inductance calculated	LpCal	213.19			µH	213.19
32	Magnetizing inductance choosen	Lp	230			µH	230
33	Leakage inductance calculated	Lr	4.0			µH	4.0
34	Resonant capacitance at the nominal condition	CrCal	0.085			µF	0.085
35	Average voltage across the resonant capacitor	VCrAvg	196.0			V	196.0
36	Factor of the capacitance at the VCrAvg over at 0 V	kCrV	20%				20.0%
37	Capacitance at 0 V bias	Cr0V	0.424			µF	0.424
38	Selected value of the resonant capacitors	Cr	0.440			µF	0.440
39	Calculated LS on time at the nominal output	tTransNom	2.290			µs	2.290
40	Percentage of tTRANSnom at 0 V bias	tTransRvs0Vperc	223.6			%	223.6
41	Equivalent ESR of the resonant capacitor	CrESR	10			mOhm	10
42	9.5 Transformer main windings						
43	Maximal core flux	Bmax	0.35			T	0.35
44	Core selected	Core	RM10				RM10
45	Selected turns count of the secondary winding	Ns	3	3.00		turns	3
46	Selected turns count of the primary winding	Np	21	15.96		turns	21
47	Realized turns ratio of Np:Ns	N	7.00	3.63	8.04		7.00
48	DC resistance of the transformer primary winding	RdcPri	60.0			mOhm	60.0
49	DC resistance of the transformer secondary winding	RdcSec	7.0			mOhm	7.0
50	9.6 VCC supply, auxiliary widings and ZCD network						
51	VCC supply solution proposal		Charge pump + LDO, or Flyback + boost for advanced design				Charge pump + LDO, or Flyback + boost for advanced design
52	VCC supply solution selected		ChargePump_LDO				ChargePump_LDO
53	Target VCC voltage fron the auxiliary winding	VVCCT	12.0			V	12.0
54	Diode forward conduction voltage	Vf_Dvcc	0.7			V	0.7
55							
56							
57							
58							
59							
60							
61							
62							
63	9.6.2 Option 2: charger pump + LDO						
64	1st auxiliary winding turns count	NA1_CP	1	1.00	1.13		1

Notes | ReadMe | SystemCal | PFCcal | HFBcal | DesignSummary | MagCore | ChangeHistory

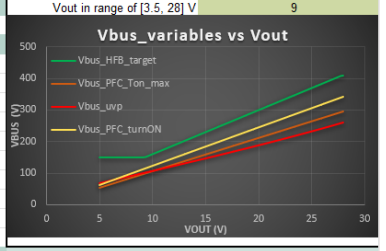
4. DesignSummary

Design illustration

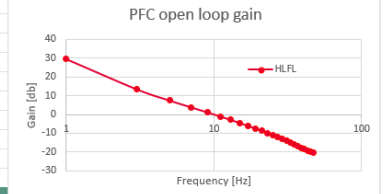
Hardware

.csv parameters

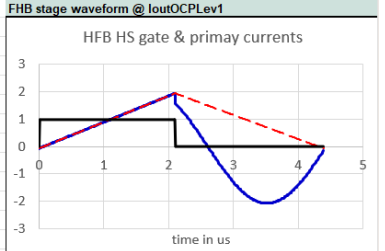
	A	B	C	D
1	Design #	Design1		Key de
2	Hardware components		Bus voltage depending on the given Vout and Iout	
3	System	System	Vout in range of [3.5, 28] V	9
4	R_HV	R_HV;51.0 kOhm		
5	PFC stage	PFC stage		
6	AC rectifier	Bridge rectifier: VRRMmin 448.02 V, IaveBRmax 2.36 A, IrmsACmax 2.62 A		
7	PFC choke	PFC choke: Lpfc 180.0 µH, core RM10, Bmax 0.35 T, NmP 46, NaP 8, Isat 4.73 A		
8	Qpfc	QPFC: VdsQpfcMin 522.0 V, IrmsQpfcMax 1.75 A, IpkQpfcMax 4.85 A		
9	Dpfc	Dpfc: VDpfcMin 522.0 V, IaveDpfcMax: 0.44 A, IpkDpfcMax 4.85 A		
10	Cbus	Cbus: 82 µF, Voltage rating 450.0 V, IrmsMaxLF 0.82 A		
11	RPFCvsH	RPfcvsH: 10500.0 kOhm x 2 in series		
12	RpfcvsL	RpfcvsL: 150.0 kOhm, 750.0 kOhm in parallel		
13	Cpfcvs	CpfcVS: 200.0 pF		
14	RcsP	PFC switch current sense resistance: 1370 Ohm		
15	RzcdP	RzcdH: 9.1 kOhm, RzcdLP: 18.0 kOhm		
16	HFB stage	HFB stage		
17	Switches	HS switch: IPD60R600P7		
18		LS switch: IGLD60R190D1		
19		Secondary side recitifier: BSC160N15NS5 x 2		
20	Transformer	HFB transformer: Core RM10, Lp 230.0 µH, Lr 4.0 µH		
21		Transformer windings: Np 21, Ns 3, Naux1 1, Naux2 2		
22		VCC supply: ChargePump_LDO		
23	Resonant capacitor	Cr: 0.44 µF, kCrV 20.0%, Irms 1.23 A		
24	Shunt resistance	Rshunt: 0.33 Ohm, 0.33 Ohm		
25	ZCD voltage divider	ZCD divider: RzcdH 18.7 kOhm, RzcdL 6.8 kOhm		
26	Output capacitor	Cout: 1000 µF, ESR: 37.0 mOhm, Irms 8.22 A		
27	csv parameters			
28	1.1 Basic Parameters: System	1.1 Basic Parameters: System		
29		V_in_bi;120.2		
30		V_in_Bo;106.1		
31		V_out_Nom;28.00		
32		V_out_UVP;3.5000		
33		V_out_OVP;30.8		
34		I_out_Nom;5.00		
35		I_out_OCP_Lev1_Perc;125.00		
36		I_out_OCP_Max_Perc;145.00		
37		MFIO_funct;OTP_NTC		
38	1.2 Basic Parameters: HFB	1.2 Basic Parameters: HFB		
39		Switch_Type;Si		
40		N;7.0		
41		t_TRANS_nom;2.29		
42		t_TRANS_RVS_0V_perc;224		
43		I_MAG_neg_Nom_perc;11.2		
44		V_out_CRM2RVS;16.00		
45		V_out_RVS2CRM;18.00		
46		t_zvs_min;600		
47	1.3 Basic Parameters: PFC	1.3 Basic Parameters: PFC		
48		V_busCap_RV_min;450.0		
49		V_bus_OVP;435.0		



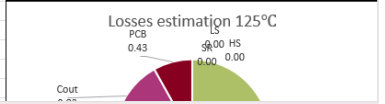
PFC regulator



FHB stage waveform @ IoutOCPLev1



HFB stage power losses estimation @ IoutOCPLev1



Notes | ReadMe | SystemCal | PFCcal | HFBcal | DesignSummary | MagCore | ChangeHistory

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1 System design

- Desing process (3/3)

Taking the current Excel design sheet as example

– Optional customized magnetic core

	A	B	C	D	E	F	G	H	I
1		Required parameters							
2	Required parameters	Effective magnetic cross section	Effective magnetic volume	Winding cross section	Window height	Window width	Effective magnetic path length	Average length of turns	Thermal resistance
3	**Magnetic core type**	**Ae mm2**	**Ve mm3**	**An mm2**	**Wh mm**	**Ww mm**	**le mm**	**lt mm**	**Rth k/W**
4	E16/8/5	20.1	756	22.3	10	2.6	37.6	34	65
5	E20/10/6	32.1	1490	34	12.5	3.4	46.3	41.2	46
6	E25/13/7	52.5	3020	61	15.6	3.95	57.5	50	40
7	E30/15/7	60	4000	90	17.5	5.15	67	56	23
8	E32/16/11	97	7187	108.5	20.1	5.55	74	64.4	22
9	E36/18/11	120	9670	122.55	21.5	5.7	81	76.4	18
10	EFD25/13/9	58	3310	40.7	16.4	3.15	57	50	
11	EFD30/15/9	69	4690	52.3	20	3.325	68	56.7	
12	EQ25	89.7	2370		6.4	5.5	26.4		
13	ER42/22/15	170	16800	222	27.6	5.8	99	70.8	
14	ETD29/16/10	76	5350	97	19.4	4.85	70.4	52.8	
15	ETD34/17/11	97.1	7630	122	20.9	5.8	78.6	60.5	
16	PQ2620	121	5470	31.3			45		
17	PQ3220	154.2	7460	47	10	5	48.4	66	
18	RM10	98	4310	41.5	10.9	4.25	44	52	
19	RM10_LP	99.1	3360				33.9		
20	RM12	146	8320	73	15	5	57	61	
21	RM12_LP	147.5	6195	73			42	6	
22	RM14	200	14000	107	18	6	70	71.5	
23	RM7	44.1	1325	39.6	8.4	3.75	30	30	
24	RM8	64	2430	30	8.9	4.15	38	42	
25	rr								
26									
27									
28									
29									
30									

Notes | ReadMe | SystemCal | PFCcal | HFBcal | DesignSummary | MagCore | ChangeHistory

– Change history

	A	B	C
1	**Change history**		
2	**Version**	**Date**	**Remark**
3	V0.2.0, RC01	2025-06-24	PFC optimisation options added Min of VinBo updated Holdup time requirement for the bus capacitance added Power losses in the PFC VS path added HFB Lp calculation modified/add the option of IoutNom (HFBcal line 31) HB and SR database move to a separate file MySwitches.xlsx
4	V0.1.0, RC01	2025-01-09	Initial release, RC01
5			
6			
7			
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17			
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19			
20			

Notes | ReadMe | SystemCal | PFCcal | HFBcal | DesignSummary | MagCore | ChangeHistory

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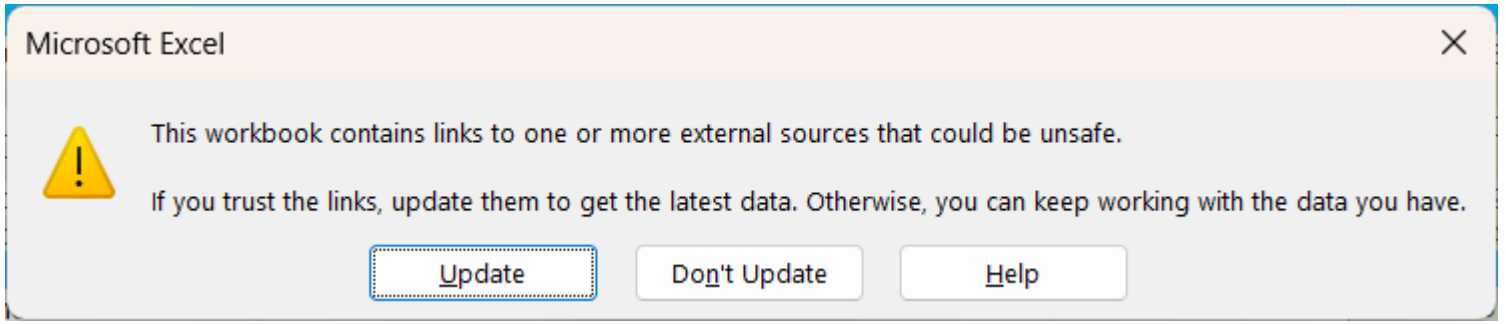
1 System design
- Information: Update link at start-up

- ***Design tool V0.2.0***
  - Message at opening the design tool



  - A separate file about the switches used in the design sheets, called MySwitches.xlsx
  - Design sheet picking up certain information about the selected switch directly from the MySwitches.xlsx file.
  - This pop-up box offering users the opportunity to update that link and pick up the respected value

- ***Design tool V1.0.0***
  - ***Switch information as direct input***

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1 System design

- Database MySwitches.xlsx update (1/2)

Taking the current Excel design sheet V0.2.0 as example

– MyMOSFET

	A	B	C	D	E
1	Product	Data Sheet	Product Status	Simulation Model	Qualification
2	BSS192P	https://www.infineon.cc	active and preferred	/cms/en/product/power/mo	Automotive
3	BSR92P	https://www.infineon.cc	active and preferred	/cms/en/product/power/mo	Automotive
4	BSP317P	https://www.infineon.cc	active and preferred	/cms/en/product/power/mo	Automotive
5	BSP92P	https://www.infineon.cc	active	/cms/en/product/power/mo	Automotive
6	ISZ15EP15LM	https://www.infineon.cc	active and preferred		Industrial
7	ISZ56DP15LM	https://www.infineon.cc	active and preferred		Industrial
8	ISZ75DP15LM	https://www.infineon.cc	active and preferred		Industrial
9	ISP14EP15LM	https://www.infineon.cc	active and preferred		Industrial
10	IPD42DP15LM	https://www.infineon.cc	active and preferred		Industrial
11	ISC16DP15LM	https://www.infineon.cc	active and preferred		Industrial
12	IPB720P15LM	https://www.infineon.cc	active and preferred		Industrial
13	IRFR6215	https://www.infineon.cc	activeactive		Standard
14	SPD04P10PL G	https://www.infineon.cc	active and preferred	/cms/en/product/power/mo	Automotive
15	SPD15P10P G	https://www.infineon.cc	active and preferred	/cms/en/product/power/mo	Automotive
16	SPD15P10PL G	https://www.infineon.cc	active and preferred	/cms/en/product/power/mo	Automotive
17	ISP16DP10LMA	https://www.infineon.cc	active and preferred		Automotive
18	IPD11DP10NM	https://www.infineon.cc	active and preferred		Industrial
19	ISZ24DP10LM	https://www.infineon.cc	active and preferred		Industrial
20	IPB320P10LM	https://www.infineon.cc	active and preferred		Industrial
21	IPB19DP10NM	https://www.infineon.cc	active and preferred		Industrial
22	IPP330P10NM	https://www.infineon.cc	active and preferred		Industrial
23	ISP98DP10LM	https://www.infineon.cc	active and preferred		Industrial
24	ISP16DP10LM	https://www.infineon.cc	active and preferred		Industrial
25	ISP20EP10LM	https://www.infineon.cc	active and preferred		Industrial

MyMOSFET | MyGaN

– MyGaN

	A	B	C	D	E
1	Product	Data Sheet	Generation	Product Status	Infineon Pac
2	IGC019S06S1	https://www.infineon.com/	G3	active and preferred	PG-TSON-6
3	IGC025S08S1	https://www.infineon.com/	G3	active and preferred	PG-TSON-6
4	IGC033S101	https://www.infineon.com/	G3	active and preferred	PG-VSON-6
5	IGC033S10S1	https://www.infineon.com/	G3	active and preferred	PG-TSON-6
6	IGB070S10S1	https://www.infineon.com/	G3	active and preferred	PG-TSON-4
7	GS61008P-TR	https://www.infineon.com/	≤ G2	active	PG-ULGA-5
8	IGB110S101	https://www.infineon.com/	G3	active and preferred	PG-VSON-4
9	IGB110S10S1	https://www.infineon.com/	G3	active and preferred	PG-TSON-4
10	GS61004B-TR	https://www.infineon.com/	≤ G2	active	PG-ULGA-3
11	IGC037S12S1	https://www.infineon.com/	G3	active and preferred	PG-TSON-6
12	IGC090S20S1	https://www.infineon.com/	G3	coming soon	PG-TSON-6
13	GS66516T-TR	https://www.infineon.com/	≤ G3	active and preferred	PG-ULGA-4
14	GS-065-060-5-T-A-TR	https://www.infineon.com/	≤ G3	on request	PG-WLGA-4
15	IGT65R025D2	https://www.infineon.com/	G5	active and preferred	PG-HSOF-8
16	GS66516B-TR	https://www.infineon.com/	≤ G3	active and preferred	PG-ULGA-6
17	IGLT65R025D2	https://www.infineon.com/	G5	active and preferred	PG-HDSOP-16
18	IGOT65R025D2	https://www.infineon.com/	G5	active and preferred	PG-DSO-20
19	IGLT65R035D2	https://www.infineon.com/	G5	active and preferred	PG-HDSOP-16
20	IGT65R035D2	https://www.infineon.com/	G5	active and preferred	PG-HSOF-8
21	IGOT65R035D2	https://www.infineon.com/	G5	active and preferred	PG-DSO-20
22	IGLT65R045D2	https://www.infineon.com/	G5	active and preferred	PG-HDSOP-16
23	IGT65R045D2	https://www.infineon.com/	G5	active and preferred	PG-HSOF-8
24	IGOT65R045D2	https://www.infineon.com/	G5	active and preferred	PG-DSO-20
25	GS66508B-TR	https://www.infineon.com/	≤ G3	active and preferred	PG-ULGA-4
26	GS66508T-TR	https://www.infineon.com/	≤ G3	active and preferred	PG-ULGA-4
27	GS-065-030-2-L-TR	https://www.infineon.com/	≤ G3	active and preferred	PG-VSON-8

MyMOSFET | MyGaN

https://www.infineon.com/product-table/power-mosfets

https://www.infineon.com/products/power/gallium-nitride/gallium-nitride-transistor#products

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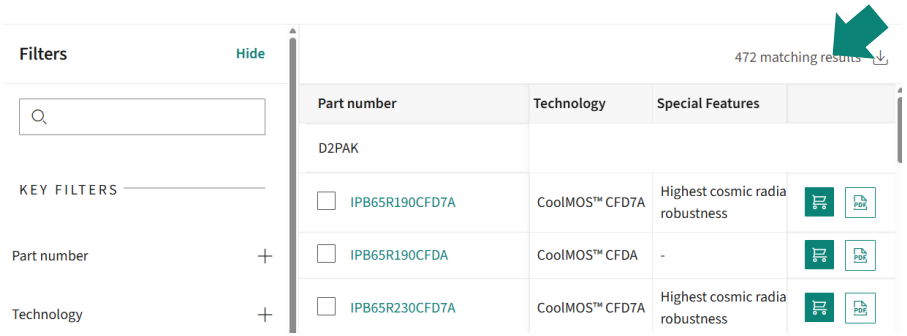
1 System design
- Database MySwitches.xlsx update (2/2)

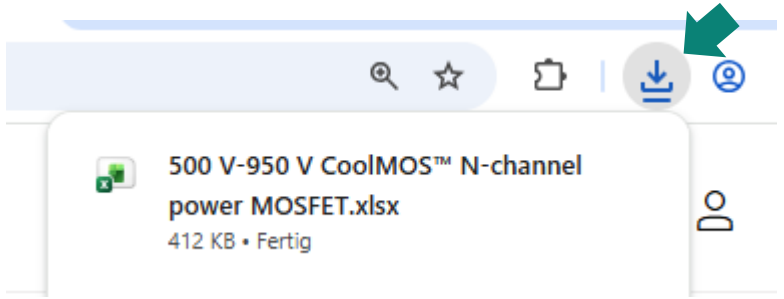
– Necessary steps to update the switch database
  – **Taking the 500 V-900 V N-channel MOSFETs as example**
  1. Go to Infineon's web page and select the product class



  2. Click on the "view product" button



  3. Click on the download button and check download status



  4. Open the downloaded file
  5. Copy the whole sheet, paste it to the sheet MyMOSFET and save the file.

  – **The same procedure for update the SR MOSFET database**

– The database for the MOSFET updated

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1 System design
- Board development

- Design and review
  - Schematic draft
    - Component selection
      - Voltage and current rating
      - Package, dimension of bulk devices
  - PCB development
    - Board floor plan and component placement
      - Controller IC outside of any loops with pulse current
      - Bus capacitor position enabling short ground connections
      - Varistor close to input terminals and small loop area
      - Separation and proper distance of the input filter and others
      - Small signal components close to the IC, including the lower one of the bus voltage divider high-side resistors
    - Key signals and cautions
      - PFC: CS/ZCD, bus voltage sense
      - HFB: CS, FB, and ZCD
      - CS: Differential pair routing vs. short & width ground
      - FB: Differential pair routing and small loop
      - Proper distance to signals with high dv/dt or high di/dt
    - Grounding concept
      - Bus capacitor ground as the potential reference
      - Star-connection of all ground connections
      - Short and wide ground connections
      - Separate tracks for different stages: input, PFC and HFB
      - Using Kelvin grounding for driving signal if applicable
      - Short and wide ground connection of the Y-capacitor at both sides
    - High di/dt loops: Small area for power loops, gate driver
    - high dv/dt signals: Short trace and distance to other signals, no overlap of the half bridge highside driver circuitry and other signals
    - Thermal and EMC metal cover
      - Grounding: primary vs. secondary side (safety, insulation, EMC and thermal distribution)
      - Recommendation: No overlap with the controller HV pin and its external resistors, and half-bridge switching node
  - Board assembly
    - Polarity and terminals
    - Soldering temperature and solder paste
    - ESD protection measures

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1 System design
- Board inspection

Optical check

- Component
  - Nothing missing
  - Correctly placed
  - Clean and proper soldered
  - Heat sink properly attached to components and thermal interface materials correctly applied

Components check

- Capacitors
  - correct polarity, voltage rating, and physical condition
- Transformers and inductors
  - Correct winding orientation and insulation.
- Semiconductors
  - correct pin marking

Circuit check

- Check connectivity of the main signal paths using a multimeter:
  - Path from AC input to bus capacitor
  - Half-bridge primary side path
  - Output current loop and feedback loop
  - IC pins and board

Test setup

- Board connection
  - Connect AC-source to the input
  - Connect DC-load to the output
  - Setup and connect scope to VCC, MFIO, LSGD, FB

Recommendation: Only use a power-analyzer for efficiency and standby-power consumption measurement

Attention: Lethal voltages are present on the hardware.
Do not operate unless you are trained to handle high-voltage circuits.

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Design Flow
- Overview

1. System design & hardware preparation
   - Input
     - Application specific parameters
     - Design intention
   - Outcome as proposal
     - Hardware value
     - .csv parameters



2. FW parameterization
   - Interface board required
   - dpVision tool, .csv file and images required
   - FW parameter value update in dpVision
   - Download parameter value to IC



3. First power-up and general tests
   - First system cold power-up
   - General operation check

4. System optimization
   - Hardware update
   - Parameter finetune
     - To achieve desired performance and operating behavior
     - Individual protection settings



5. Finalizing the design
   - Fix hardware
   - Burn .csv parameters
   - Production release

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2 FW parameterization
- Three required components (1/3)

– XDP™ hybrid flyback controllers requiring parameterization

– **Three** items necessary for parameterization

1. **Interface board**: https://www.infineon.com/evaluation-board/IF-BOARD-DP-GEN2

   – FW version 2.5 (dpIfGen2_V2.5.0_2017_6_27) or later required

   – Checking process

   – Step 1-3

   –

   – FW update

   – Step 4-6

   – Connection

   – To computer per short USB cable

   – 50 cm or shorter USB cable proposed

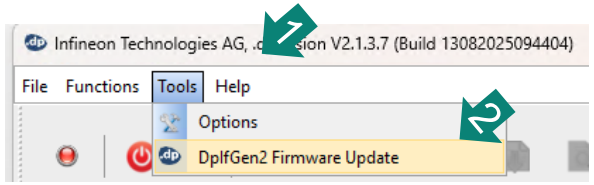
   – To power board per short connection

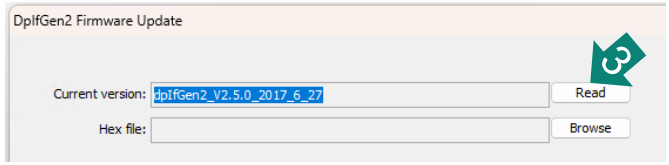
   – VCC, Comm (MFIO), GND

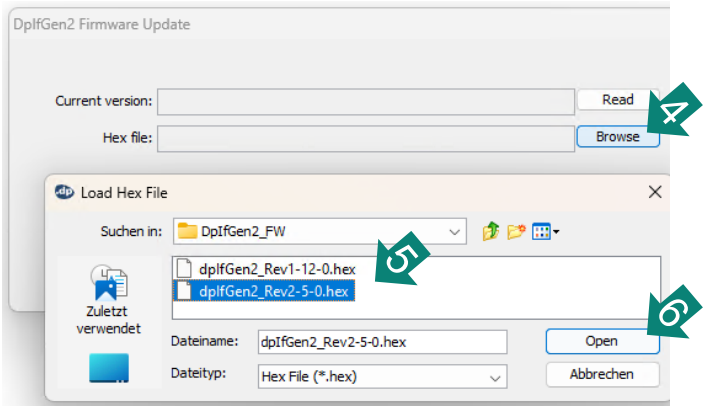
   – Supporting

   – Test configuration set during test / debugging

   – Burn parameters set once value finalized







.dp interface board Gen2



Sideview



8-pin connector; Comm to IC's MFIO pin

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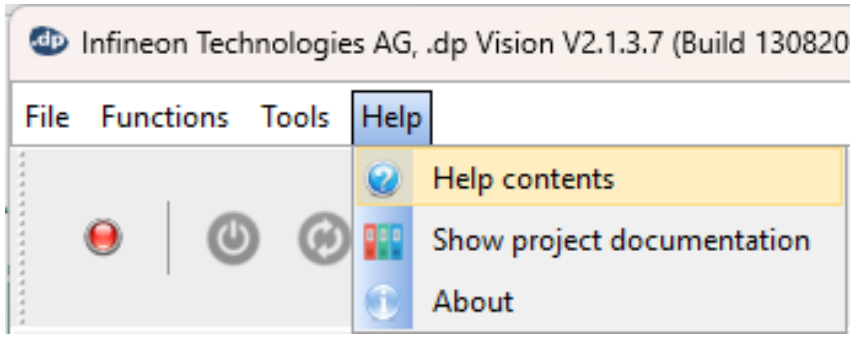
2 FW parameterization
- Three required components (2/3)

2. dp Vision tool

- Two versions available at: https://softwaretools.infineon.com/tools/com.ifx.tb.tool.dpvision
- Different product requiring different version of the dpVision tool
  - XDPS2201, XDPS2221, XDPS2222
    - **Version 2.1.1.0**
  - XDPS2201E, XDPS2221E
    - **Version 2.1.3.7:** having more features, including import values from a .txt file
  - Important: Both tools can be installed on one computer, but DO NOT run both at the same time!

- User manual inside the dpVision tool
  - Help\Help contents



  - Attention: some content is not up-to-date

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2 FW parameterization
- Three required components (3/3)

3. .csv file and illustrating images

- .csv file containing parameters
  - Configurable
    - Basic parameters: application specified parameters
    - Advanced parameters: mainly for advanced super users
  - Constants
  - Derived parameter
- Illustrating images
  - For easy understanding of the parameters
  - Must be stored under C:\Users\xxx\Infineon Technologies AG\.dp Vision\Images, where xxx to be replaced by your username in your computer system
- Product specific

- Precondition for parameterization
  - FW main version number in the IC = FW main version number in the loaded .csv file; Otherwise, no communication between the IC and computer ➔ use the dedicated .csv file for the selected product

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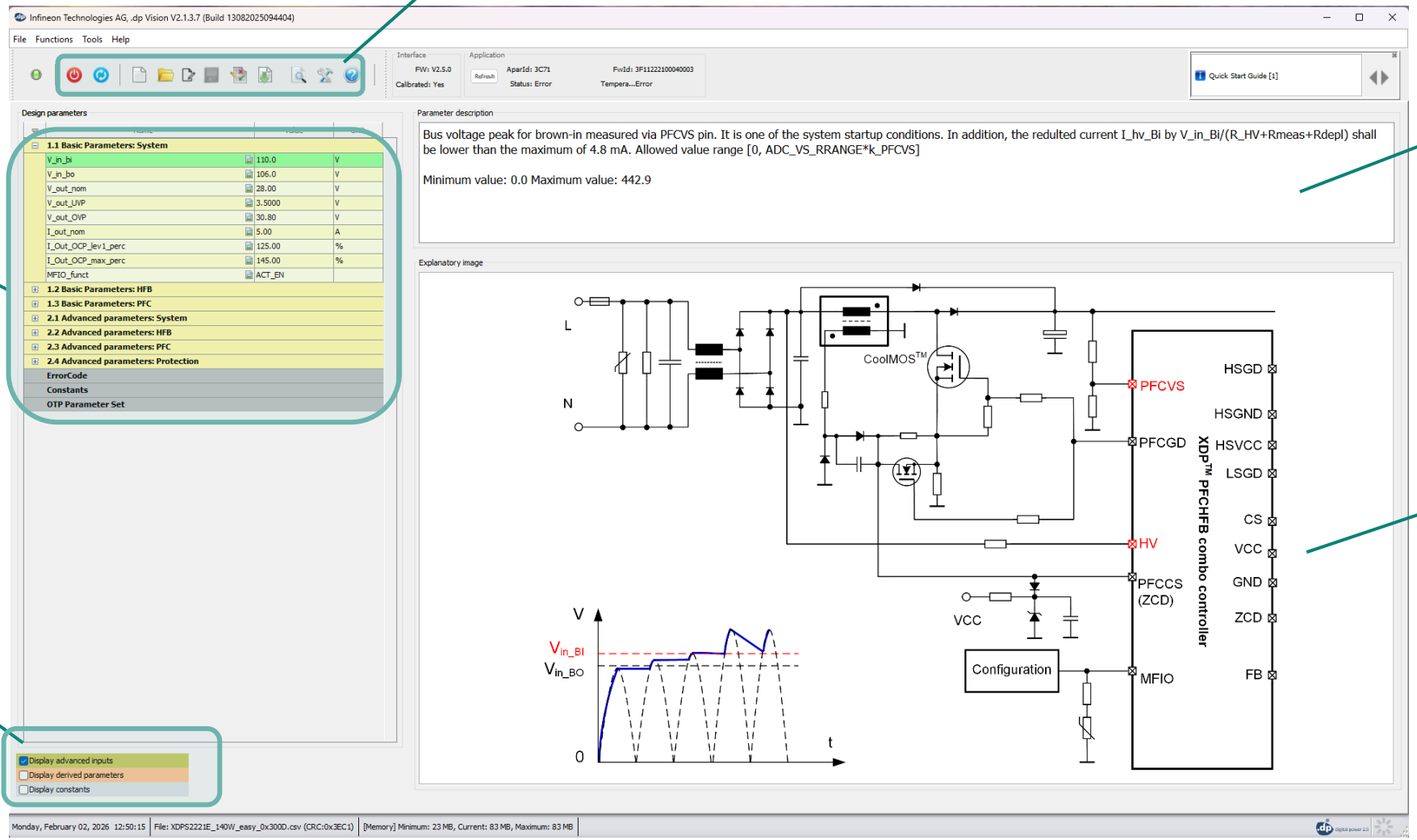
2 FW parameterization
- dpVision: GUI of V2.1.3.7

Quick access buttons



Parameters

Switch boxes

Parameter description; Font size changeable by *CTRL + mouse scroll wheel*

Parameter illustrating image

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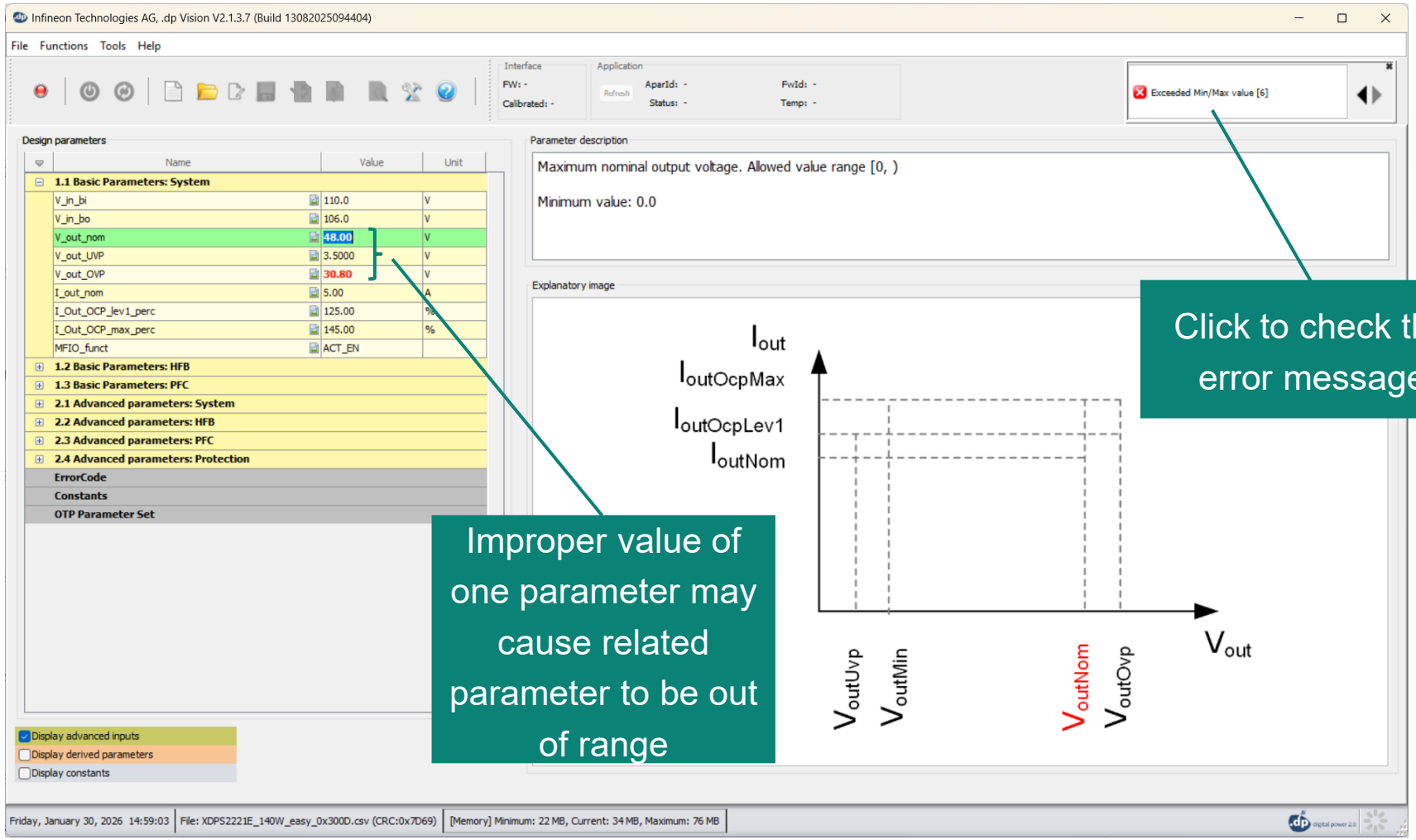
2 FW parameterization
- dpVision: Change parameter value

- Two options
  1. Change the value directly
     - Change the parameter value
     - Enter
  2. Import value
     - From an existing .csv file
     - From a .txt file (V2.1.3.7 feature)
     - Detailed procedure on the next page

- Colour of value
  - **Bold and blue**: value successfully changed
  - **Red**:
    - out of range, then impossible to Test or Burn configuration
    - Check the upper-right message box for information



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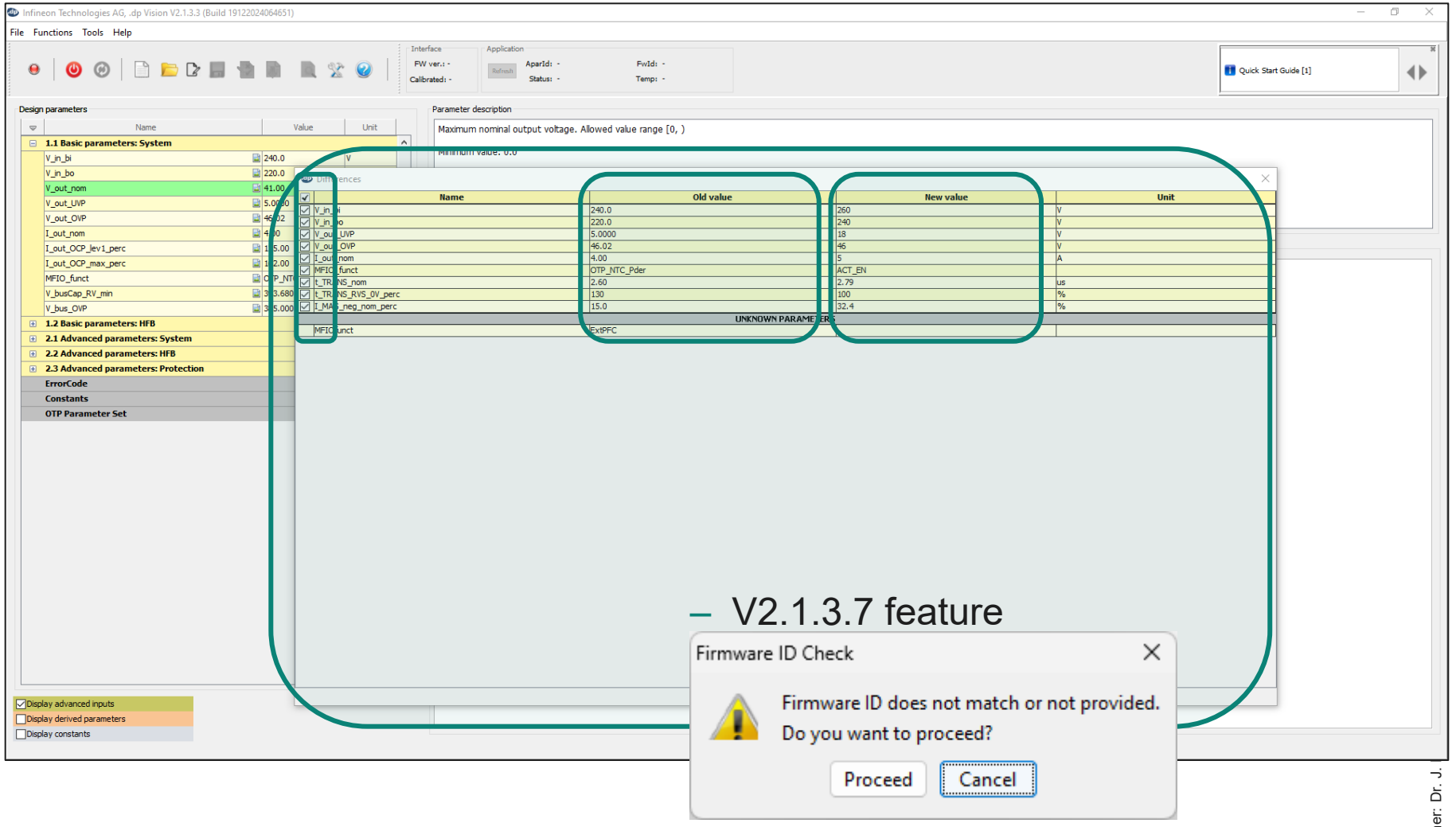
2 FW parameterization
- dpVision: Import of parameter value

1. One working .csv file already loaded into the dp vision GUI
2. Select “File” -> “Import”
3. Select the source file for parameter value import
   - A .csv file, or
   - A .txt file coming from design sheet (V2.1.3.7 only)
4. Check the to be imported parameters at the left side
5. Verify change
6. Proceed



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Design Flow
- Overview

1. System design & hardware preparation
   - Input
     - Application specific parameters
     - Design intention
   - Outcome as proposal
     - Hardware value
     - .csv parameters

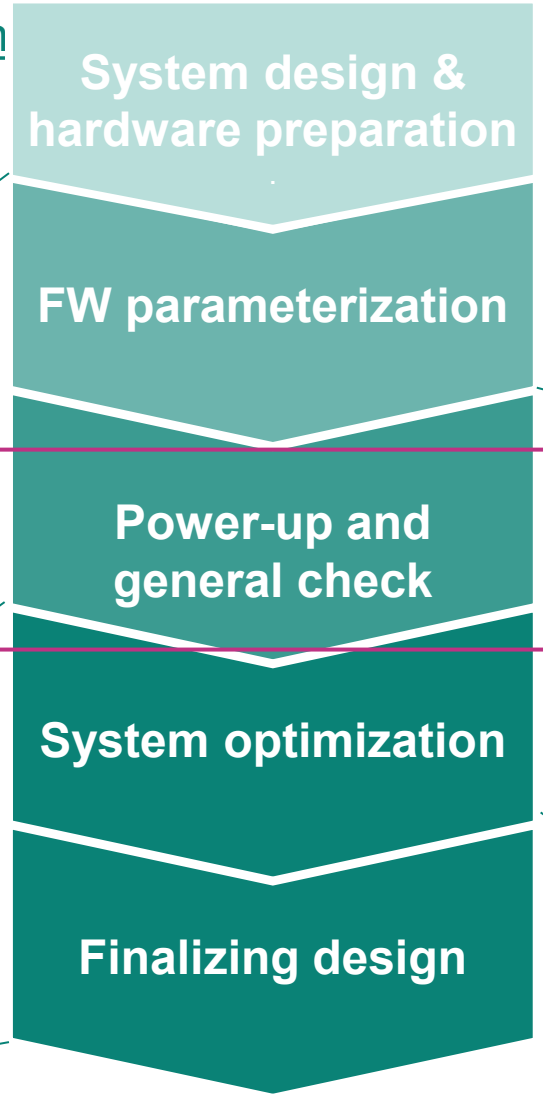




3. First power-up and general tests
- First system cold power-up
- General operation check

5. Finalizing the design
   - Fix hardware
   - Burn .csv parameters
   - Production release





2. FW parameterization
   - Interface board required
   - dpVision tool, .csv file and images required
   - FW parameter value update in dpVision
   - Download parameter value to IC



4. System optimization
   - Hardware update
   - Parameter finetune
     - To achieve desired performance and operating behavior
     - Individual protection settings



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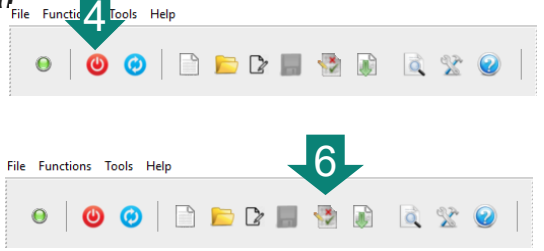
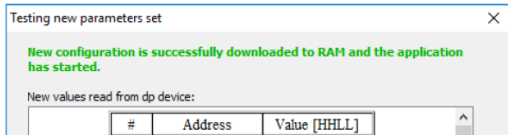
2 FW parameterization
- Procedure for *Test Configuration Set*

- ***Test Configuration Set***
  - Storing the whole parameter set into RAM. This parameter value set gets lost once V_{VCC}<V_{VCCoff}, for example after auto-restart, then the IC operates with value in the OTP afterwards
  - Used during board debugging or performance improvement
- Precondition for the configuration test and burn
  - Power board assembled with the specific IC
  - Board properly connected to
    - AC source with a proper voltage, but keep it off
    - DC load with proper mode and value, be either on or off
    - Interface board connected to computer and IC int
  - dpVision tool properly installed
  - The specific .csv file and the images file properly stored

- Required sequence for ***Test Configuration Set***
  1. Load the working .csv file
  2. Set the value properly
  3. Save the .csv file, *optional*
  4. ***Power on*** device
  5. Turn on the AC source
  6. ***Test Configuration Set***



- After these steps, the following message box shown and the IC/power board starting its operation with the new RAM parameter set



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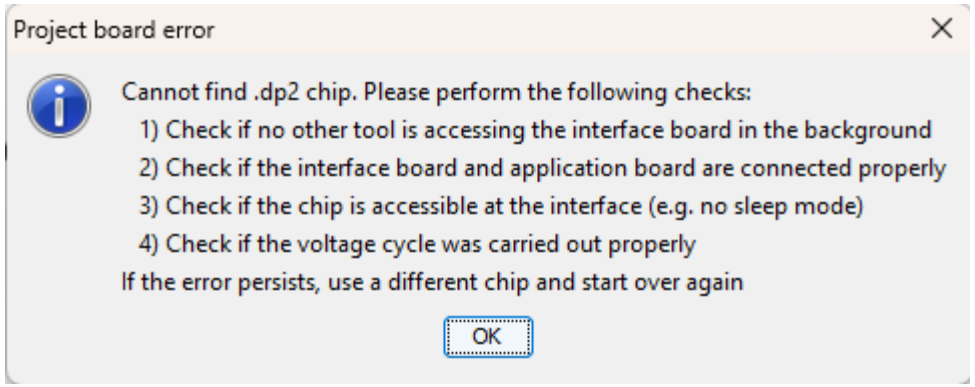
2 FW parameterization
- Error message at power-on device

– Error message box appearing at **power-on device** after a previous **power-on device** activity



– Error coming from the failed VCC cycles at the **power-on device** the controller IC

– Solution
  – Power-on device after a few seconds

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3 Power-up and General Tests
- Check points

- VCC check points
  - Proper VCC initial charge-up
  - V_{VCC} stable after some operation time

- HFB operation check points
  - HFB switching
  - HFB output voltage stable
  - System in burst mode operation at no load
  - Mode transfer at different load condition

- PFC operation check points in case of combo controllers used
  - PFC switching
  - Bus voltage level and stability

  - Information: Difference between XPDS2221E and XDPS2221/XDPS2222
    - XDPS2221 / XDPS2222: the HFB stage starting first, PFC start-up operation only on request based on the input and output conditions, such as input and output voltage, and output power
    - XDPS2221E: both PFC and HFB start operation at the same time; further PFC operation depending on the input and output conditions, such as input and output voltage, and output power

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3 Power-up and General Tests
- Cold start-up (1/2)

– System start-up without load:

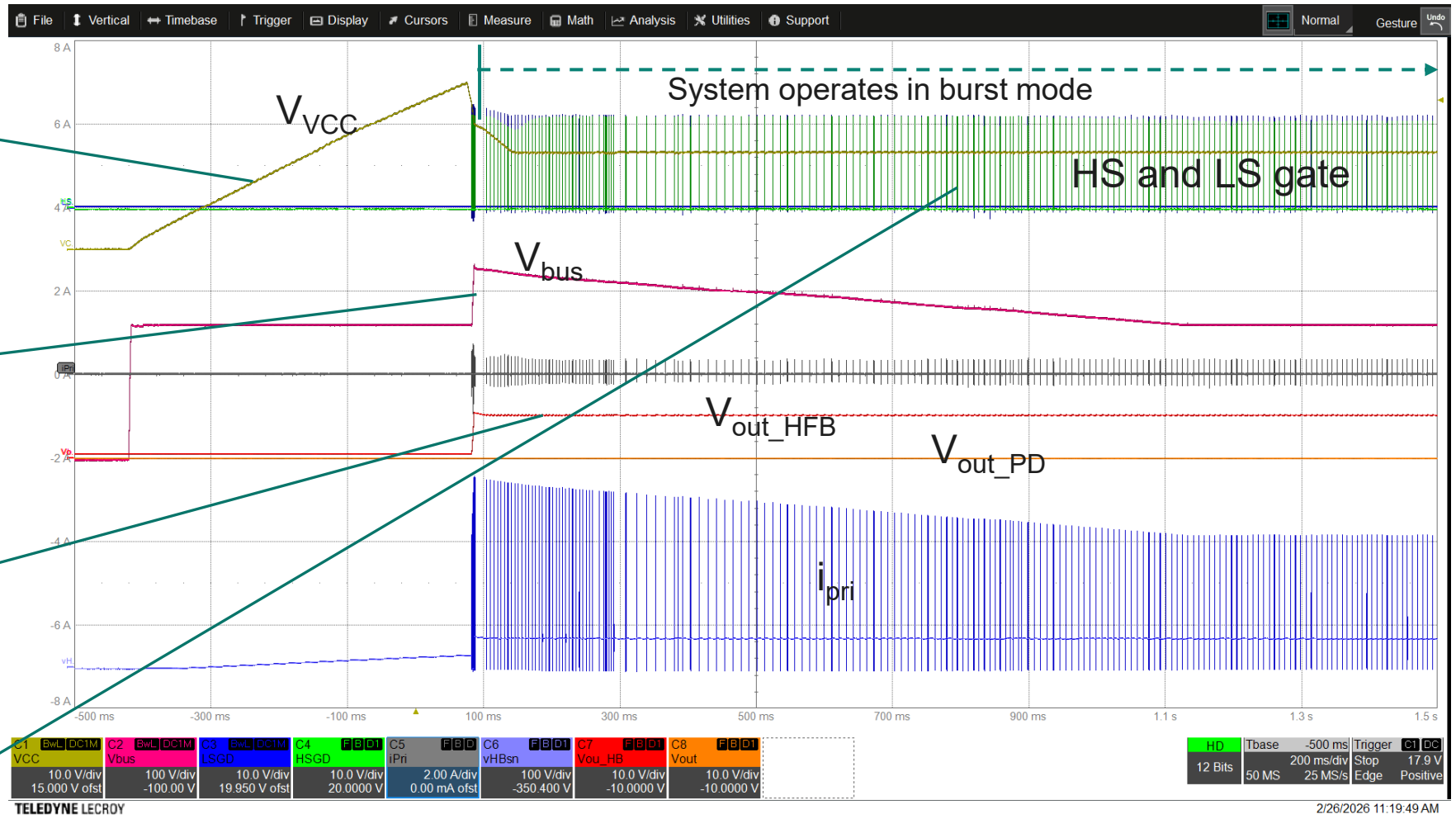
Proper V_{VCC} charge up and stable level after some operation time

PFC operates and bus voltage arises at very beginning

Stable HFB output voltage

Stable burst mode operation

Operating waveforms from an XDPS2221E 120 W 3-C board



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3 Power-up and General Tests
- Cold start-up (2/2)

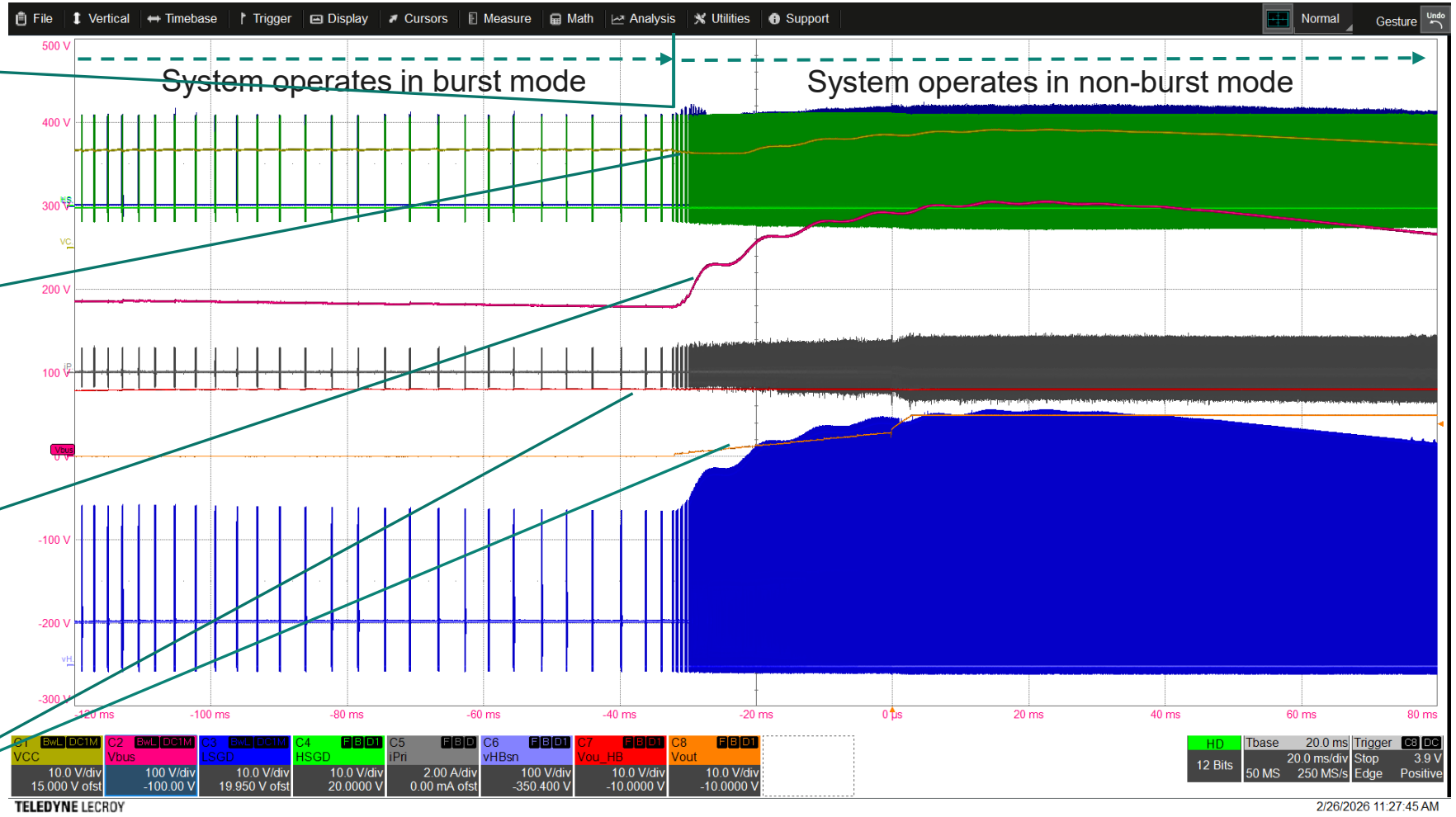
PD load switch enabled

Operation mode changed

PFC operation started and bus voltage regulated

Stable HFB output voltage & PD output enabled/regulated

Operating waveforms from an XDPS2221E 120 W 3-C board



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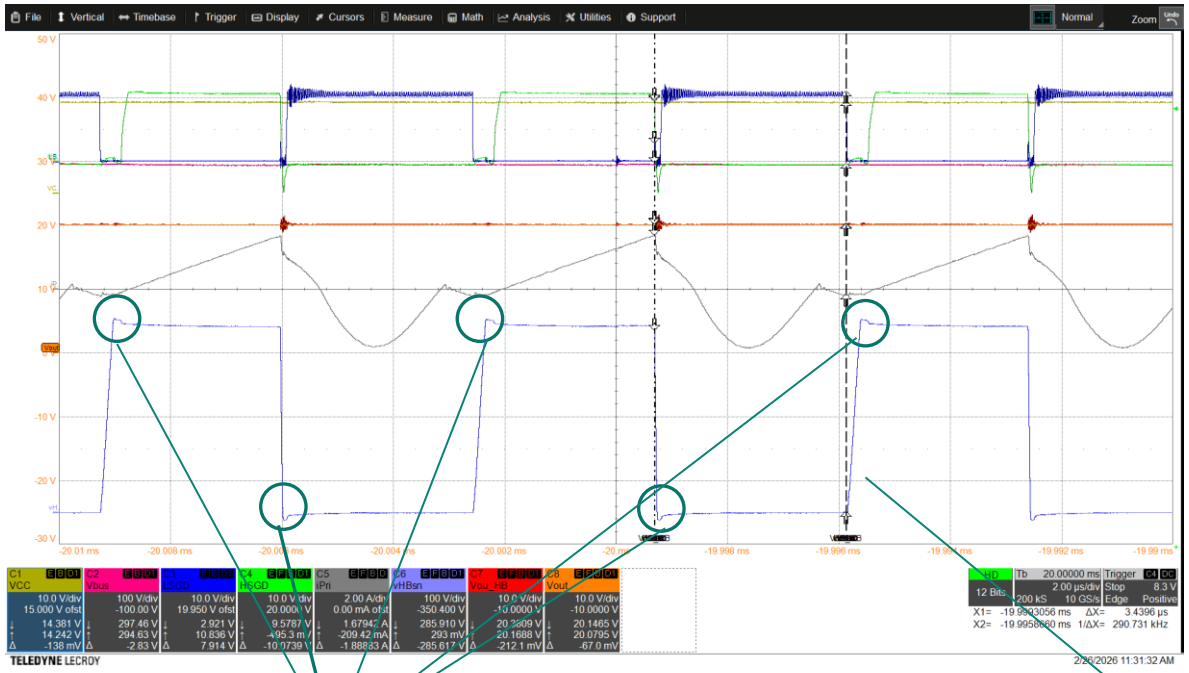
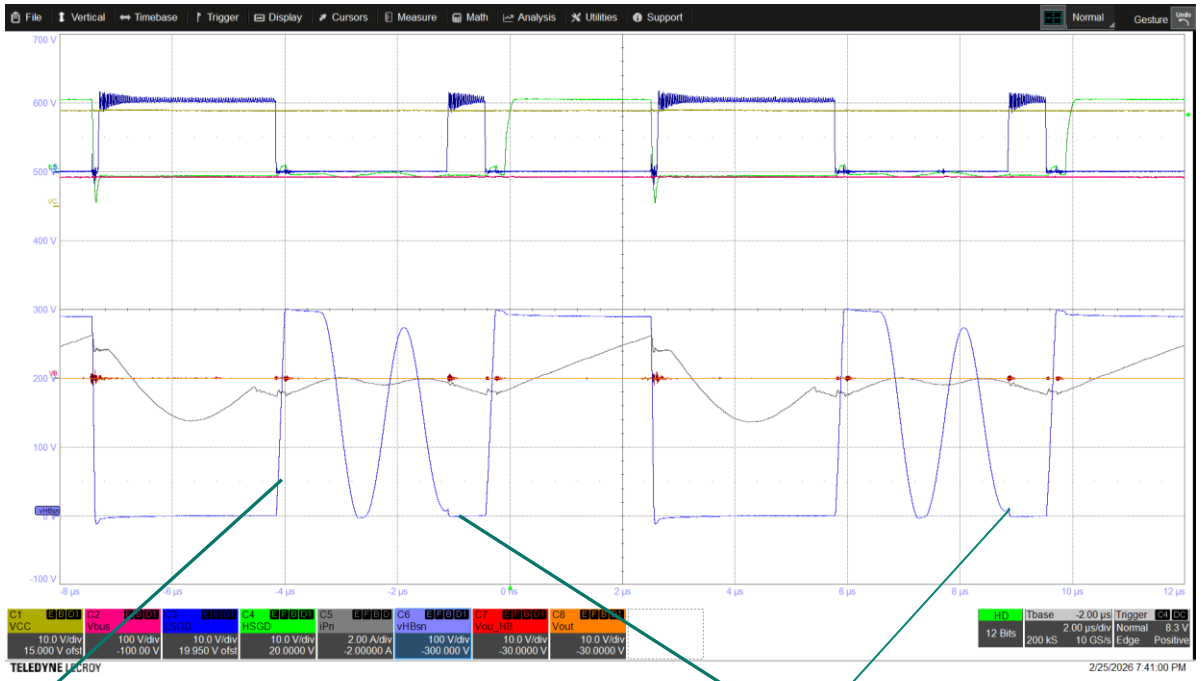
3 Power-up and General Tests
- Mode transfer and key information

Operating waveforms from an XDPS2221E 120 W 3-C board

– CRM at nominal load 20 V 5A



– ZV-RVS at 20 V 2 A



Voltage over- and undershoot = ZVS turn-on and enough current; Good timing

CRM in full load and ZV-RVS in partial load

Valley turn-on of the ZVS pulse

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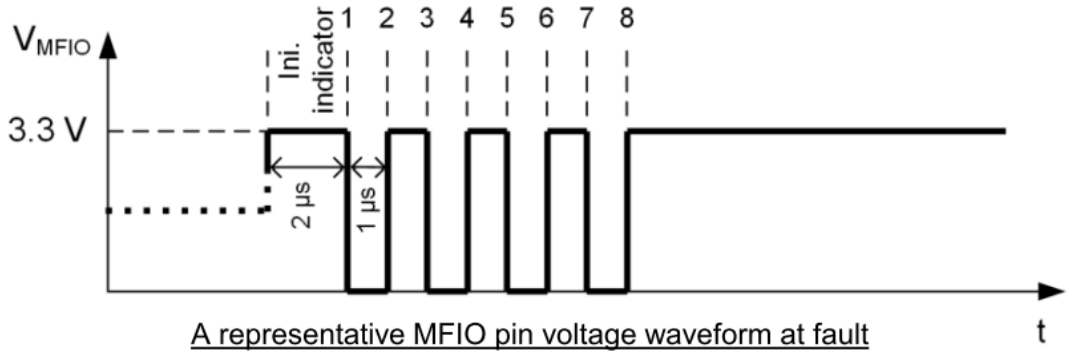
3 Power-up and General Tests
- Error code at MFIO pin

- If a protection triggered, the corresponding error code (EC) sent out at the MFIO pin
- The error code
  - Starting with an initial indicator of a logic-high pulse of 2 µs
  - Followed by pulse(s) with width of 1 µs
  - EC = total number of the rising and falling edge of the pulse strain at the MFIO pin
    - One example: the waveform below indicating the EC of 8, related to the output maximum current protection
  - If the EC information integrated in the .csv file as constants, further explanation and possible root cause visible in dp Vision



A representative MFIO pin voltage waveform at fault

ErrorCode	
ErrorCodeReadout	0
BrownOutProtection_Avg	1
BrownOutProtection	2
CSpinShortProtection	3
OutputStartUpTimeoutProtection	4
MissingHFBZCDatStartUp	5
OutputOvervoltageProtection	6
OutputUndervoltageProtection	7
OutputMaximumCurrentProtection	8
OutputOvercurrentProtectionOCP1level1	9
BusUndervoltageProtection	11
ACovervoltageProtectionBusOVP	12
PeakOvercurrentProtectionOCP2	13
LowFBvoltageAtStartUp	14
ExternalOvertemperatureProtection	16
ExternalOvertemperatureProtectionAtStartUp	17
BusVoltageOutOfRangeAtStartUp	18
WatchdogTimeOut	19
CSpinOpenProtection	22
RAMparityProtection	23
VCCovervoltageProtection	25
HFBopenLoopProtection	26
VoutShortCircuitProtection	27
BusUndervoltageProtectionStartup	29

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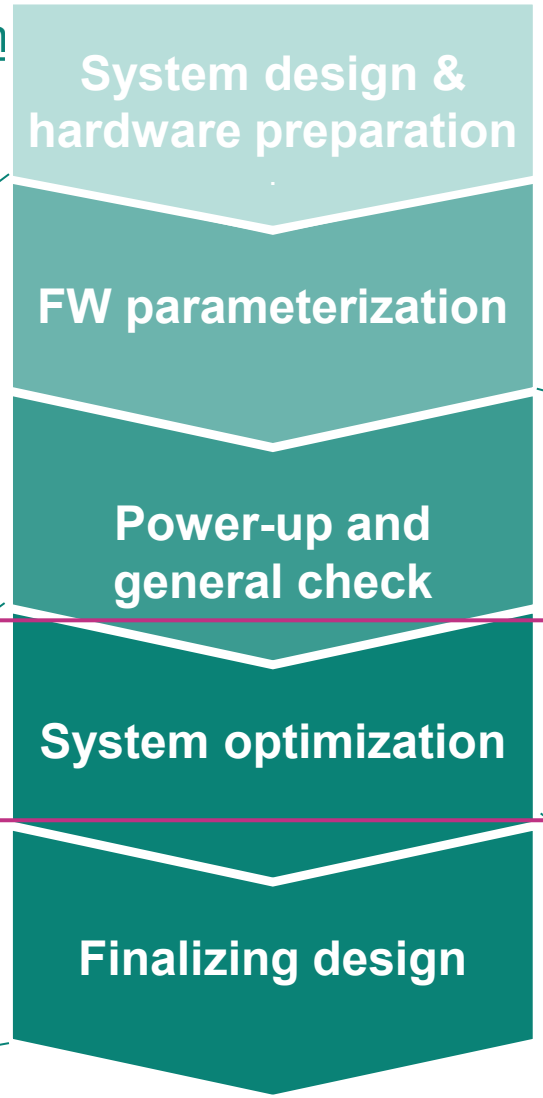

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4 System Optimization
- Overview

- Improving efficiency at nominal output
- Improving average efficiency
- PFC ZCD circuitry
- PFC transfer function

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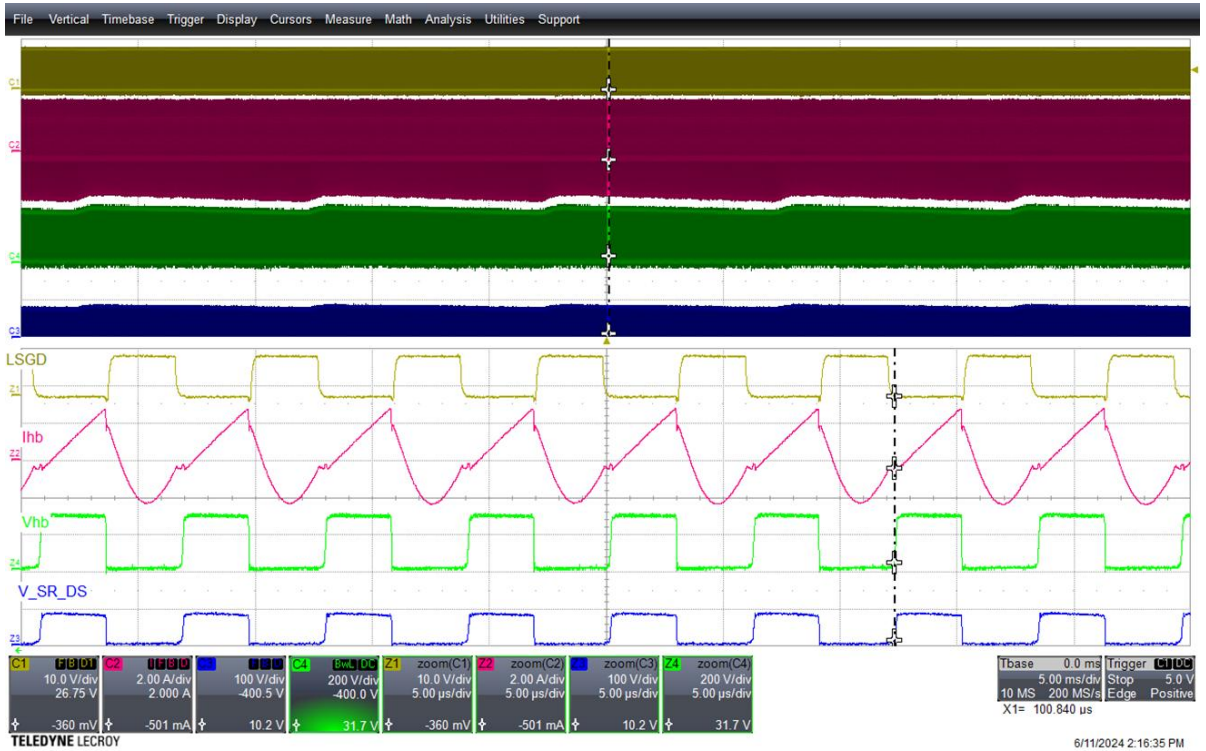
4 System Optimization
- Improving efficiency at nominal output

- Main parameters to improve the efficiency at the nominal output condition
  - $t_{TRANSnom}$
  - $I_{MagNegNomPerc}$
  - Capacitance of the resonant capacitor

- Step 1: tune the parameter $t_{TRANSnom}$
  - Signals to be checked: LSGD, Ihb, VSRDS, Vhb
  - Operating condition: V_{outnom}, I_{outnom}
  - Goal: just enough negative current for zero-voltage turn-on for the highside switch
  - Adjusting parameter $t_{TRANSnom}$
    - Too short $t_{TRANSnom}$ ➔ cut resonance and therefore high voltage spike across the SR switch
    - Too long $t_{TRANSnom}$ ➔ worse efficiency and voltage spike across the SR switch



C1: LSGD C2: I_{hb} C3: $V_{SR,DS}$ C4: V_{hb}

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4 System Optimization
- Improving efficiency at nominal output

- Step 2: tune the parameter $I_{MagNegNomPerc}$
  - Signals to be checked: LSGD, Ihb, VSRDS, Vhb
  - Operating condition: V_{outnom}, I_{outnom}
  - Goal: Calculated $I_{MagNegNom}$ matching the measured negative current
  - Adjusting parameter $I_{MagNegNomPerc}$
    - Too high value ➔ negative impact on efficiency and load current capability

$$I_{outNom} = N * \frac{I_{MagPosNom} + I_{MagNegNom}}{2}$$

    - Too low value ➔ risk of non-ZVS
      - Negative current between 0.3 A – 0.5 A for Silicon switches and lower value for GaN devices

	1.2 Basic parameters: HFB		
	Switch_type	Si	
	t_ls2zcd	500.000	ns
	N	3.60	
	Iset_nom_perc	48.05	%
	Rshunt_HFB	0.0945	Ohm
	t_TRANS_nom	2.60	us
	t_TRANS_RVS_0V_perc	130	%
	t_TRANS_RVS_0V	3.4	us
Tune	I_MAG_neg_nom_perc	15.0	%
	I_MAG_pos_nom	2.55	A
Measure	I_MAG_neg_nom	0.33	A
	I_MAG_neg_max_perc	40.0	%
	I_MAG_neg_max	0.89	A

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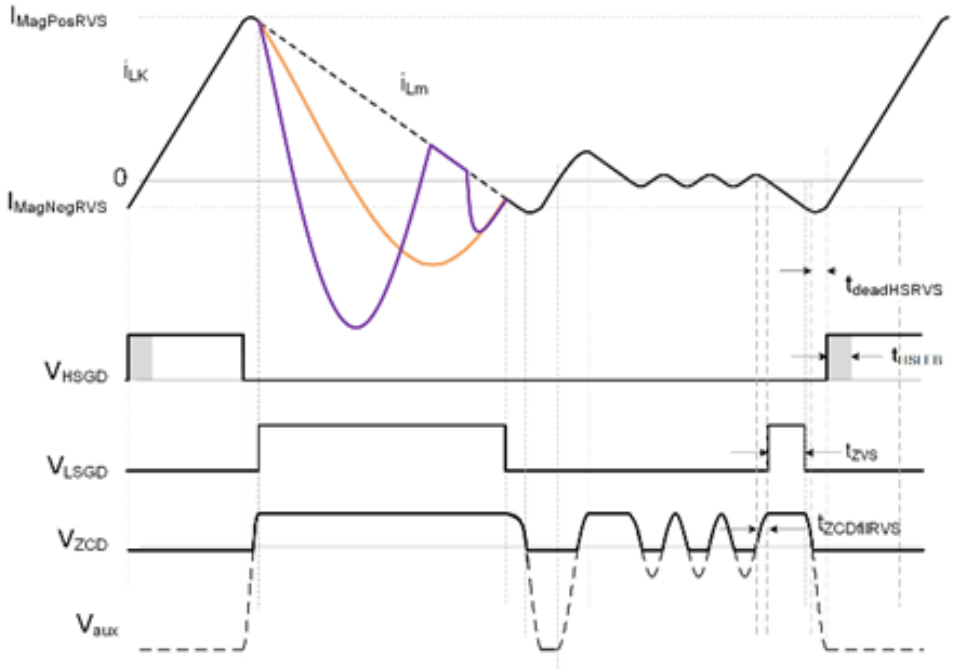
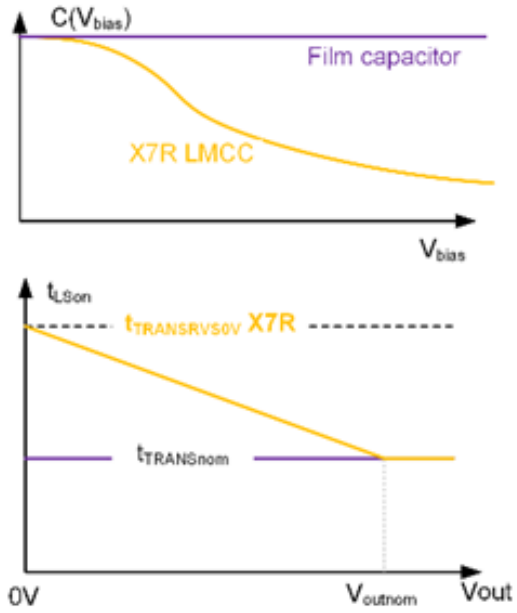
4 System Optimization
- Improving efficiency at nominal output

- Step 3: check the resonant capacitor
  - Signals to be checked: LSGD, Ihb, VSRDS, Vhb
  - Operating condition: V_{outnom}, I_{outnom}
  - Goal: Ensuring a complete half-resonance during low-side on-time
  - Checking the primary current during lowside on-time and changing the resonant capacitance for
    - No cut resonant curve
    - No double resonant curve
    - Resonant current crossing the magnetizing current possibly close to the lowside gate turn-off point
  - Set parameter $t_{TRANSRVS0Vperc}$ according to the type of the used capacitor





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4 System Optimization
- Overview

- Improving efficiency at nominal output
- Improving average efficiency
- PFC ZCD circuitry
- PFC transfer function

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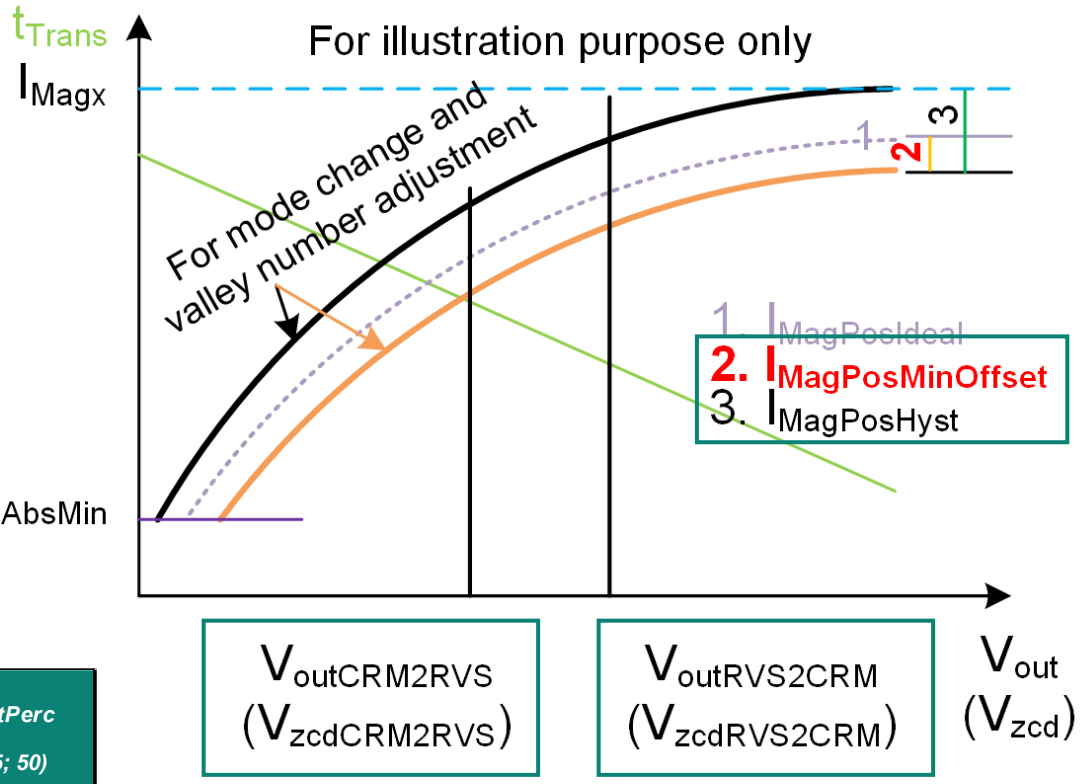
4 System Optimization
- Improving average efficiency

- Average efficiency mainly related to
  - Set points for the operation mode transition between ZV-RVS and CRM: helpful with lower output current at the transition from ZV-RVS to CRM
  - Proper SR operation: no mis-triggering in ZV-RVS operation

- Four parameters for the mode transition
  - Output voltage thresholds $V_{outCRM2RVS}$ and $V_{outRVS2CRM}$
  - Output current parameters $I_{MagMinOffsetPerc}$ and $I_{MagPosHystPerc}$ $I_{MagPosAbsMin}$
  - Minimum of the positive peak current $I_{MagPosRvsAbsMinPerc}$
  - Influence of these parameters

	$V_{outCRM2RVS}$	$V_{outRVS2CRM}$	$I_{MagMinOffsetPerc}$ (5 - 10)	$I_{MagPosHystPerc}$ (12.5; 25; 37.5; 50)
RVS to CRM transition at a lower output current	decrease	decrease	increase	decrease
RVS to CRM transition at a higher output current	increase	increase	decrease	increase



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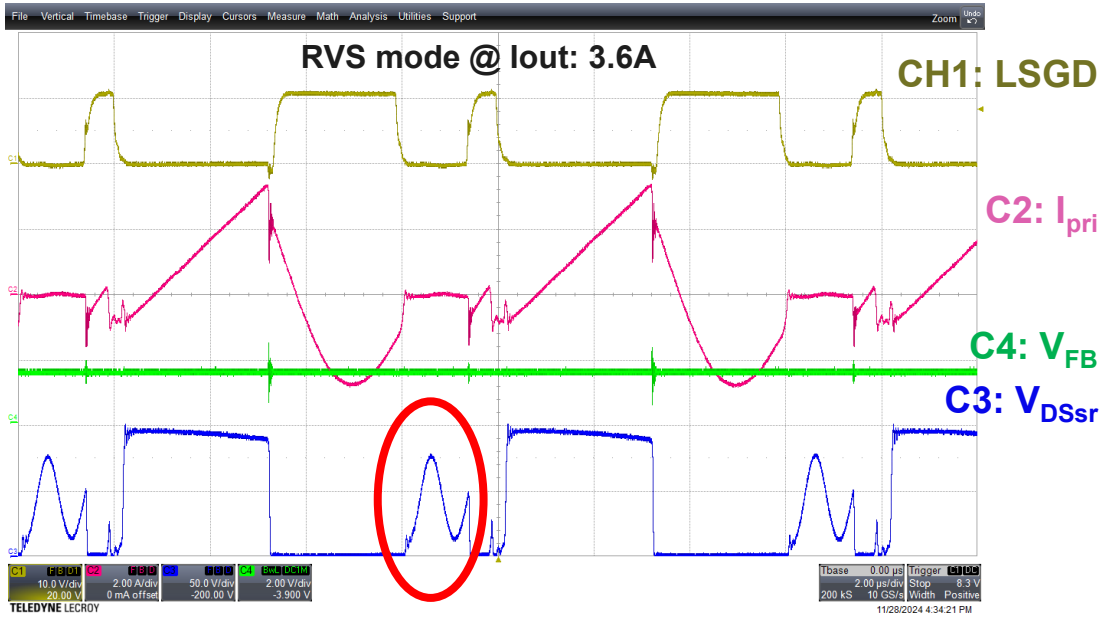
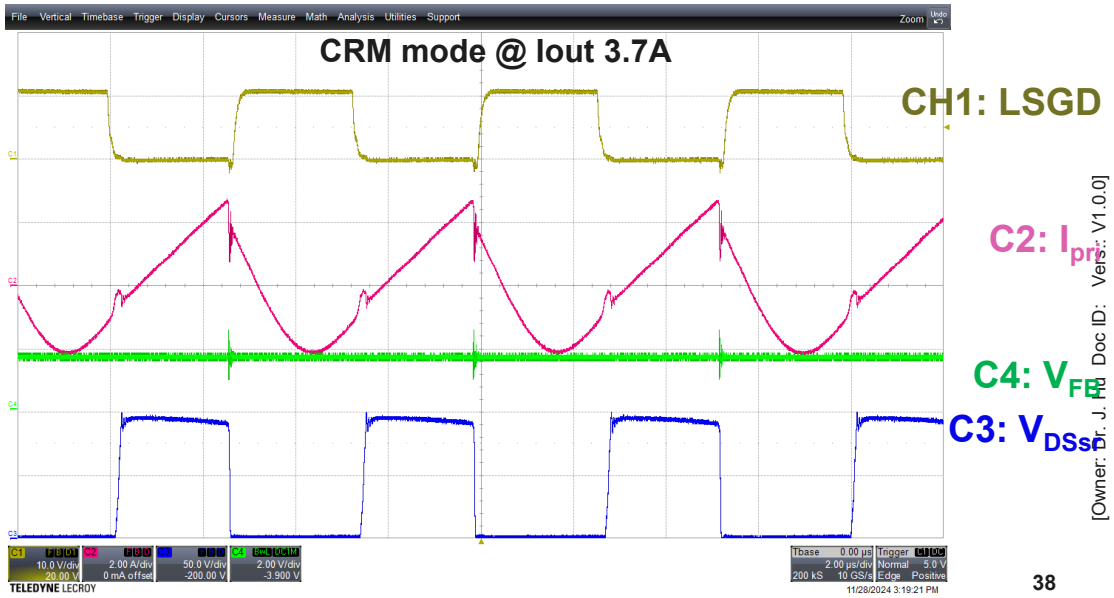
4 System Optimization
- Improving average efficiency

- Fine tune example
  - Performed on the 170W BPA reference design
- Starting point
  - CSV-Parameters:
    - $I_{MAGposHystPerc}$: 37.5%
    - $I_{MAGposRVSabsMinPerc}$: 40%
    - $I_{MAGminOffsetPerc}$: 5.0%
    - $V_{outCRM2RVS}$: 14.00 V
    - $V_{outRVS2CRM}$: 16.00 V
  - Observations at 230 Vac and 41 Vout
    - RVS to CRM transition at 3.7 A load
    - Miss-triggering of SR-FET in RVS mode
- Fine tune
  - $I_{MagPosHystPerc}$ 37.5% ➔ 20%
    - Lower current at transition to CRM operation
  - $I_{MagPosRvsAbsMinPerc}$ 40% ➔ 50%
    - SR miss-triggering avoided
  - ZV-RVS to CRM transition: 3.7 A ➔ 3.3 A





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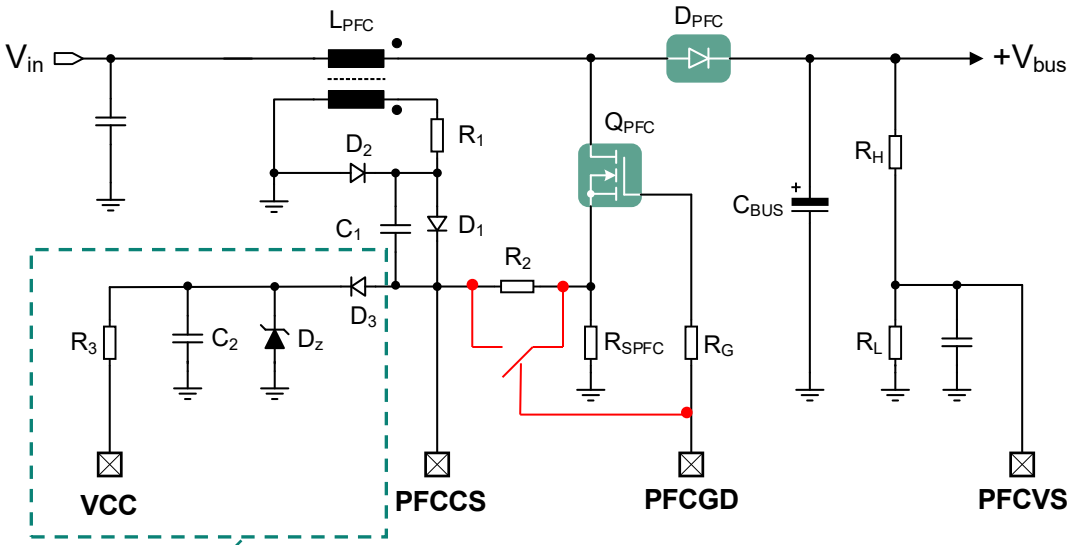
4 Optimization
- PFC ZCD circuitry with discrete switch

Case 1: PFC switch without OCP



Voltage clamping circuitry

- A by-pass switch mandatory for PFC OCP
  - In parallel to R2 and Controlled by PFC gate
  - Low Qg device, i.e., 2N7002
- Design steps
  - Dimension of the voltage clamping circuitry to ensure PFCcs pin voltage below its maximum
  - Select the ratio of $R_2/(R_1 + R_2)$ to ensure the amplitude for proper ZCD at the peak of the maximum AC voltage
  - Choose the C1 and R1 for proper ZCD signal amplitude
  - Select the R1 as high as possible to minimize the power losses

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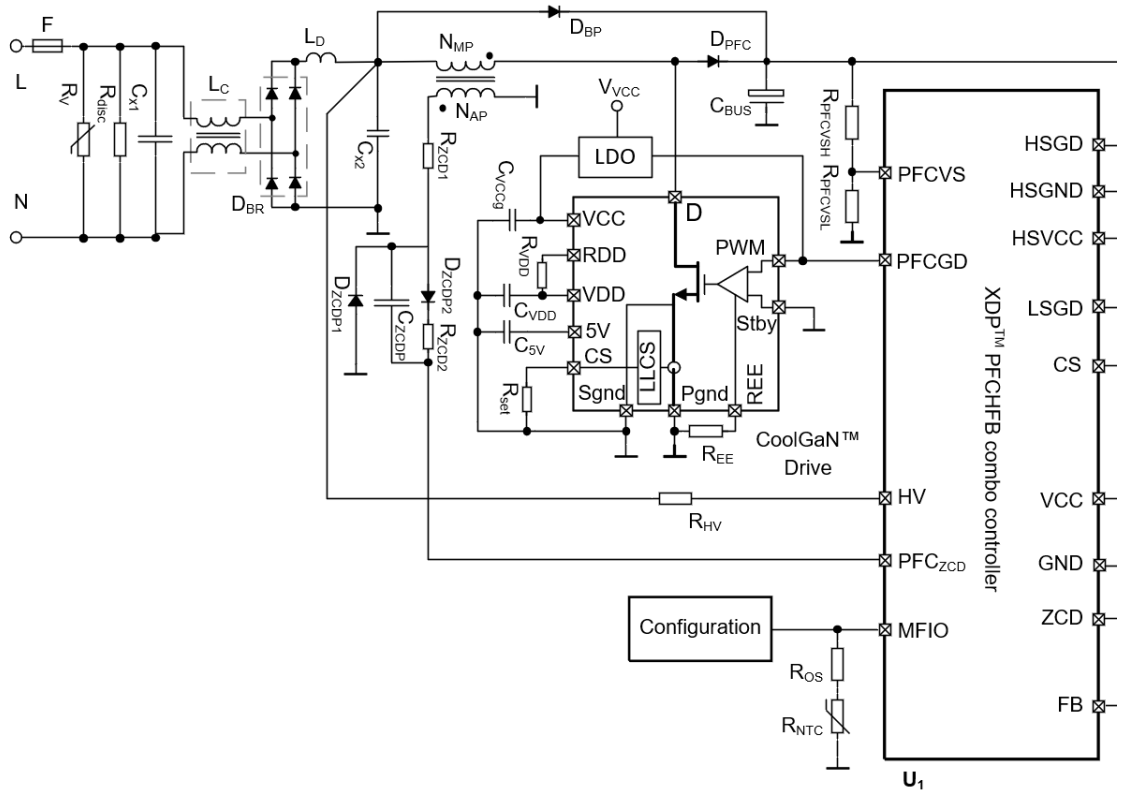
4 Optimization
- PFC ZCD circuitry with CS-integrated switch

Case 2: PFC switch with OCP, **XDPS2221E feature!**



- PFC OCP by the CoolGaN™ Drive Single device
  - OCP level set by R_{set}
- Only ZCD function for PFCcs pin
- Design approach for ZCD circuit
  - Select the proper value of R_{ZCD1} and R_{ZCD2} to keep the I_{ZCD} current under the rated value of 2.5 mA
  - Choose the C_{ZCDP} and R_{ZCD1} / R_{ZCD2} for proper ZCD
    - Lower R_{ZCD2} or higher C_{ZCDP} leading to
      - Higher ZCD oscillation amplitude
      - Less phase shift of the oscillation
  - Select R_{ZCD1} and R_{ZCD2} as high as possible to minimize the losses during the demagnetizing time of the PFC choke
  - $$P_{Rzcdmax} = \frac{\left(\frac{V_{bus} * N_{AP}}{N_{MP}}\right)^2}{R_{zcd1} + R_{zcd2}}$$

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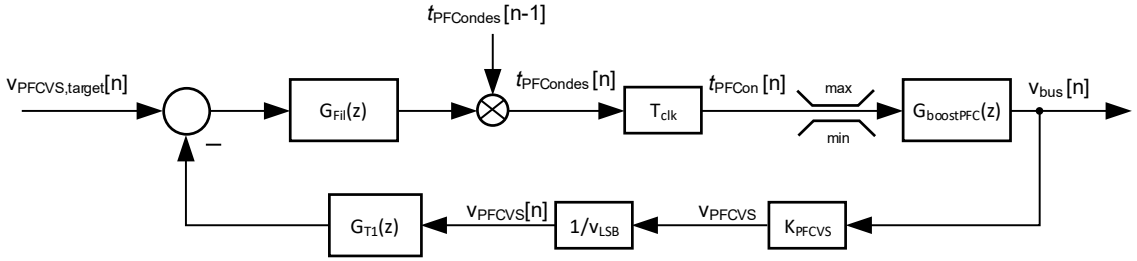
4 Optimization
- PFC transfer function and its parameters

– PFC digital control loop



7.7 PFC control parameters					
PFC_CoefA	256.0				256
PFC_CoefB	822.0				822
PFC_CoefT1	5.0				5

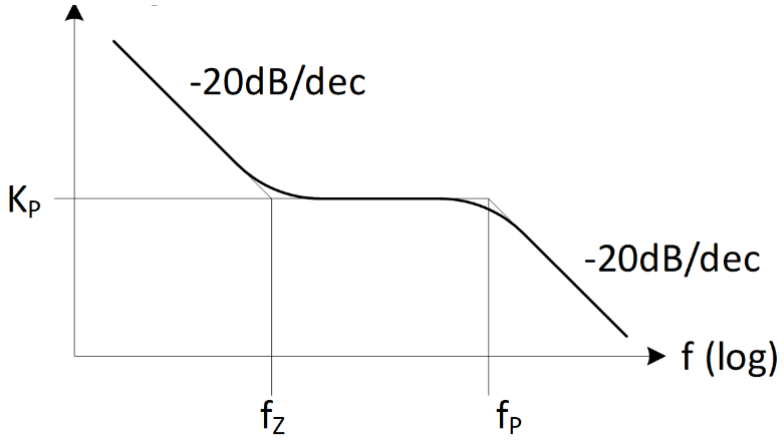
– Open loop gain of the PFC stage with the PIT1 regulator

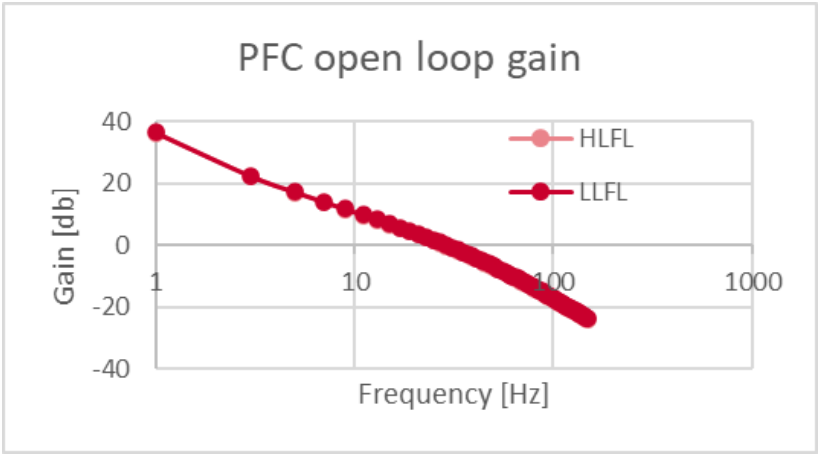
$$\frac{P_{PFC}}{\bar{V}_{bus}} \cdot \frac{1}{sC_{PFC}} \cdot K_P \cdot \frac{1+\frac{2\pi f_Z}{s}}{1+\frac{s}{2\pi f_P}} \quad \text{with}$$

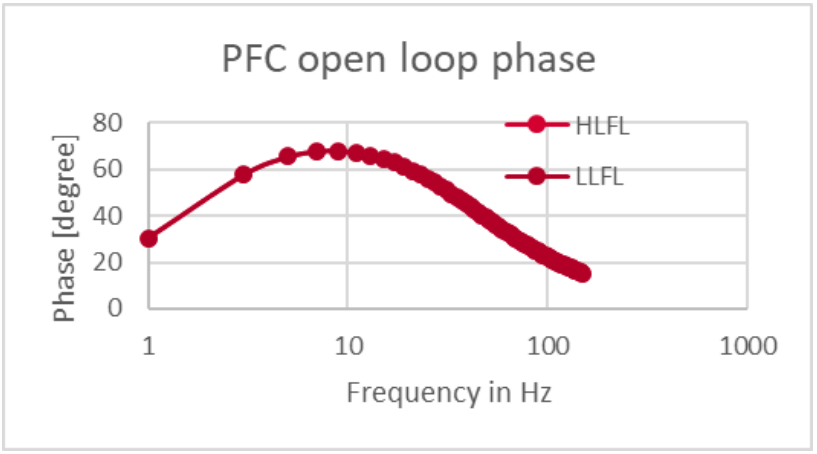
$$f_Z = \frac{\boldsymbol{PFC_{CoefA}}}{256 \cdot 2\pi \cdot 120\mu s \cdot \boldsymbol{PFC_{CoefB}}}$$

$$f_P = \frac{1}{2\pi \cdot 120\mu s \cdot \left(2^{\boldsymbol{PFC_{CoefT1}}} - 1\right)}$$

$$K_P = \frac{2^{-16} \cdot \boldsymbol{PFC_{CoefB}}}{\frac{2.8333V}{1791}} \cdot k_{PFCVS}$$







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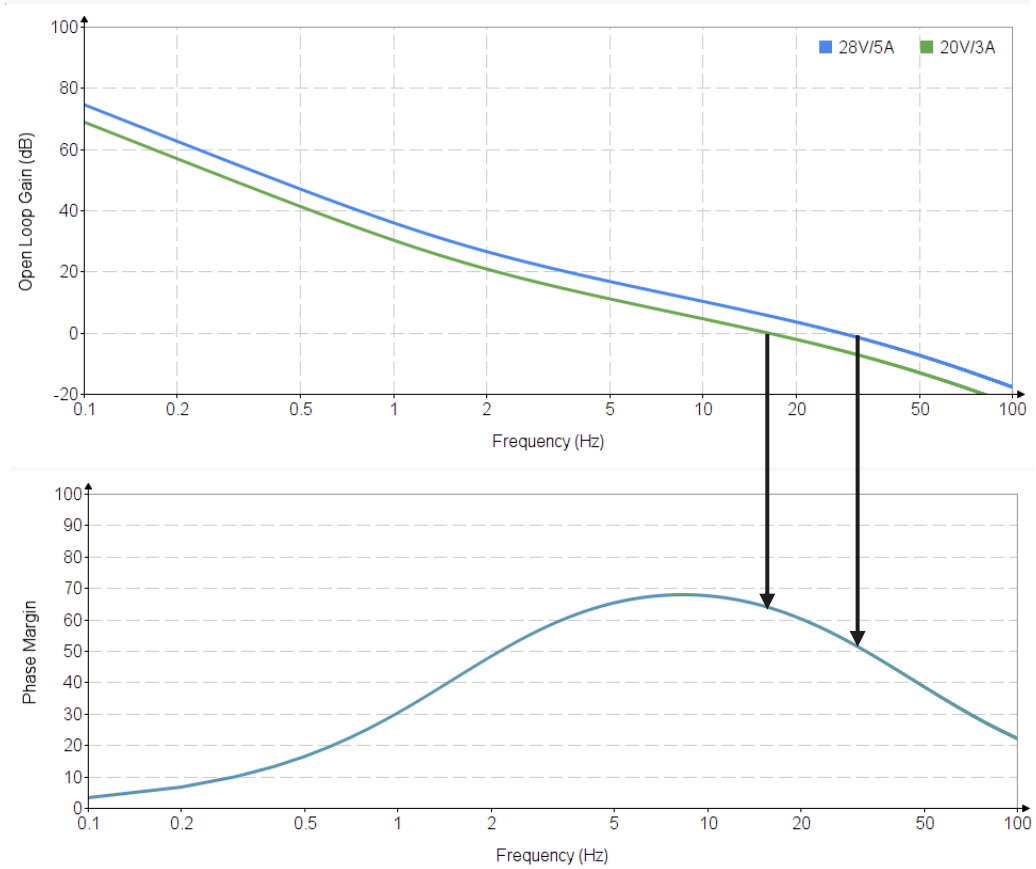
4 Optimization
- PFC transfer function

- Design steps
  - Set PFCCoefT1 to have at least 20dB suppression at the double mains frequency at the full load to reduce the bus voltage ripple
  - Set PFCcoefB and PFCcoefA to have
    - fz below 5 Hz
    - phase margin is between 45 and 60 degree

- Recommended value range in tracking
  - 128 ≤ PFCCoefB ≤ 2047
  - 256 ≤ PFCCoefA ≤ 2047
  - 4 ≤ PFCCoefT1 ≤ 6

- PFCCoefT1 parameter value [4, 5, 6, 7] correspond to filter time of [1.86, 3.78, 7.62, 15.30] ms. Smaller value for faster Vbus response



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Design Flow
- Overview

1. System design & hardware preparation
   - Input
     - Application specific parameters
     - Design intention
   - Outcome as proposal
     - Hardware value
     - .csv parameters

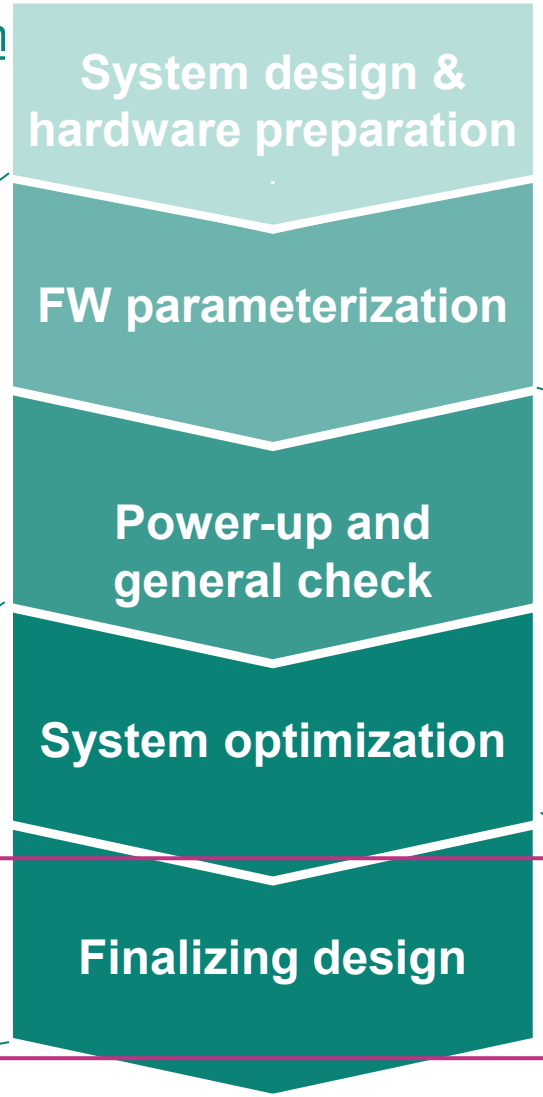




3. First power-up and general tests
   - First system cold power-up
   - General operation check

5. Finalizing the design
   - Fix hardware
   - Burn .csv parameters
   - Production release





2. FW parameterization
   - Interface board required
   - dpVision tool, .csv file and images required
   - FW parameter value update in dpVision
   - Download parameter value to IC



4. System optimization
   - Hardware update
   - Parameter finetune
     - To achieve desired performance and operating behavior
     - Individual protection settings



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5 Finalizing the design
- Recommended steps

- Three steps to finalize the design
  - Hardware
    - Check the component change
    - Update the related documents
  - Parameter
    - Save the used the utilized parameter to a file for production
    - Burn the parameter set to the IC
    - Start the final tests and confirm the performance
  - Board and parameter release for board production

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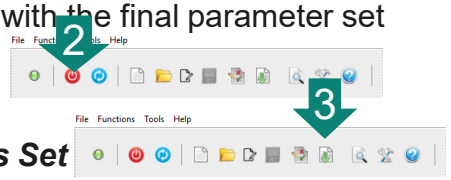
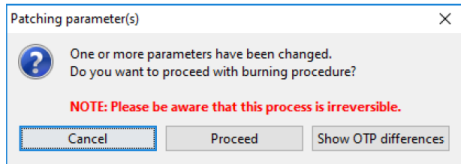
5 Finalizing the design
- *Burn Configuration Set* via dpVision

- Parameter burnt in OTP (one-time Programmable cell) per ***Burn Configuration Set***
- Procedure for ***Burn Configuration Set***
  - Recommended to test the configuration before burn the parameter
    1. Load the .csv file with the final parameter set
    2. ***Power on*** device
    3. ***Burn parameters Set***



Info: Burn configuration set button active only when the csv file has been saved!

Following message shown where it is possible to check the OTP difference:



With a successful burn process, a message box pops up with message about a successful parameter burn process. However, when burn the parameter on board with big VCC capacitor, the verification process may fail and then there is message about a failed burn process is shown. In this case, a second burn process is required.

4. Power off device and disconnect the interface board from the power board

- Once the parameter set burnt properly, then the IC starting its operation with the new parameter set at the next AC power-on
- ***Burn Configuration Set*** burning only the difference between the OTP content and the new APARAM set
- Limited times of ***Burn Configuration Set***
  - Depending on the number of related OTP bytes due to the parameter change
  - Most likely 8 ~ 20 times of parameter burn before the OTP getting fully used
  - Use the ***Test Configuration Set*** during board debugging and performance improvement to avoid frequent IC change on board
  - ***Burn Configuration Set*** only when necessary: meaning parameter change leads to protection triggered. Once a protection is triggered, the system operates with OTP parameter set after restart

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5 Finalizing the design
- Two options for burning FW and/or parameter

Business volume

3rd party service authorized by Infineon: FW+parameter burning for mass production

Please consult Infineon sales team

Interface board and dp vision:
Parameter burning during board evaluation

Interface board and dp OTP burner:
FW+parameter burning for small quantity board production

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