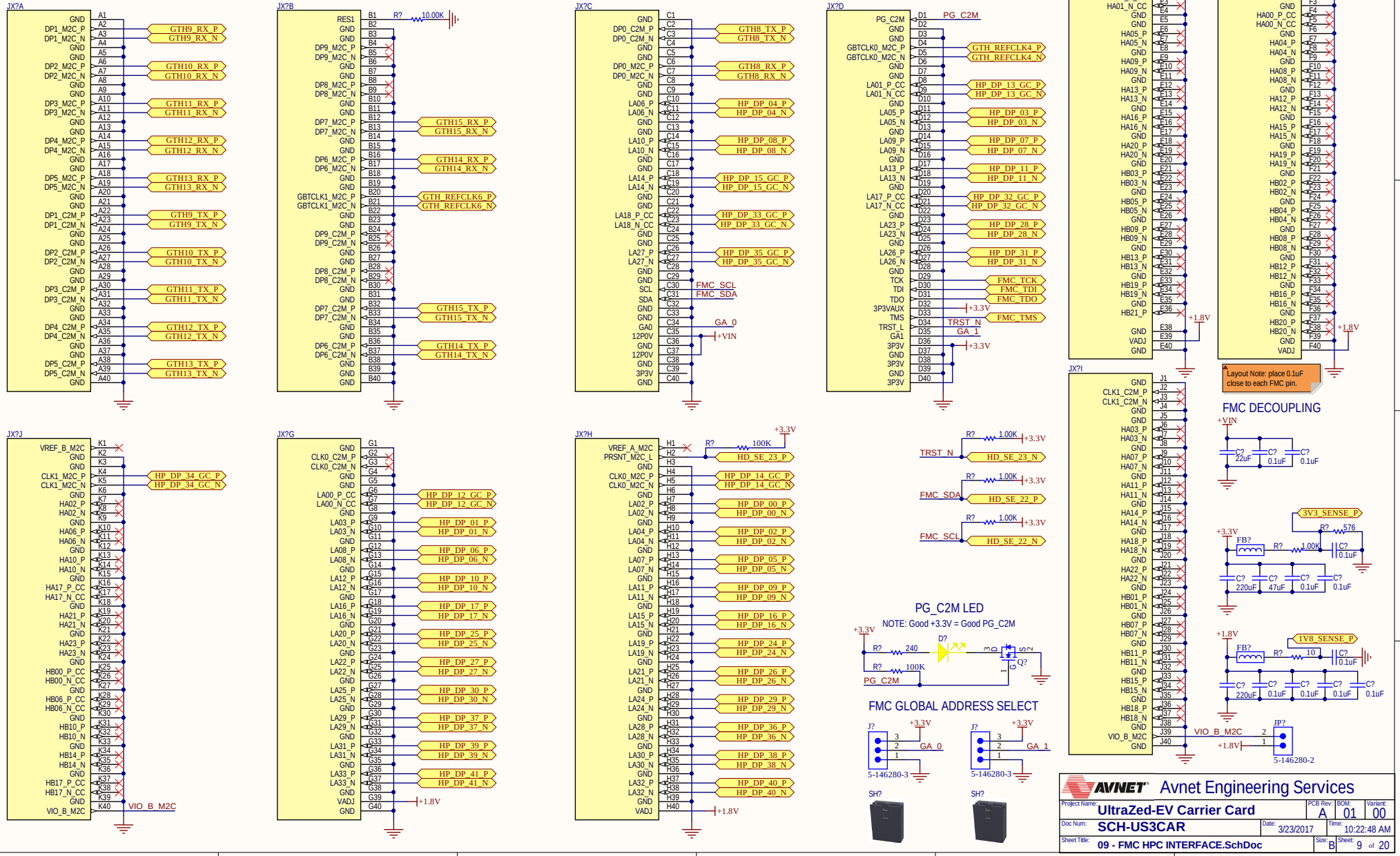
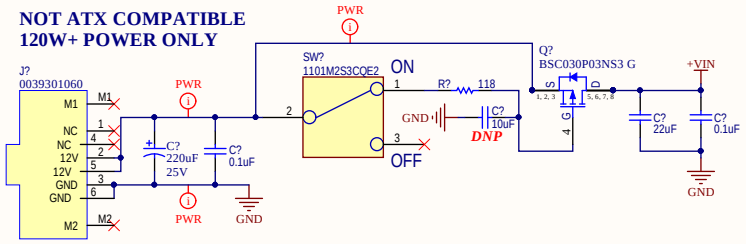
FMC HPC INTERFACE



POWER 1

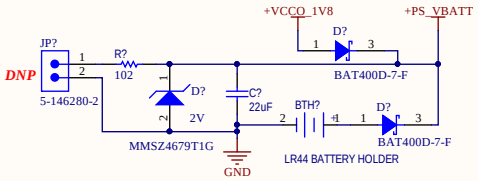
POWER INPUT

NOT ATX COMPATIBLE
120W+ POWER ONLY

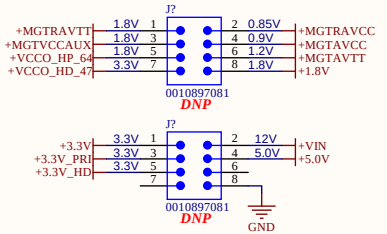


NOTE: NEW PINOUT FOR 120W+ PSU

+PS_VBATT_TEST

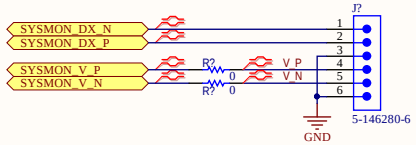


VOLTAGE MONITOR HEADERS

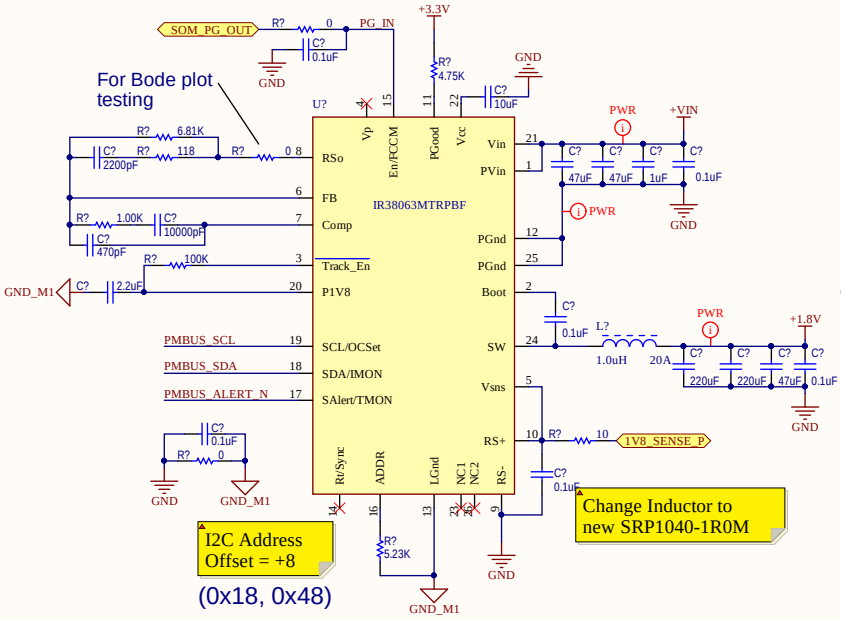


PMBUS_SCL
PMBUS_SDA
PMBUS_ALERT_N

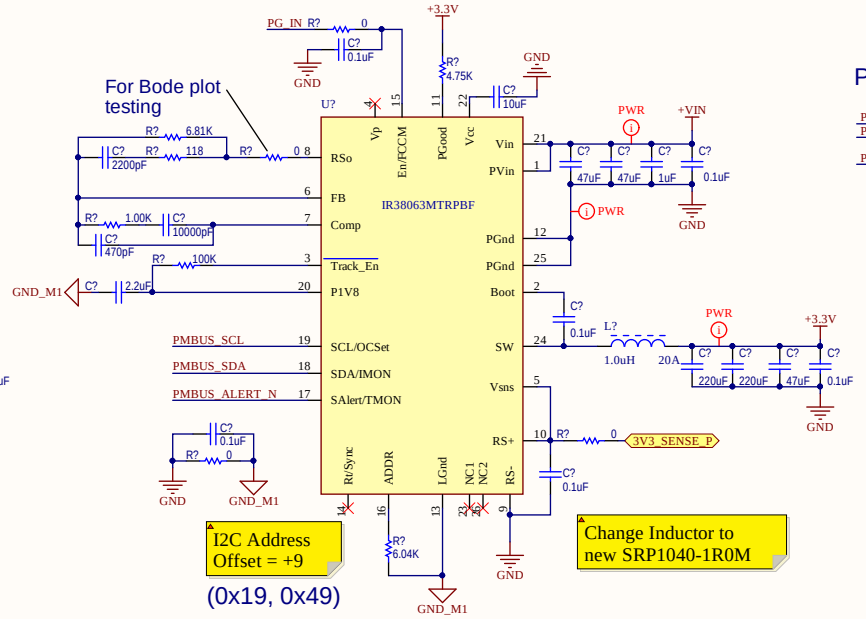
SYSMON HEADER



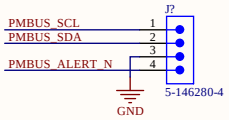
1.8V MAIN (HIGH CURRENT)



3.3V MAIN (HIGH CURRENT)

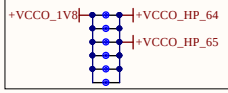


PMBus HEADER

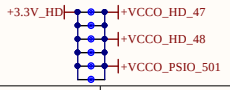


Layout Note: Net Ties at 0.5mm each. Tie as close as possible to each JX pin.

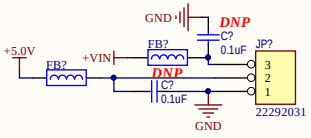
+1.8V NET TIES



+3.3V NET TIES



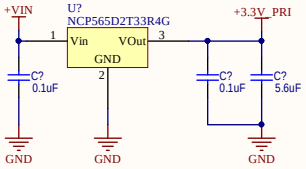
FAN HEADER

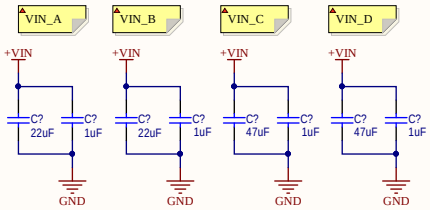


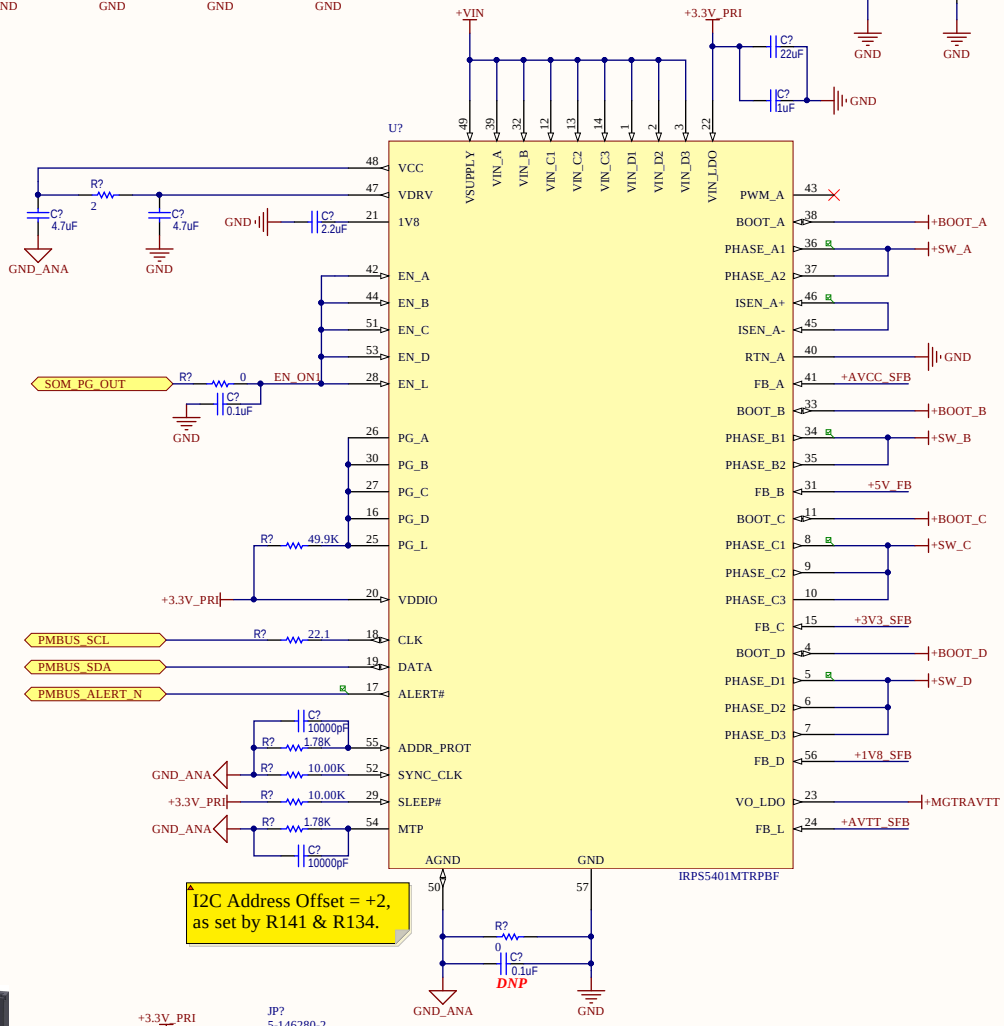
AVNET Avnet Engineering Services			
Project Name: UltraZed-EV Carrier Card	PCB Rev: A	BOM: 01	Variant: 00
Doc Num: SCH-US3CAR	Date: 3/23/2017	Time: 10:22:59 AM	
Sheet Title: 17 - POWER1.SchDoc	Size: B	Sheet: 17 of 20	

POWER 2

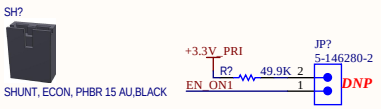
+3.3V PRIMARY REG



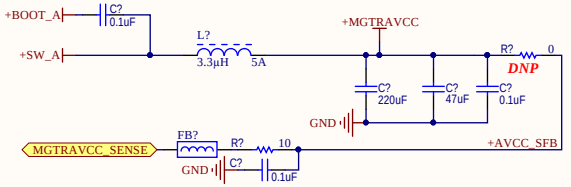




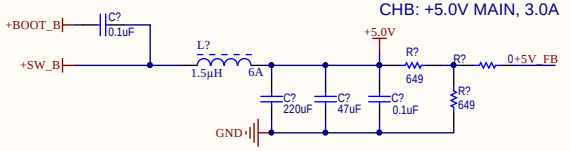
I2C Address Offset = +2, as set by R141 & R134.



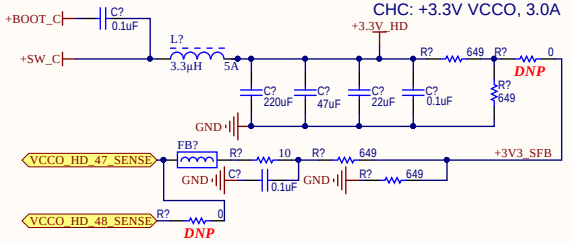
CHA: +0.85V MGTRAVCC, 2.0A



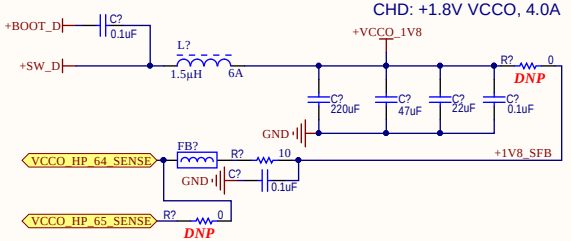
CHB: +5.0V MAIN, 3.0A



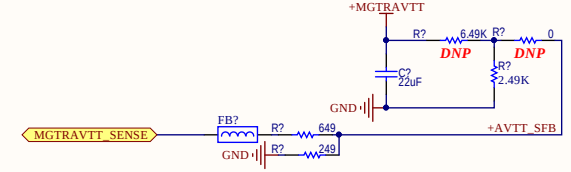
CHC: +3.3V VCCO, 3.0A



CHD: +1.8V VCCO, 4.0A

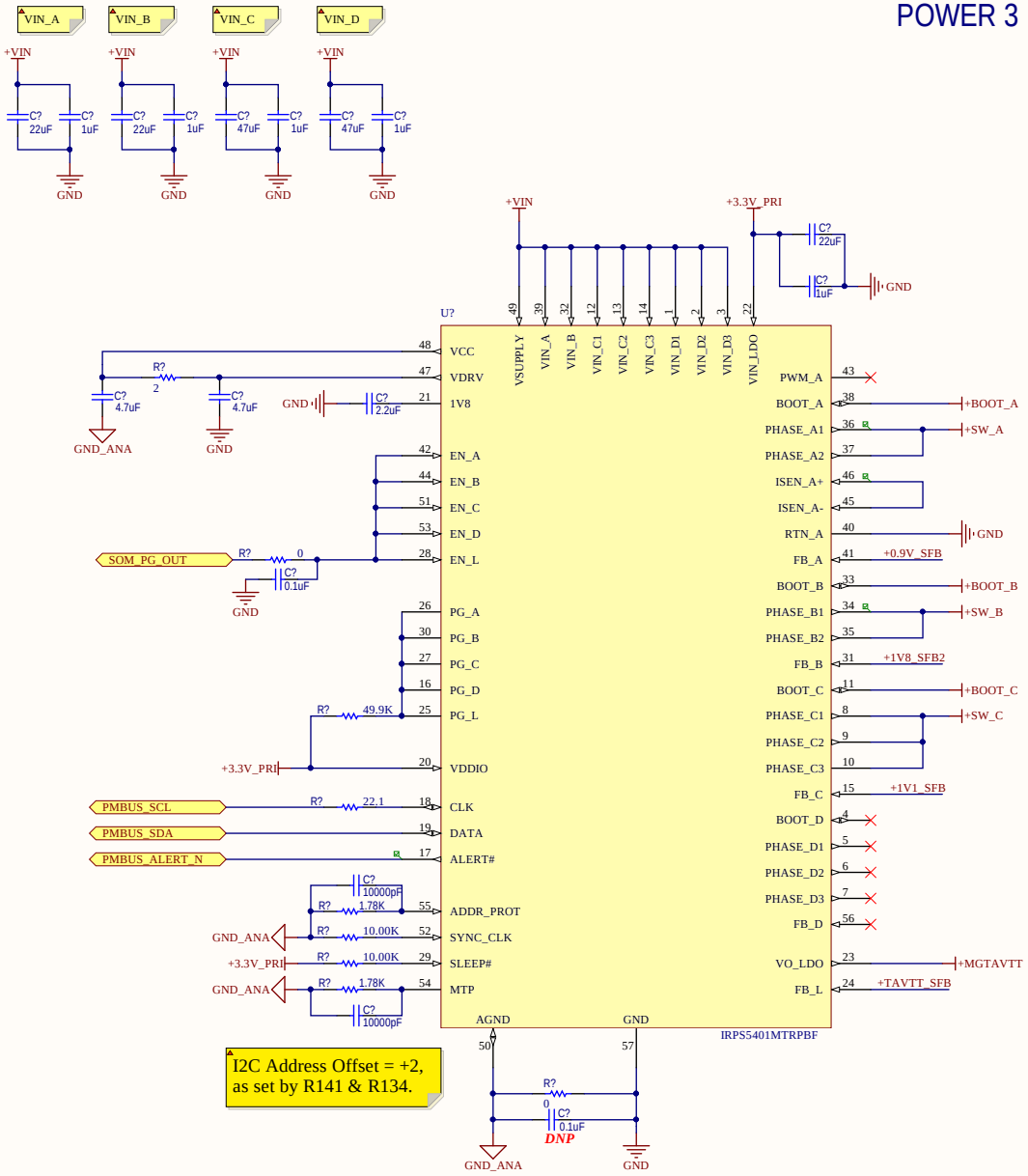


CH_LDO: +1.8V MGTRAVTT, 0.3A

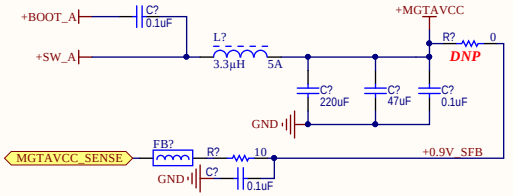


AVNET Avnet Engineering Services			
Project Name: UltraZed-EV Carrier Card	PCB Rev: A	BOM: 01	Variant: 00
Doc Num: SCH-US3CAR	Date: 3/23/2017	Time: 10:23:10 AM	
Sheet Title: 18 - POWER2.SchDoc	Size: B	Sheet: 18 of 20	

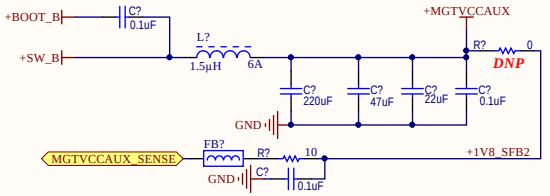
POWER 3



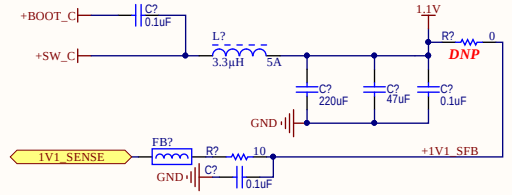
CHA: +0.9V MGTAVCC, 2.0A



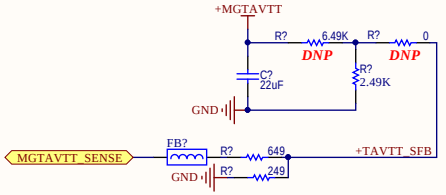
CHB: +1.8V MGTVCCAUX, 2.0A



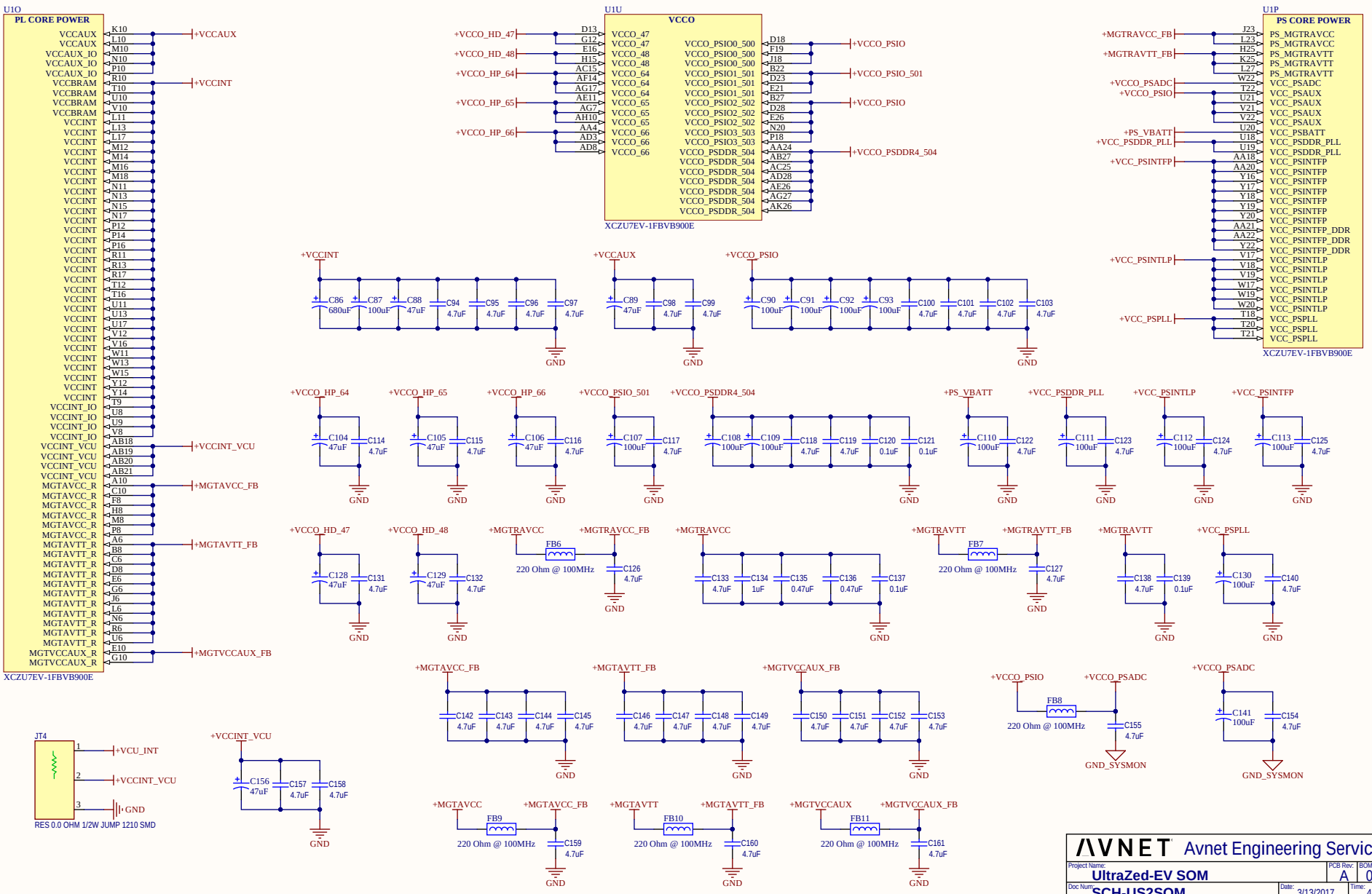
CHC: +1.1V HDMI, 2.0A

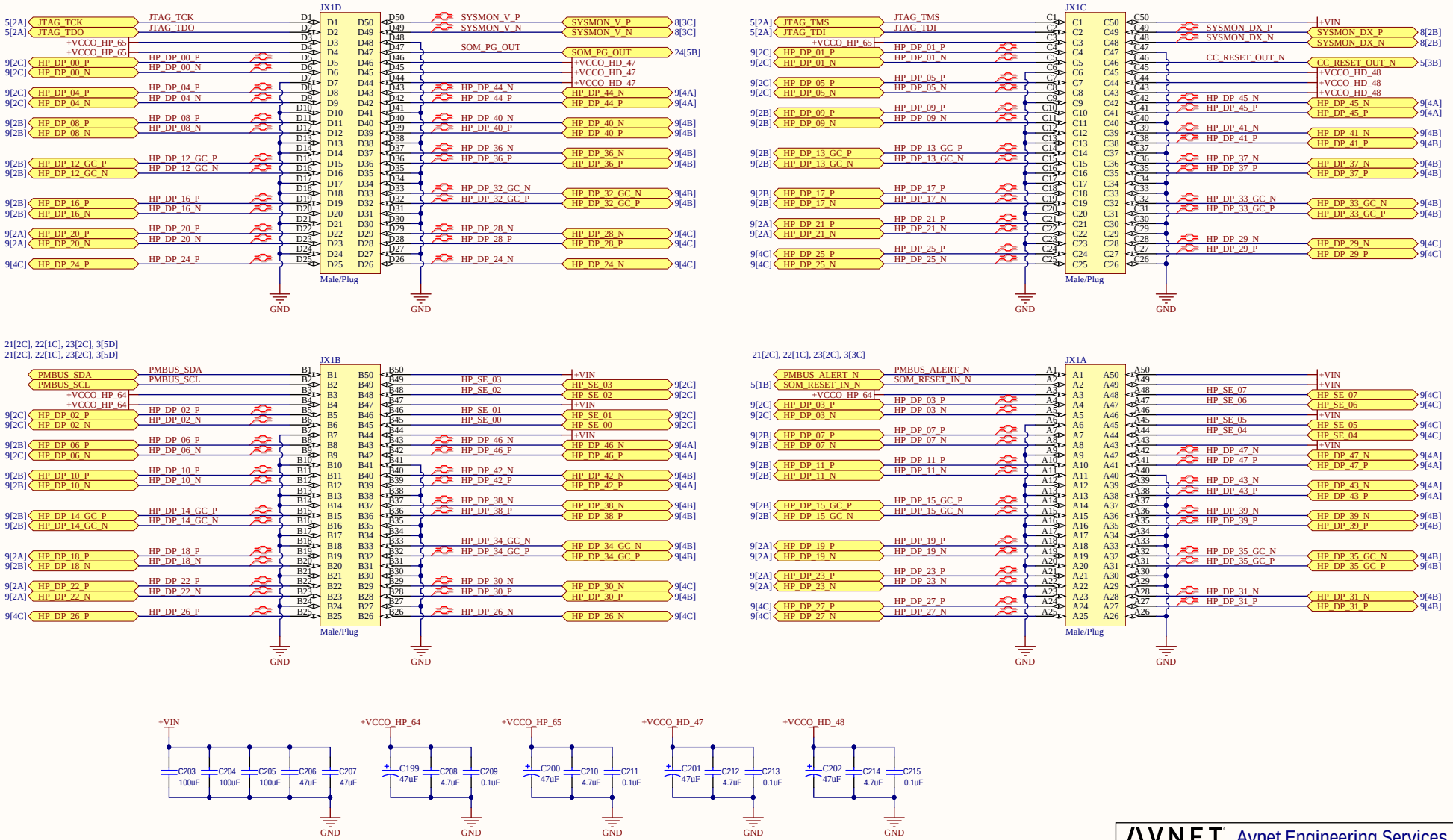


CH_LDO: +1.2V MGTAVTT, 0.5A



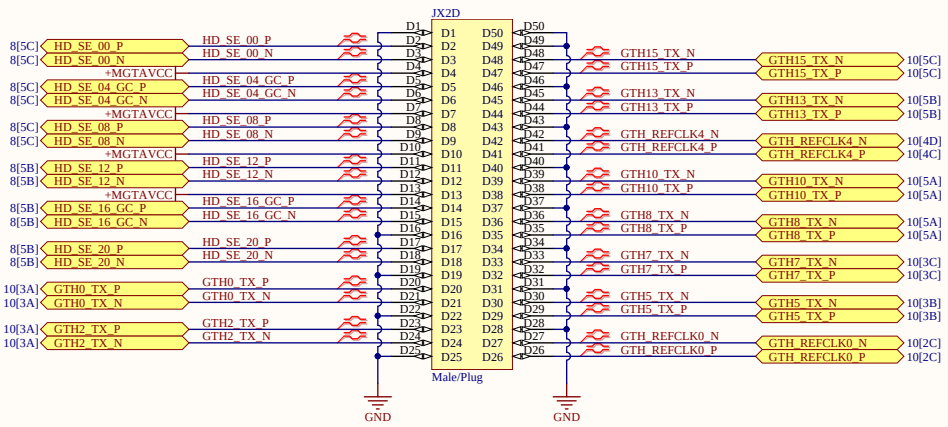
Avnet Engineering Services			
Project Name: UltraZed-EV Carrier Card	PCB Rev: A	BOM: 01	Variant: 00
Doc Num: SCH-US3CAR	Date: 3/23/2017	Time: 10:23:21 AM	
Sheet Title: 19 - POWER3.SchDoc	Size: B	Sheet: 19 of 20	

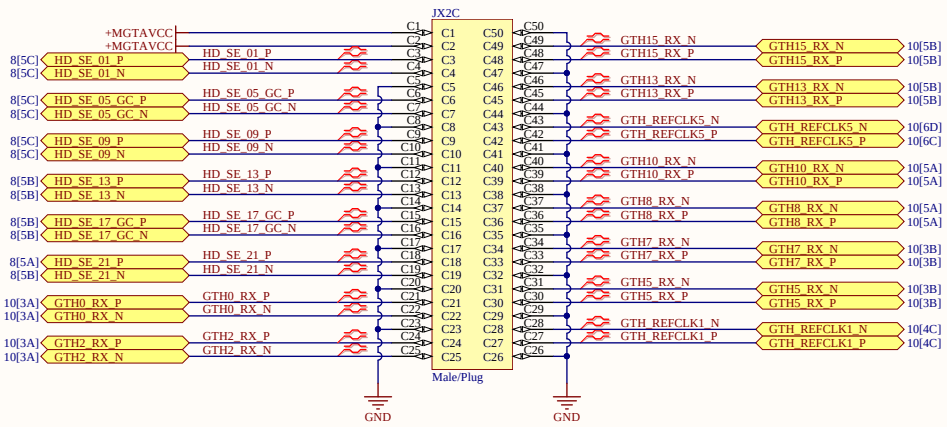

U1O
PL CORE POWER
XCZU7EV-1FBVB900E
U1U
VCCO
XCZU7EV-1FBVB900E
U1P
PS CORE POWER
XCZU7EV-1FBVB900E
+VCCAUX
+VCCINT
+VCCINT_VCU
+MGTAVCC_FB
+MGTAVTT_FB
+MGTVCCAUX_FB
+VCCO_PSIO
+VCCO_PSIO_501
+VCCO_PSDDR4_504
+VCCO_HP_64
+VCCO_HP_65
+VCCO_HP_66
+VCCO_HD_47
+VCCO_HD_48
+MGTRAVCC_FB
+MGTRAVTT_FB
+VCCO_PSADC
+PS_VBATT
+VCC_PSDDR_PLL
+VCC_PSINTFP
+VCC_PSINTLP
+VCC_PSPLL
GND
GND_SYSMON
FB6
FB7
FB8
FB9
FB10
FB11
220 Ohm @ 100MHz
JT4
+VCU_INT
RES 0.0 OHM 1/2W JUMPER 1210 SMD
AVNET Avnet Engineering Services
Project Name: UltraZed-EV SOM
PCB Rev: A
BOM: 01
Variant: 01
Doc Num: SCH-US2SOM
Date: 3/13/2017
Time: 4:23:43 PM
Sheet Title: 11 - MPSoC Power and Decoupling.SchDoc
Size: B
Sheet: 11 of 25

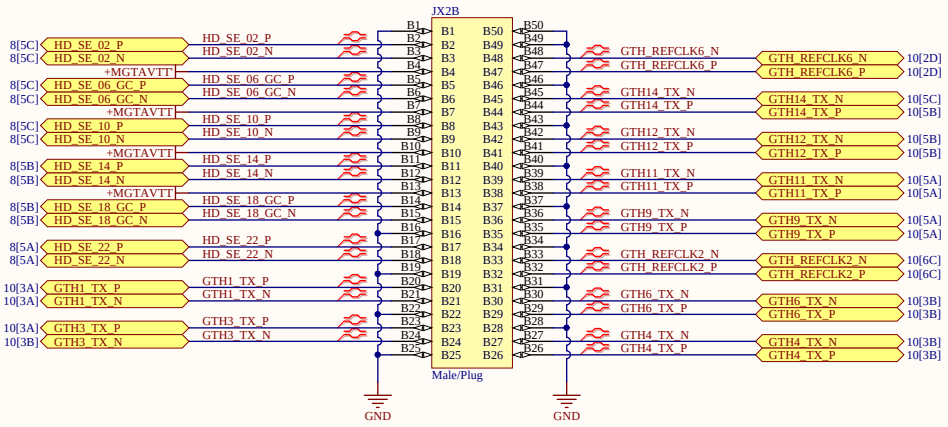


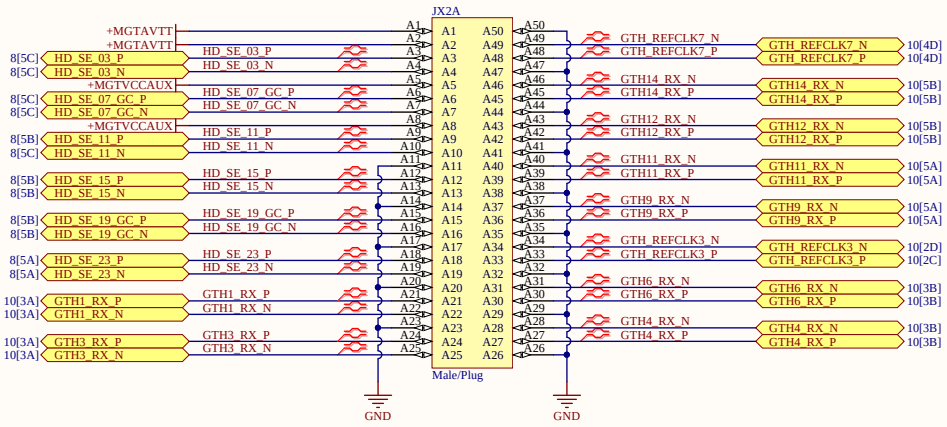
Project Name:	UltraZed-EV SOM
PCB Rev:	A
BOM:	01
Variant:	01
Doc Num:	SCH-US2SOM
Date:	3/13/2017
Time:	4:23:48 PM
Sheet Title:	18 - JX1 Micro Header.SchDoc
Size:	B
Sheet:	18 of 25

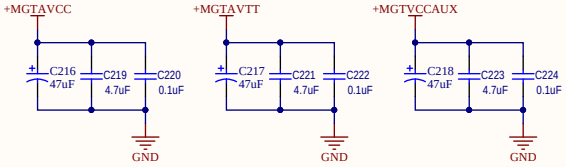
Avnet Engineering Services





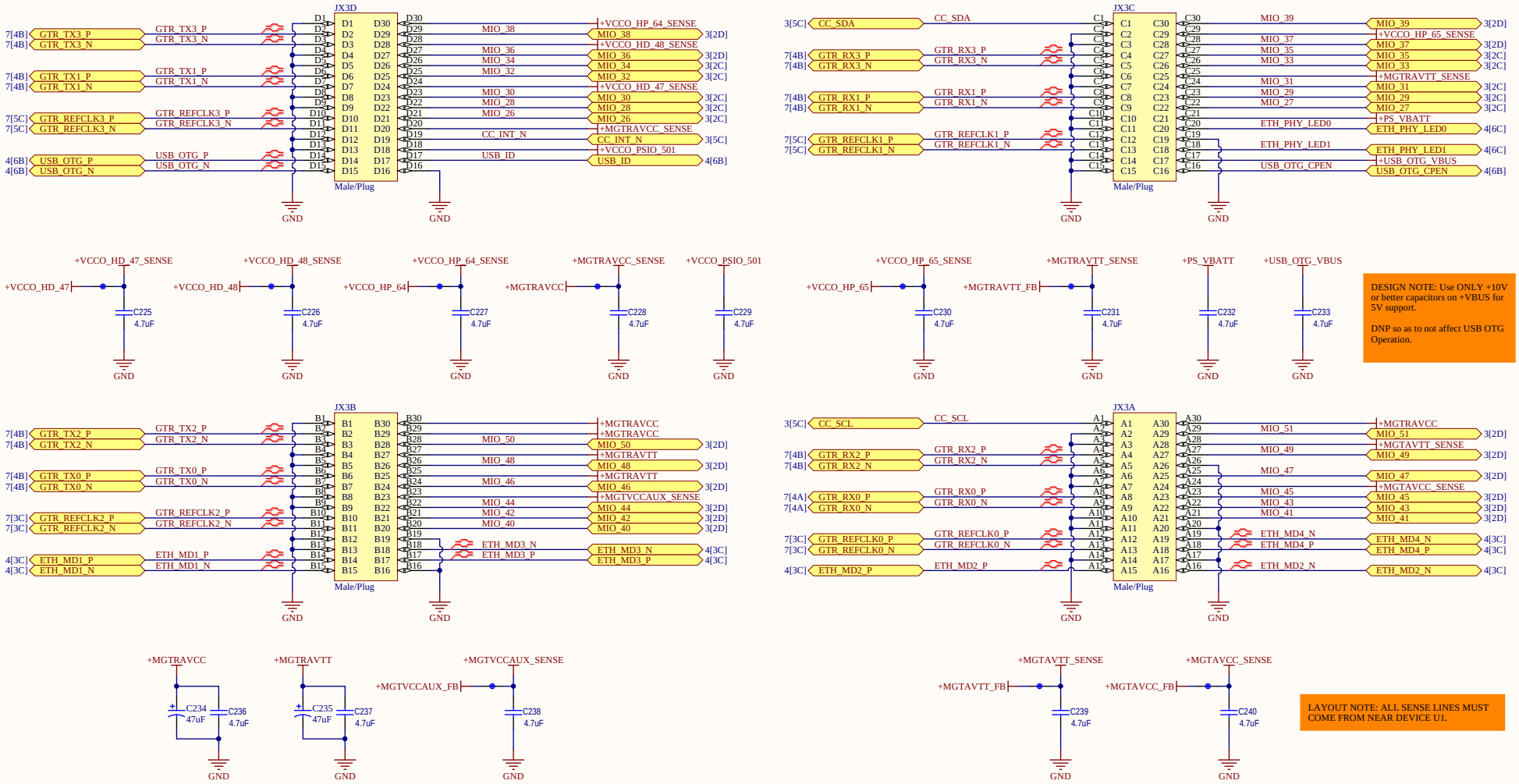






AVNET Avnet Engineering Services

Project Name: UltraZed-EV SOM	PCB Rev: A	BOM: 01	Variant: 01	
Doc Num: SCH-US2SOM	Date: 3/13/2017	Time: 4:23:54 PM		
Sheet Title: 19 - JX2 Micro Header.SchDoc	Size: B	Sheet: 19 of 25		



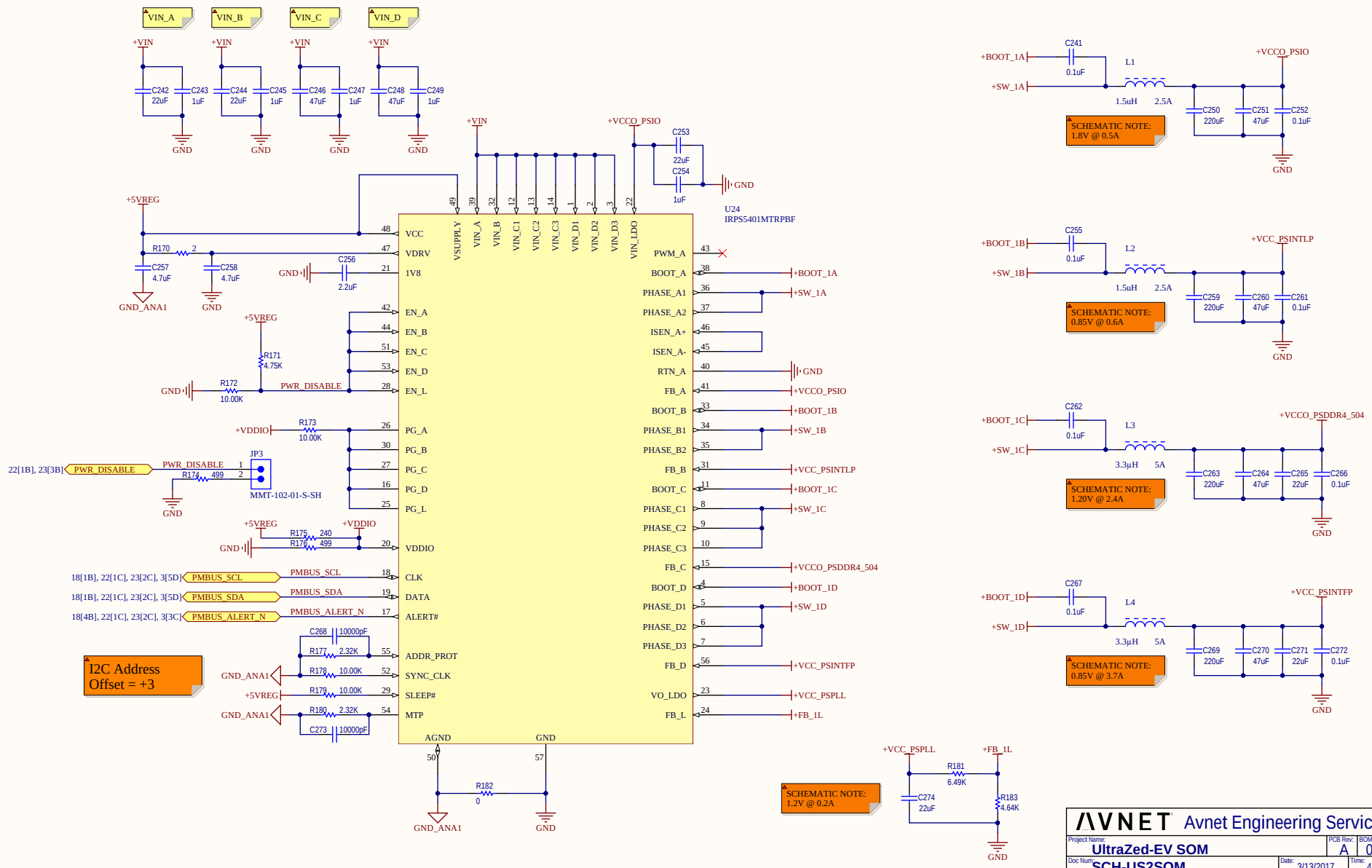
DESIGN NOTE: Use ONLY +10V or better capacitors on +VBUS for 5V support.

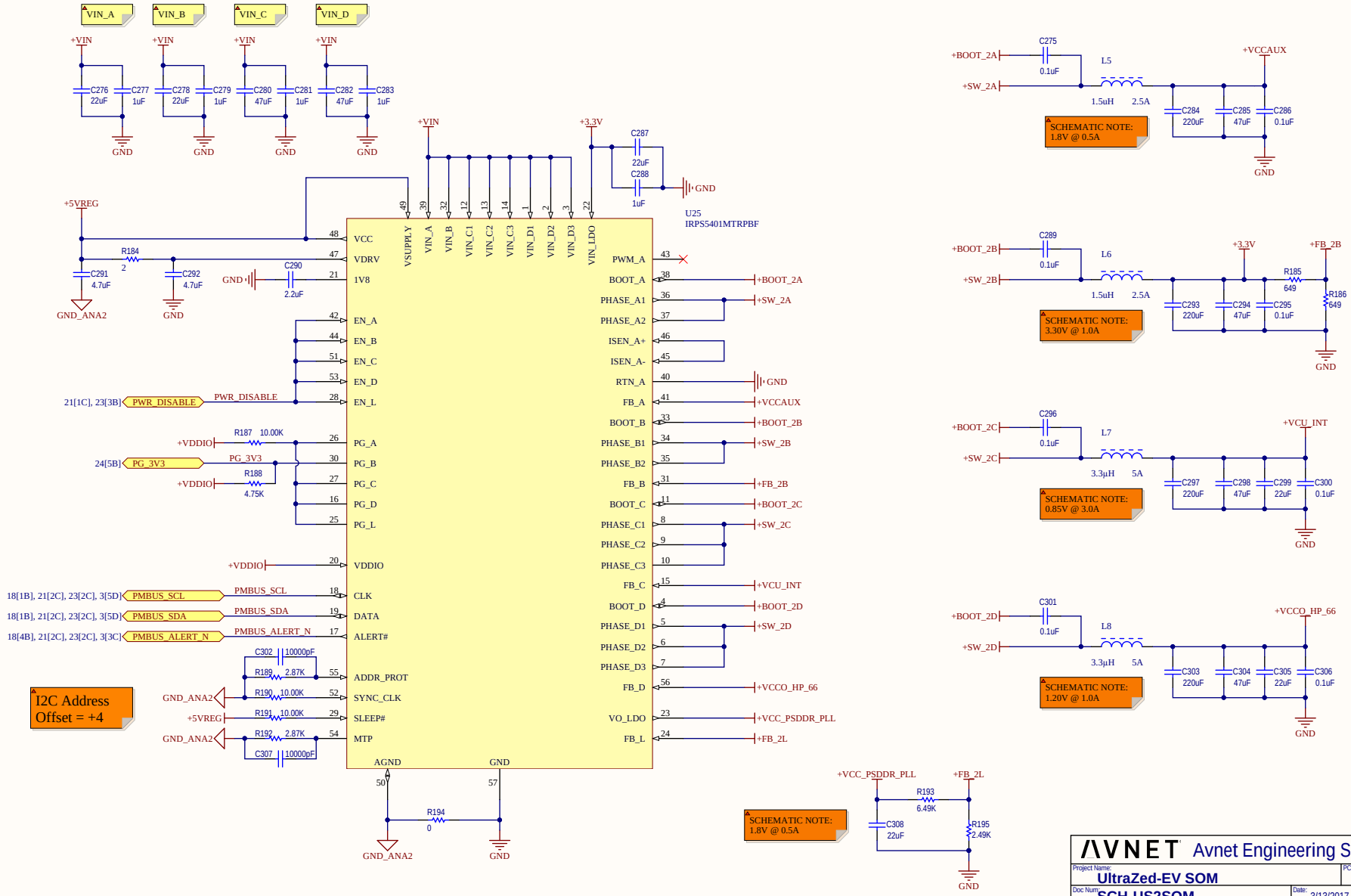
DNP so as to not affect USB OTG Operation.

LAYOUT NOTE: ALL SENSE LINES MUST COME FROM NEAR DEVICE U1.

AVNET Avnet Engineering Services

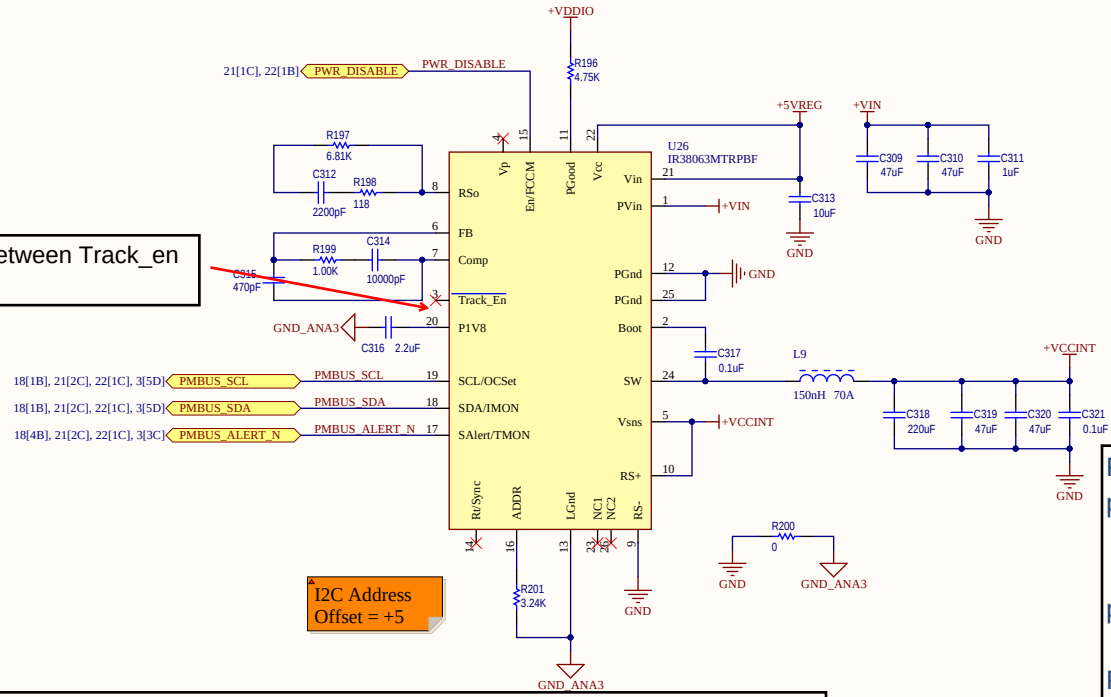
Project Name: UltraZed-EV SOM	PCB Rev: A	BOM: 01	Variant: 01
Doc Num: SCH-US2SOM	Date: 3/13/2017	Time: 4:23:59 PM	
Sheet Title: 20 - JX3 Micro Header.SchDoc	Size: B	Sheet: 20 of 25	


VIN_A
VIN_B
VIN_C
VIN_D
U24
IRPS5401MTRPBF
VCC
VDRV
1V8
EN_A
EN_B
EN_C
EN_D
EN_L
PG_A
PG_B
PG_C
PG_D
PG_L
VDDIO
CLK
DATA
ALERT#
ADDR_PROT
SYNC_CLK
SLEEP#
MTP
VSUPPLY
VIN_A
VIN_B
VIN_C1
VIN_C2
VIN_C3
VIN_D1
VIN_D2
VIN_D3
VIN_LDO
PWM_A
BOOT_A
PHASE_A1
PHASE_A2
ISEN_A+
ISEN_A-
RTN_A
FB_A
BOOT_B
PHASE_B1
PHASE_B2
FB_B
BOOT_C
PHASE_C1
PHASE_C2
PHASE_C3
FB_C
BOOT_D
PHASE_D1
PHASE_D2
PHASE_D3
FB_D
VO_LDO
FB_L
AGND
GND
PWR_DISABLE
PMBUS_SCL
PMBUS_SDA
PMBUS_ALERT_N
I2C Address
Offset = +3
SCHEMATIC NOTE:
1.8V @ 0.5A
SCHEMATIC NOTE:
0.85V @ 0.6A
SCHEMATIC NOTE:
1.20V @ 2.4A
SCHEMATIC NOTE:
0.85V @ 3.7A
SCHEMATIC NOTE:
1.2V @ 0.2A
MMT-102-01-S-SH
Avnet Engineering Services
Project Name: UltraZed-EV SOM
PCB Rev: A
BOM: 01
Variant: 01
Doc Num: SCH-US2SOM
Date: 3/13/2017
Time: 4:24:05 PM
Sheet Title: 21 - PMIC Power Supply #1.SchDoc
Size: B
Sheet: 21 of 25



AVNET Avnet Engineering Services

Project Name: UltraZed-EV SOM	PCB Rev: A	BOM: 01	Variant: 01	
Doc Num: SCH-US2SOM	Date: 3/13/2017	Time: 4:24:25 PM		
Sheet Title: 22 - PMIC Power Supply #2.SchDoc	Size: B	Sheet: 22 of 25		



Connect 100K between Track_en and P1V8

PVin=12V, with load side caps, predicted BW= 78 kHz

PVin=5V, with load side caps, predicted BW= 68 kHz

PVin=12V, without load side caps, predicted BW= 100 kHz

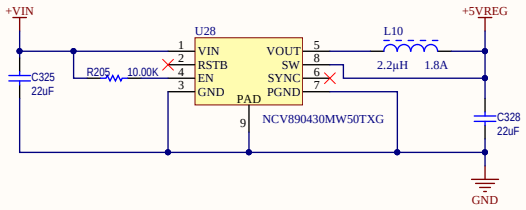
PVin=5V, without load side caps, predicted BW= 90 kHz

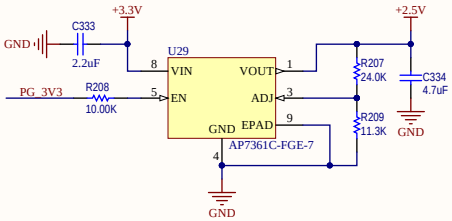
Add 3 X47uF ceramic caps to this design. This is so that we can meet transient requirements when the carrier card capacitance is available, while preventing the bandwidth from becoming too high when the carrier card is not mounted. Then,

R197=4.87K
C312=2200pF
R198=86.6ohm
C314=10 nF
C315=220pF
R199=1.87K

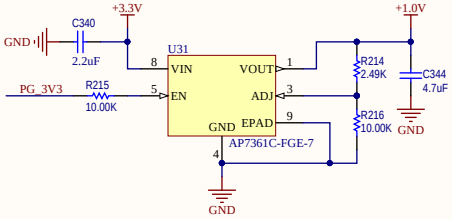
AVNET Avnet Engineering Services

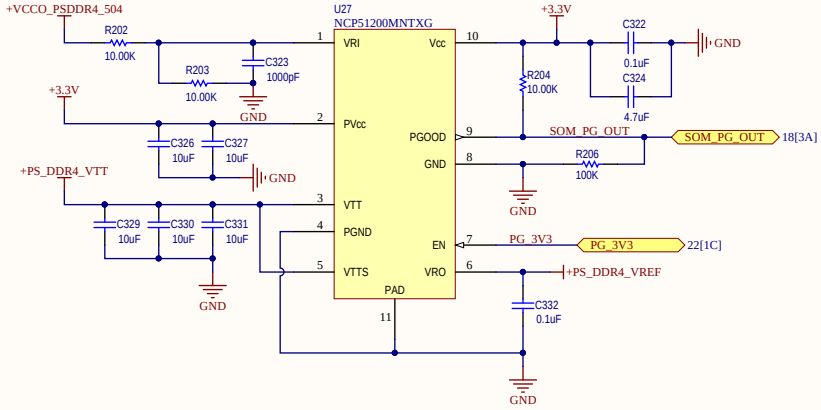
Project Name: UltraZed-EV SOM	PCB Rev: A	BOM: 01	Variant: 01
Doc Num: SCH-US2SOM	Date: 3/13/2017	Time: 4:25:11 PM	
Sheet Title: 23 - PMIC Power Supply #3.SchDoc	Size: B	Sheet: 23 of 25	

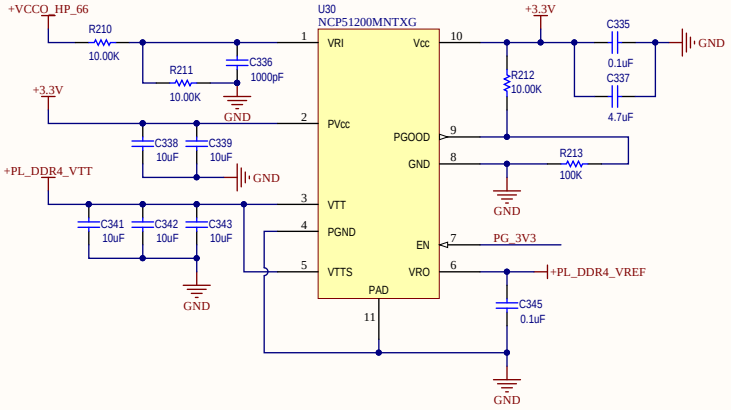




DESIGN NOTE: VOUT = ((R1/R2) + 1) * 0.8







AVNET Avnet Engineering Services			
Project Name: UltraZed-EV SOM	PCB Rev: A	BOM: 01	Variant: 01
Doc Num: SCH-US2SOM	Date: 3/13/2017	Time: 4:25:41 PM	
Sheet Title: 24 - Misc Power Supplies.SchDoc	Size: B	Sheet: 24 of 25	