65 W PAG2P-2S HF-ZVS (REF_65W_HFZVS_PAG2) charger board test report

About this document

Scope and purpose

This document provides power management test results of the 65W PAG2P-2S HF ZVS REV3 Solution Demo Board. The tests were performed on REV3 ZVS board, which is equipped with Infineon CYPAP212A1-14SXI on the primary and CYPAS211A1-32LQXQ on the secondary section of the converter.

Intended audience

This document is intended for customers and FAEs using the EZ-PD™ PAG2P/PAG2S QR zero voltage switching REF_65W_HFZVS_PAG2 hardware.

Table of contents

Table of contents

1 Introduction

This test report captures the performance of PAG2S (Power Adapter Generation 2 – Secondary controller) and PAG2P (Primary controller) high-frequency quasi-resonant zero-voltage switching (QR-ZVS) flyback based on the USB PD, 65 W charger solution demo kit. This is a highly power-dense form-factor (32 W/inch^3) and an efficient (>94 percent) charger solution kit.

EZ-PD™ PAG2P CYPAP212A1-14SXI (Power Adapter Generation 2 Primary) is Infineon's second generation integrated primary-side start-up controller for AC/DC applications targeting the mobile power adapter segment. PAG2P interfaces with the AC mains rectified output on the primary side and receives the necessary PWM signal from the secondary side to provide a regulated output voltage. PAG2P is designed to complement a secondary controlled AC/DC flyback converter topology. In this topology, voltage and current regulation is performed by the secondary controller (PAG2S). PAG2P is responsible for providing the start-up function, driving the primary side FET as well as responding to all the fault conditions.

EZ-PD™ PAG2S CYPAS211A1-32LQXQ is an integrated secondary-side PWM controller and USB Power Delivery (USB PD) controller. PAG2S integrates secondary side synchronous rectifier (SR), pulse-width modulator (PWM), and zero voltage switching (ZVS) control. PAG2S is targeted towards USB-C power adapters and fits well into high-efficiency AC-DC flyback designs with USB PD and other standard charging protocols. PAG2S also supports USB PD Extended Power Range (EPR) mode.

Figure 1 shows the application diagram for a power adapter implementing a secondary-side controlled synchronous flyback converter topology. PAG2S modulates the pulse width of the primary MOSFET in voltage control mode. PAG2S engages the internal error amplifies (EA) and a programmable ramp generator to determine the pulse width of PWM. The PWM signal is transferred from the secondary to the primary side through a pulse edge transformer.

In this topology, PAG2S integrates three key features: secondary-side PWM control, charging protocol control, and fault protection. This approach of integrating the ZVS on the secondary side has advantages over the traditional primary side control in the following ways:

- Programmable high side ON time to reach true ZVS operation to achieve optimized efficiency.

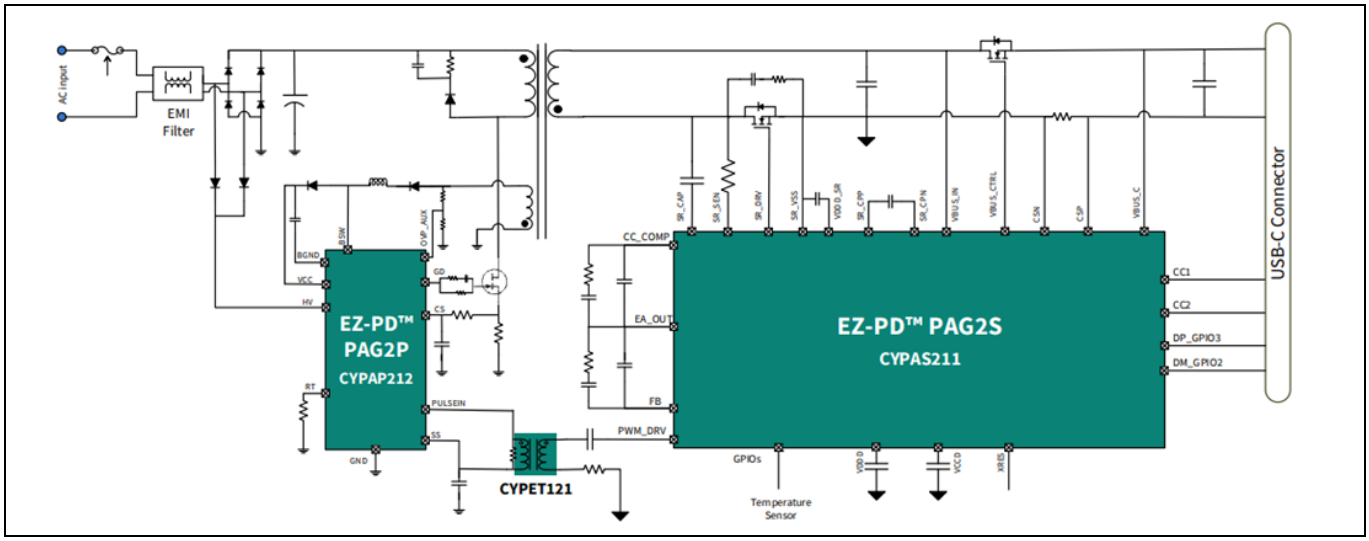


Figure 1 Application diagram for a power adapter in a secondary side controlled flyback converter topology along with ZVS operation

2 Test setup

2.1 Device under test (DUT)

Table 1 65 W PAG2P-2S HFZVS Solution Demo Board DUT hardware and software configurations

DUT contents	Description	Remarks
Hardware – configuration		
PAG2P+PAG2S HFZVS 65W Solution Board V3	Rev 3	–
Firmware		
Firmware repo	*zvs_hf_ver9.hex*	

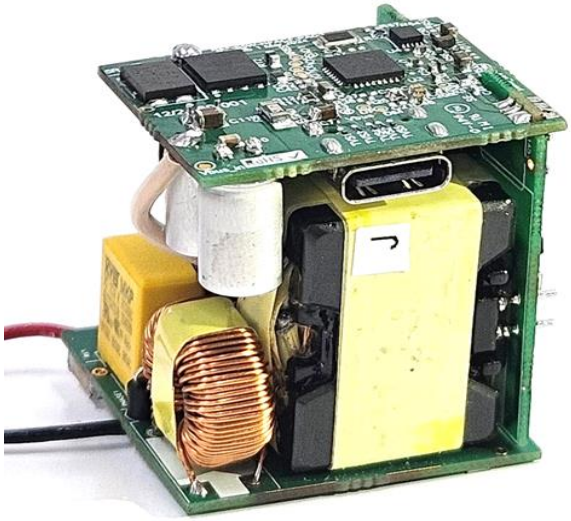


Figure 2 Isometric view of 65 W PAG2P HFZVS Solution Demo Board

Dimensions (in mm): 34.29 x 31.97 x 30.46

Figure 3 Top view of the 65 W PAG2P HFZVS Solution Demo Board

2.2 DUT setup

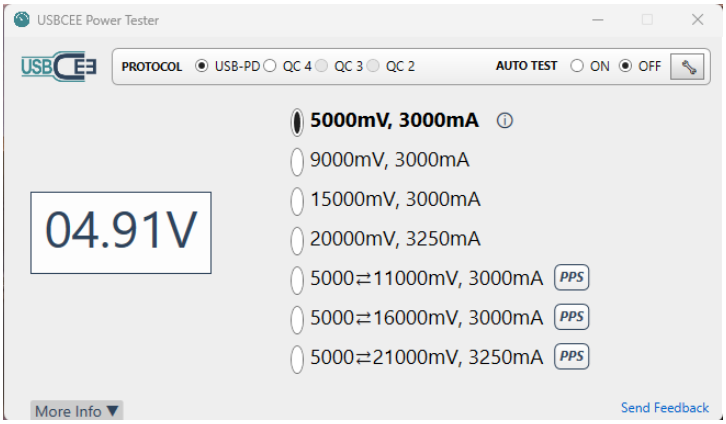


Figure 4 Physical CCGPROG PAT and USBCEE Power Tester UI

The DUT is connected to PAT i.e., Power Adapter Tester (CCPROG PAT) using a USB Type-C cable. Once a successful connection is established, PAT UI does a PDO discovery and displays the same on the UI. In our case, the solution kit is pre-configured with seven PDOs:

- PDO 1: 5 V, 3 A FIXED
- PDO 2: 9 V, 3 A FIXED
- PDO 3: 15 V, 3 A FIXED
- PDO 4: 20 V, 3.25 A FIXED
- PDO 5: 5 V to 11 V, 3 A PPS
- PDO 6: 5 V to 16 V, 3 A PPS
- PDO 7: 5 V to 21 V, 3.25 A PPS

One can either choose the suitable pre-configured PDO or configure a new one using Infineon's EZ-PD™ Configuration Utility. For the tests in the following sections, we use the pre-configured PDOs.

To know more about PAT tester, visit USBCEE.

2.3 Test equipment

The test equipment used to measure the efficiency, ripple, regulation, and transient response are shown in Table 2.

Table 2 Test equipment details

Test setup	Description
Oscilloscope name	Tektronix MDO4104C/MSO 44
Power meter	Yokogawa WT310E
Digital multimeter (V_O and I_O)	Keysight 34465A
Programmable AC source	Chroma 61501/61502
Electronic load	Chroma 63113A/63103
Thermal camera	Flir E75
Automation software	LabVIEW/Python

3 Power management test results

Note: All the tests mentioned in this report are carried-out under open-frame condition.

3.1 Efficiency and no-load consumption

Table 3 Efficiency and no-load consumption results

Parameter	Standard (Minimum value)		Unit	Test condition	Test result	
	DoE Level-6	CoCv5 Tier 2			115 V_{AC} 60 Hz	230 V_{AC} 50 Hz
Four-point average efficiency (Average of 25%, 50%, 75%, 100% load)	81.39	81.84	%	V_O = 5 V_{DC}, I_O = 3 A	92.54	93.17
	86.62	87.30	%	V_O = 9 V_{DC}, I_O = 3 A	93.36	93.95
	87.73	88.85	%	V_O = 15 V_{DC}, I_O = 3 A	93.52	93.93
	88	89	%	V_O = 20 V_{DC}, I_O = 3.25 A	93.48	93.68
CoCv5 Tier2 10% load efficiency	–	72.48	%	V_O = 5 V_{DC}, I_O = 0.3 A	90.08	89.49
	–	77.30	%	V_O = 9 V_{DC}, I_O = 0.3 A	91.28	91.29
	–	78.85	%	V_O = 15 V_{DC}, I_O = 0.3 A	91.42	88.38
	–	79	%	V_O = 20 V_{DC}, I_O = 0.325 A	91.12	88.85
	Standard (Maximum value)				Test result	
Parameter	DoE Level-6	CoCv5 Tier 2		Test condition	115 V_{AC} 60 Hz	230 V_{AC} 50 Hz
No - load power consumption	100	75	mW	No USB sink attached	24 mW	28 mW
	–	–	–	USB sink attached	60 mW	60 mW

Note:

1. *Peak Efficiency: 94.39% (At 265 V_{AC} - 63Hz, 15V - 3A)*
2. *Full load Efficiency at 230 V_{AC}: 94.26% (At 230 V_{AC} - 50 Hz, 20 V - 3.2 5A)*
3. *Full load Efficiency at 115 V_{AC}: 93.66% (At 115 V_{AC} - 60 Hz, 20 V - 3.25 A)*
4. *Full load Efficiency at 90 V_{AC}: 92.40% (At 90 V_{AC} - 47 Hz, 20 V - 3.25 A)*
5. *V_{OUT} for efficiency calculations is measured across V_{BUS_C} at board end with 10 minutes warmup*
6. *Variation of ±0.5% in efficiency can be observed across units*

Power management test results

Table 4 lists the instruments used to capture the efficiency data.

Table 4 Instruments used to capture efficiency data

Instruments	Model number
AC source	GWInstek ASR2100
Power meter (V_{IN} and PIN)	Hioki PW3335
I_{OUT} measurement shunt	Vishay Y14730R00500B0R
Electronic load	GWInstek PEL-3021
Data logger (V_{BUS} and I_{OUT})	Keysight 34970 A

Table 5 EuP Lot6 V1

Parameter	Test condition	Max. Pin (mW)	Test result			
			115 V_{AC} 60 Hz		230 V_{AC} 50 Hz	
			Pin (mW)	Efficiency (%)	Pin (mW)	Efficiency (%)
Efficiency at 250 mW load	V_O = 5 V_{DC} I_O = 50 mA	500	317	78.6	321	77.6
Efficiency at 250 mW load	V_O = 9 V_{DC} I_O = 27.78 mA		342	73.0	347	71.9
Efficiency at 250 mW load	V_O = 15 V_{DC} I_O = 16.67 mA		389	64.2	391	63.9
Efficiency at 250 mW load	V_O = 20 V_{DC} I_O = 12.5 mA		433	57.7	439	56.9

Power management test results

Table 6 Efficiency from 1% to 10% load at 90 V_{AC} 47 Hz for 20 V output

Load %	V_{AC}	Frequency	Pin	V_{OUT}	I_{OUT}	P_o	Efficiency
1	90	47	0.870	19.979	0.033	0.659	75.79%
2	90	47	1.610	19.980	0.067	1.329	82.53%
3	90	47	2.290	19.981	0.098	1.967	85.90%
4	90	47	2.990	19.981	0.131	2.623	87.74%
5	90	47	3.690	19.982	0.163	3.261	88.37%
6	90	47	4.400	19.982	0.197	3.932	89.37%
7	90	47	5.090	19.982	0.229	4.569	89.77%
8	90	47	5.790	19.983	0.262	5.228	90.29%
9	90	47	6.500	19.983	0.294	5.885	90.53%
10	90	47	7.200	19.982	0.327	6.535	90.77%

Table 7 Efficiency from 10% to 100% load at 90 V_{AC} 47 Hz for 20 V output

Load %	V_{AC}	Frequency	Pin	V_{OUT}	I_{OUT}	P_o	Efficiency
10	90	47	7.190	19.969	0.327	6.531	90.84%
20	90	47	14.130	19.968	0.653	13.044	92.31%
30	90	47	21.090	19.965	0.980	19.563	92.76%
40	90	47	28.050	19.961	1.306	26.066	92.93%
50	90	47	35.040	19.959	1.632	32.575	92.96%
60	90	47	42.030	19.954	1.959	39.080	92.98%
70	90	47	49.070	19.949	2.285	45.576	92.88%
80	90	47	56.120	19.947	2.611	52.084	92.81%
90	90	47	63.160	19.941	2.937	58.574	92.74%
100	90	47	70.410	19.938	3.264	65.068	92.41%

Table 8 Efficiency from 1% to 10% load at 115 V_{AC} 60 Hz for 20 V output

Load %	V_{AC}	Frequency	Pin	V_{OUT}	I_{OUT}	P_o	Efficiency
1	115	60	0.870	19.988	0.033	0.660	75.82%
2	115	60	1.590	19.988	0.067	1.331	83.74%
3	115	60	2.290	19.988	0.098	1.966	85.83%
4	115	60	2.990	19.988	0.131	2.620	87.64%
5	115	60	3.670	19.988	0.163	3.259	88.81%
6	115	60	4.390	19.989	0.197	3.930	89.53%
7	115	60	5.080	19.988	0.229	4.571	89.99%
8	115	60	5.780	19.988	0.262	5.227	90.43%
9	115	60	6.480	19.988	0.294	5.880	90.74%
10	115	60	7.230	19.986	0.327	6.534	90.38%

Power management test results

Table 9 Efficiency from 10% to 100% load at 115 V_{AC} 60 Hz for 20 V output

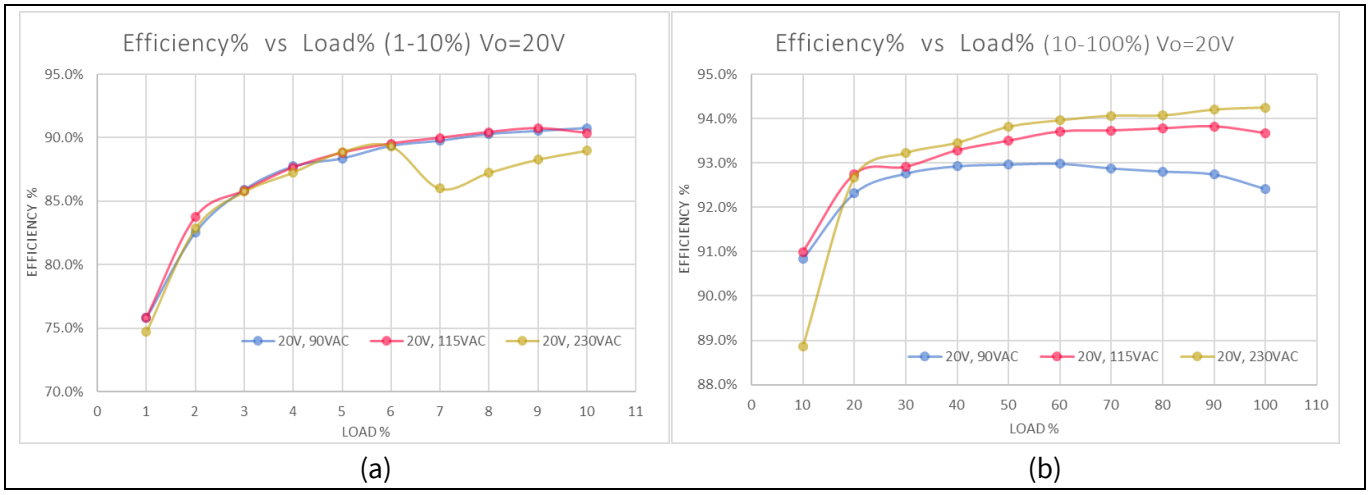
Load %	V_{AC}	Frequency	Pin	V_{OUT}	I_{OUT}	P_o	Efficiency
10	115	60	7.180	19.972	0.327	6.533	90.99%
20	115	60	14.070	19.970	0.653	13.049	92.74%
30	115	60	21.060	19.966	0.980	19.567	92.91%
40	115	60	27.950	19.962	1.306	26.072	93.28%
50	115	60	34.840	19.958	1.632	32.574	93.50%
60	115	60	41.710	19.955	1.959	39.085	93.71%
70	115	60	48.630	19.949	2.285	45.580	93.73%
80	115	60	55.540	19.945	2.611	52.083	93.78%
90	115	60	62.430	19.940	2.937	58.572	93.82%
100	115	60	69.470	19.938	3.264	65.071	93.67%

Table 10 Efficiency from 1% to 10% load at 230 V_{AC} 50 Hz for 20 V output

Load %	V_{AC}	Frequency	Pin	V_{OUT}	I_{OUT}	P_o	Efficiency
1	230	50	0.880	19.993	0.033	0.657	74.68%
2	230	50	1.600	19.991	0.066	1.325	82.82%
3	230	50	2.290	19.993	0.098	1.963	85.74%
4	230	50	3.000	19.993	0.131	2.618	87.27%
5	230	50	3.670	19.991	0.163	3.262	88.89%
6	230	50	4.400	19.991	0.197	3.931	89.34%
7	230	50	5.310	19.988	0.228	4.566	85.99%
8	230	50	5.990	19.984	0.261	5.226	87.24%
9	230	50	6.660	19.984	0.294	5.880	88.28%
10	230	50	7.340	19.984	0.327	6.531	88.98%

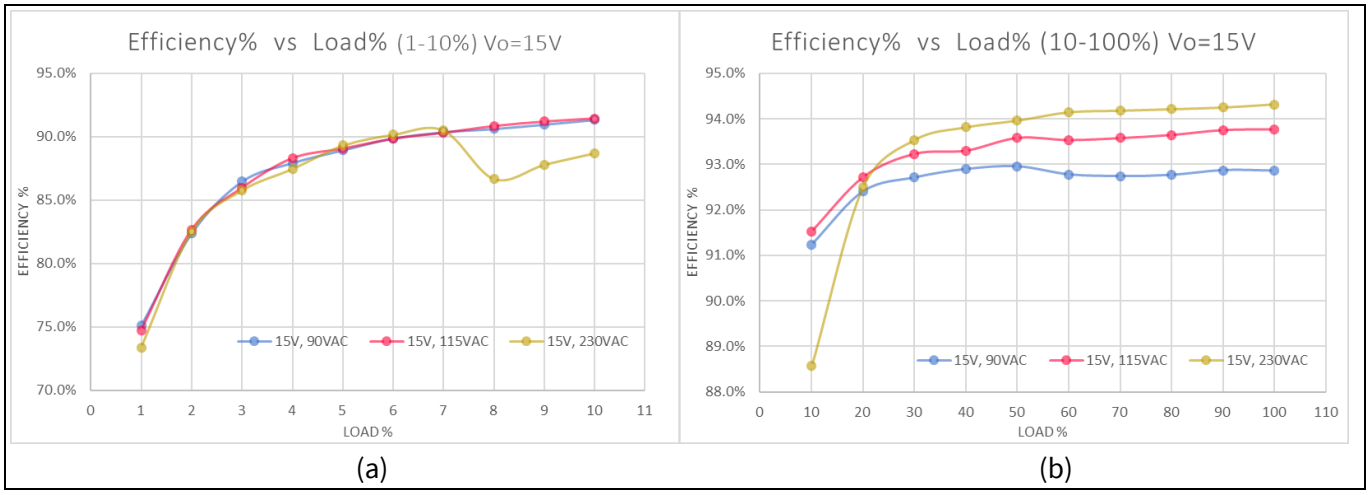
Table 11 Efficiency from 10% to 100% load at 230 V_{AC} 50 Hz for 20 V output

Load %	V_{AC}	Frequency	Pin	V_{OUT}	I_{OUT}	P_o	Efficiency
10	230	50	7.350	19.968	0.327	6.531	88.86%
20	230	50	14.080	19.966	0.653	13.047	92.66%
30	230	50	20.980	19.963	0.980	19.558	93.22%
40	230	50	27.890	19.957	1.306	26.064	93.45%
50	230	50	34.720	19.953	1.632	32.572	93.81%
60	230	50	41.580	19.948	1.959	39.069	93.96%
70	230	50	48.440	19.942	2.285	45.565	94.06%
80	230	50	55.340	19.935	2.611	52.059	94.07%
90	230	50	62.150	19.931	2.938	58.547	94.20%
100	230	50	69.000	19.927	3.264	65.032	94.25%



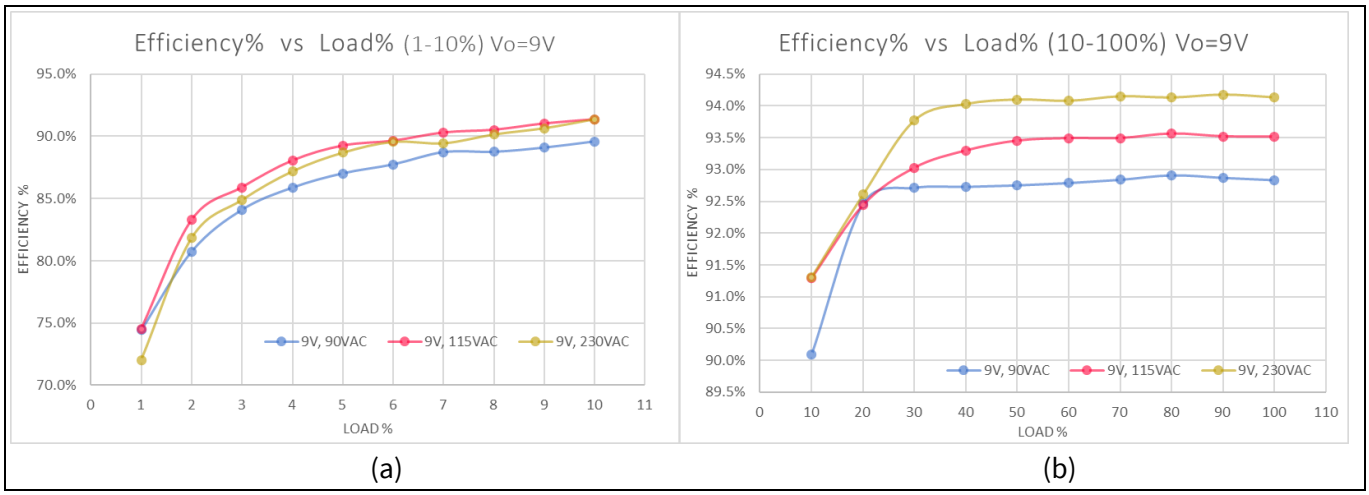
(a) (b)

Figure 5 **(a) Efficiency with 1% to 10% load for 20 V output; (b) Efficiency with 10% to 100% load for 20 V output**



(a) (b)

Figure 6 **(a) Efficiency with 1% to 10% load for 15 V output; (b) Efficiency with 10% to 100% load for 15 V output**



(a) (b)

Figure 7 **(a) Efficiency with 1% to 10% load for 9 V output; (b) Efficiency with 10% to 100% load for 9 V output**

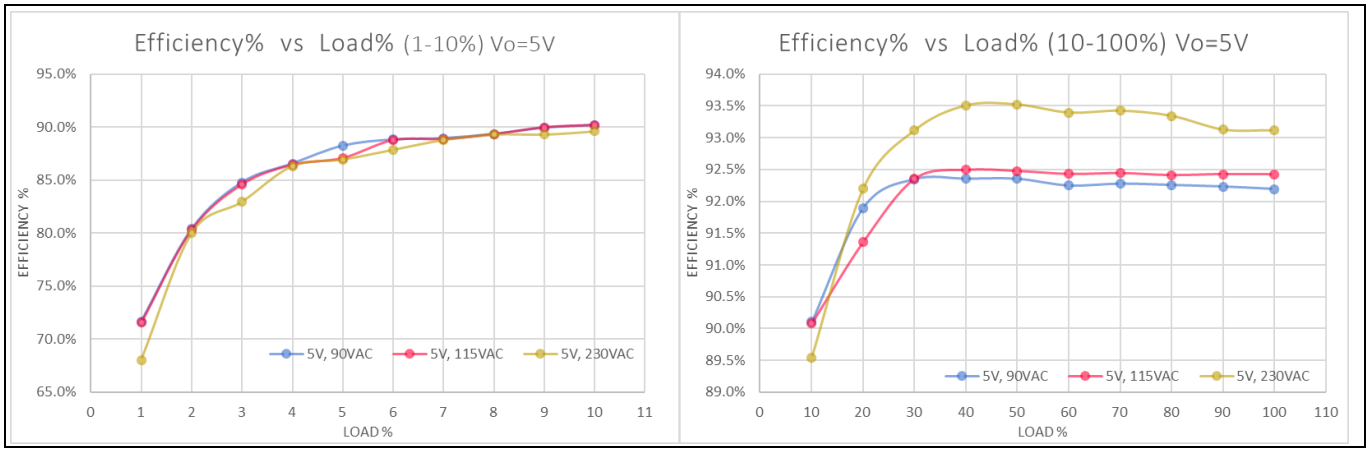


Figure 8 **(a) Efficiency with 1 to 10% load for 5 V output; (b) Efficiency with 10 to 100% load for 5 V output**

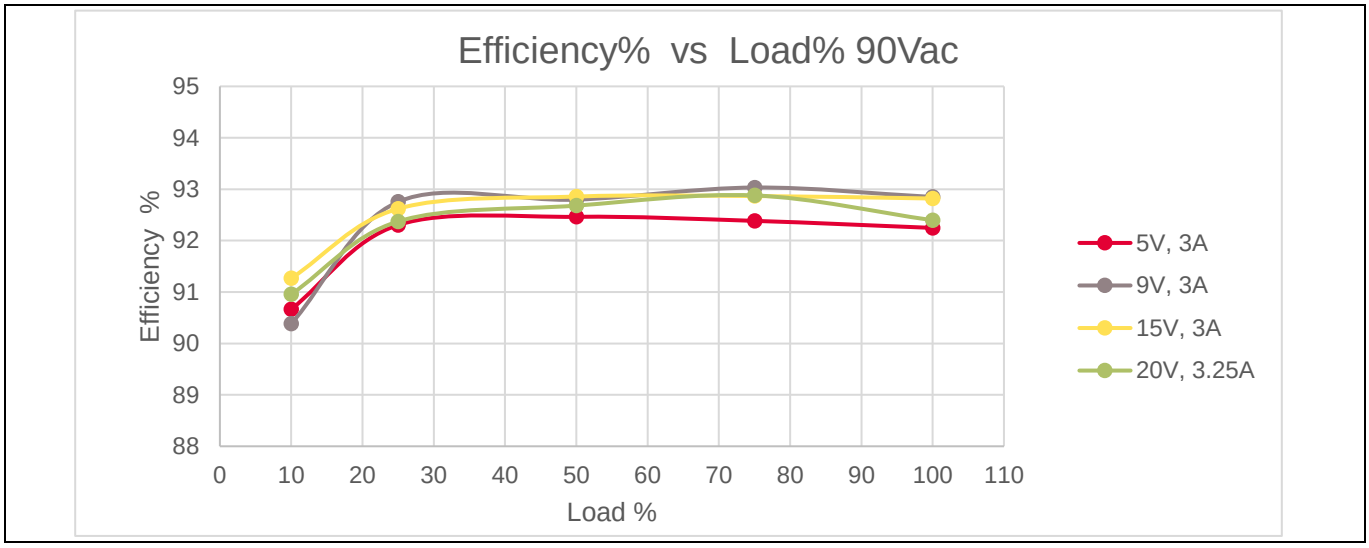


Figure 9 **Efficiency at 90 V_{AC}, 47 Hz**

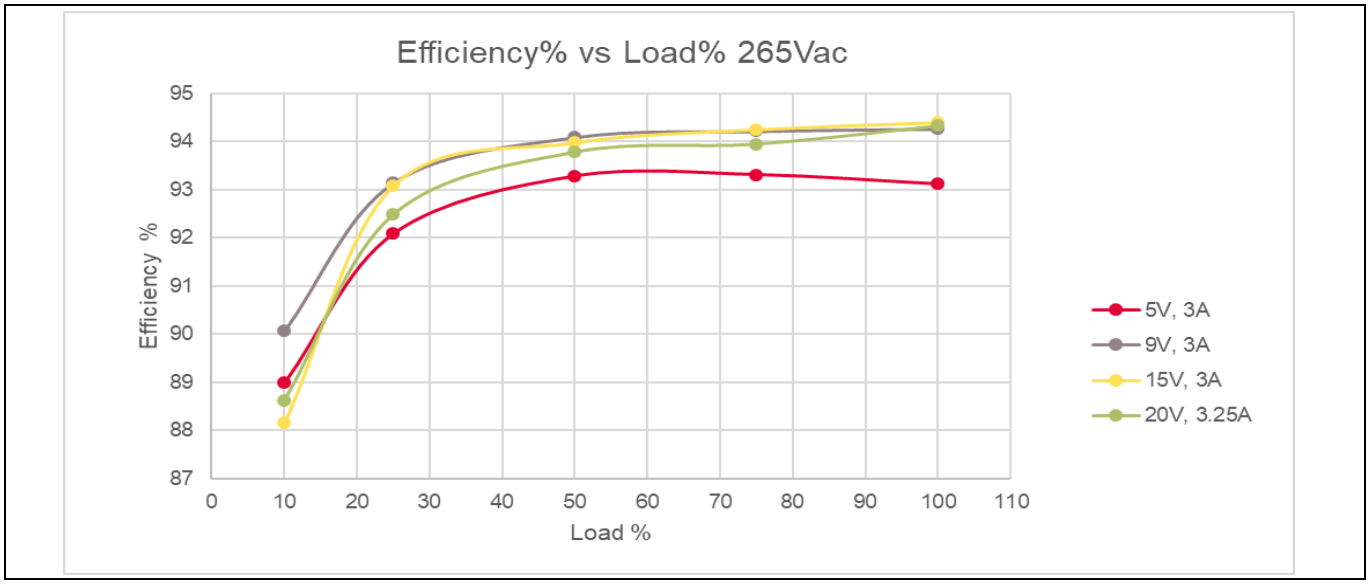


Figure 10 **Efficiency at 265 V_{AC}, 63 Hz**

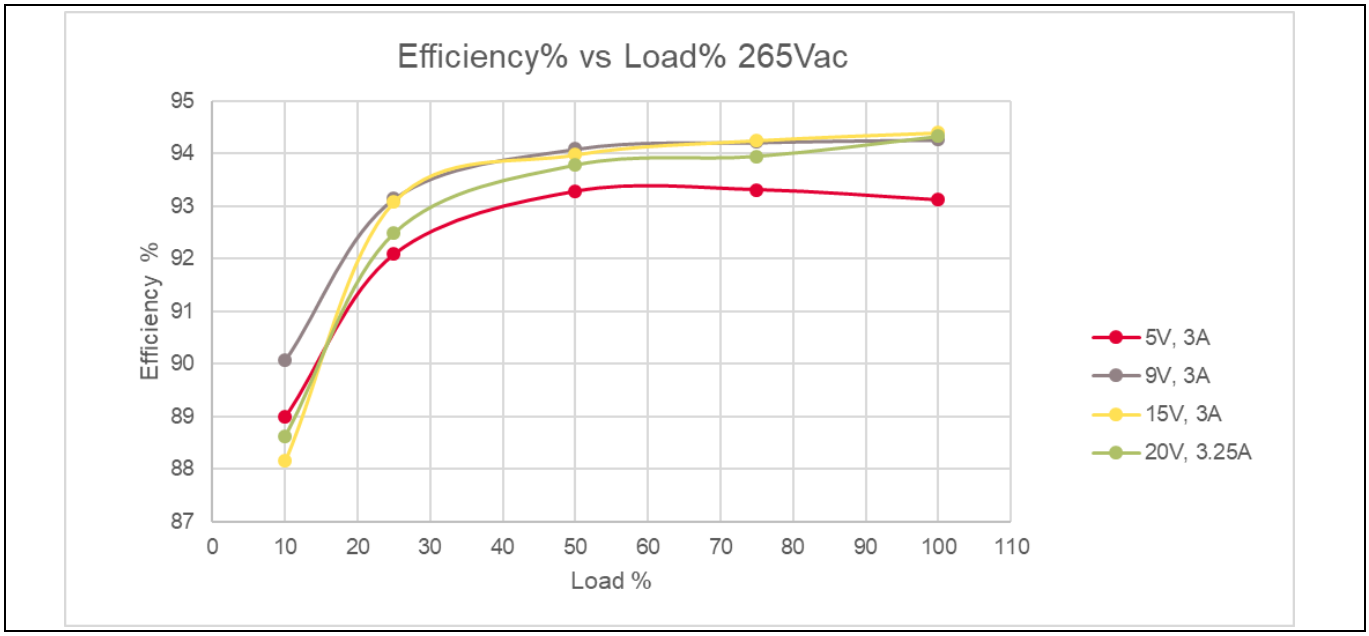


Figure 11 Efficiency at 265 V_{AC}, 63 Hz

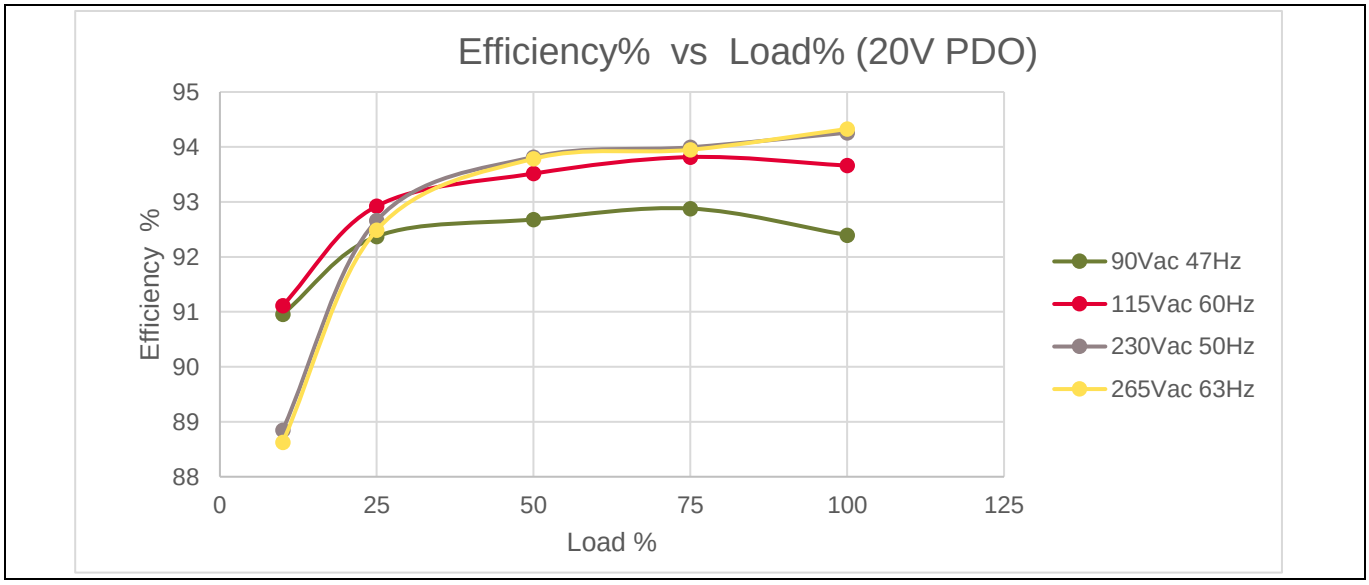


Figure 12 Efficiency at different line conditions for 20 V PDO

Table 12 Full load efficiency at different line condition

Sl.no.	V_{AC} (V)	Freq (Hz)	Pin	V_{OUT} (V)	I_{OUT} (A)	P_o (W)	Efficiency (%)	4-pt Average efficiency (%)	CoC T2	DOE 6	Full load switching frequency (kHz)
1	90	47	7.180	19.967	0.327	6.531	90.957	–	79	–	102
2	90	47	17.630	19.963	0.816	16.285	92.373	92.58	89	88	
3	90	47	35.140	19.954	1.632	32.568	92.681				
4	90	47	52.550	19.944	2.447	48.808	92.879				
5	90	47	70.410	19.934	3.264	65.057	92.397				
6	115	60	7.170	19.968	0.327	6.533	91.116	–	79	–	162
7	115	60	17.530	19.966	0.816	16.290	92.924	93.48	89	88	
8	115	60	34.830	19.955	1.632	32.571	93.515				
9	115	60	52.030	19.945	2.447	48.813	93.816				
10	115	60	69.460	19.935	3.263	65.057	93.661				
11	230	50	7.350	19.964	0.327	6.530	88.848	–	79	–	129
12	230	50	17.580	19.961	0.816	16.290	92.665	93.68	89	88	
13	230	50	34.710	19.950	1.632	32.564	93.818				
14	230	50	51.910	19.935	2.448	48.792	93.994				
15	230	50	68.990	19.926	3.264	65.029	94.259				
16	265	63	7.370	19.963	0.327	6.532	88.627	–	79	–	132
17	265	63	17.610	19.959	0.816	16.287	92.488	93.64	89	88	
18	265	63	34.720	19.948	1.632	32.562	93.784				
19	265	63	51.930	19.934	2.447	48.787	93.948				
20	265	63	68.940	19.925	3.264	65.029	94.327				

1. *CoC Tier 2 limit for 4-pt Average is 89%*
2. *CoC Tier 2 limit for 10% load is 79%*

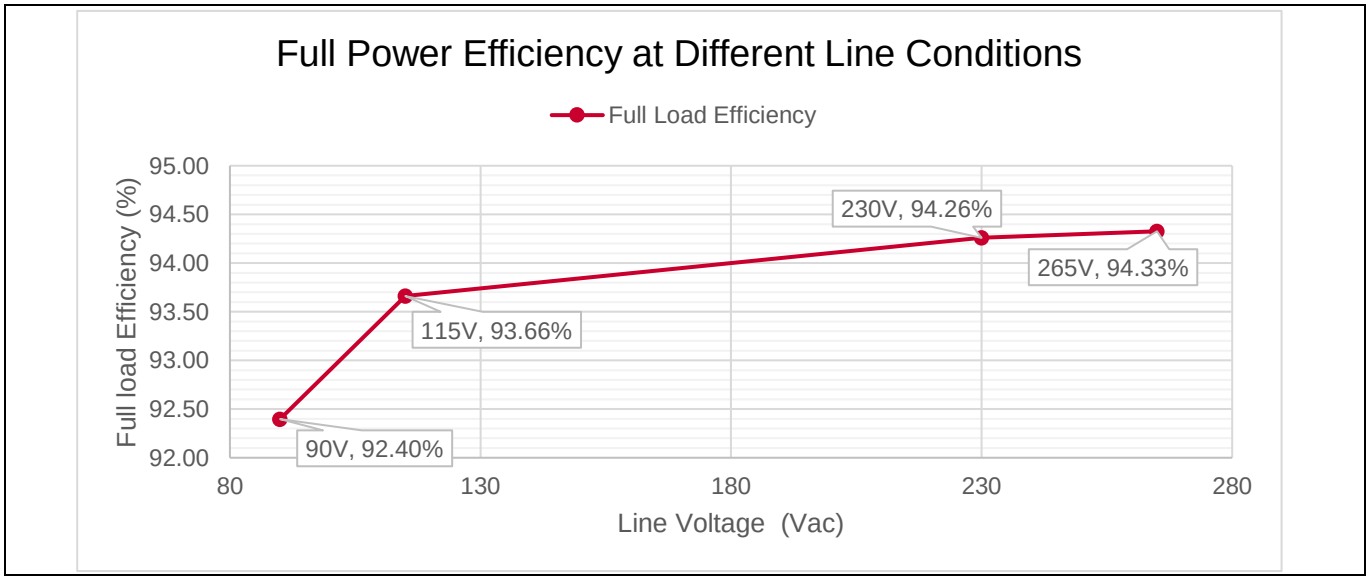


Figure 13 Full power efficiency at different line conditions

3.2 Standby power consumption

Table 13 Standby power consumption across line conditions

VIN (VAC)	90 VAC, 47 Hz	115 VAC, 60 Hz	230 VAC, 50 Hz	265 VAC, 63 Hz
Input power (mW)	24 mW	24 mW	28 mW	28 mW

Note: There should be 15 minutes of warmup time before starting to measure standby power.

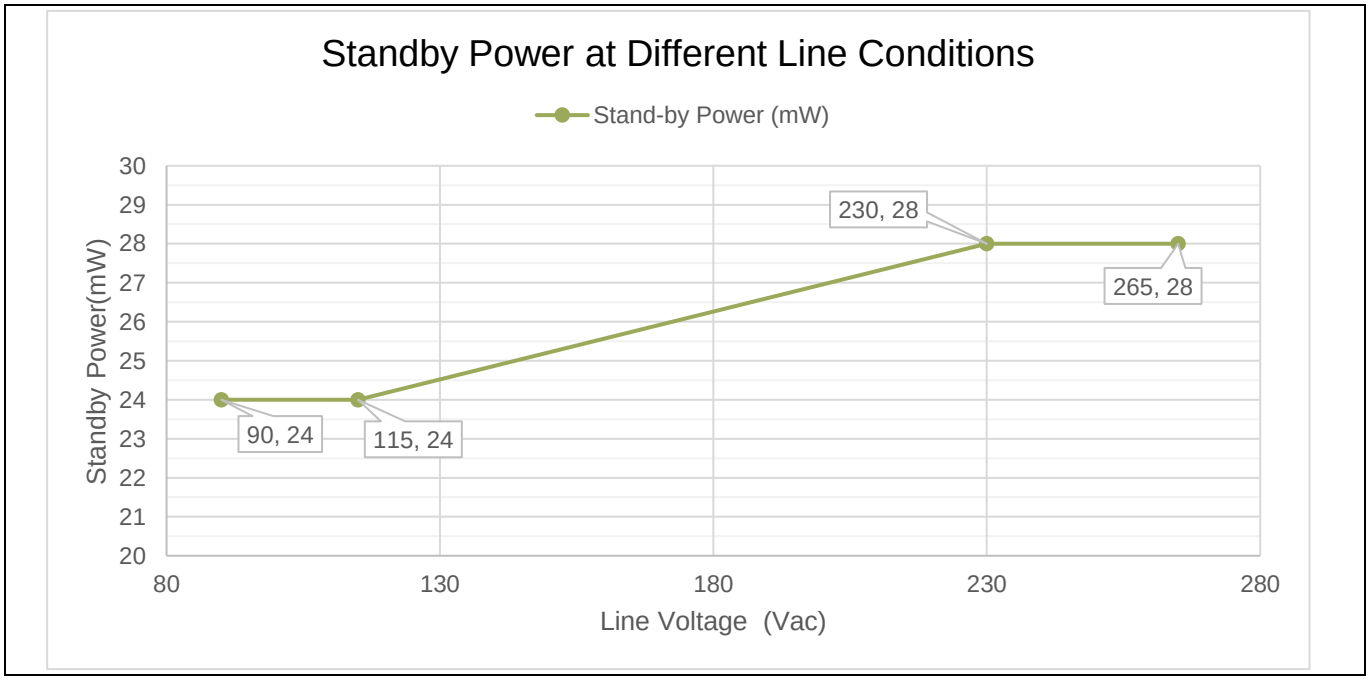


Figure 14 Standby power consumption

Note: The measurement was taken using WTViewerEfree software with line filter ON.

3.3 Output voltage and current regulation

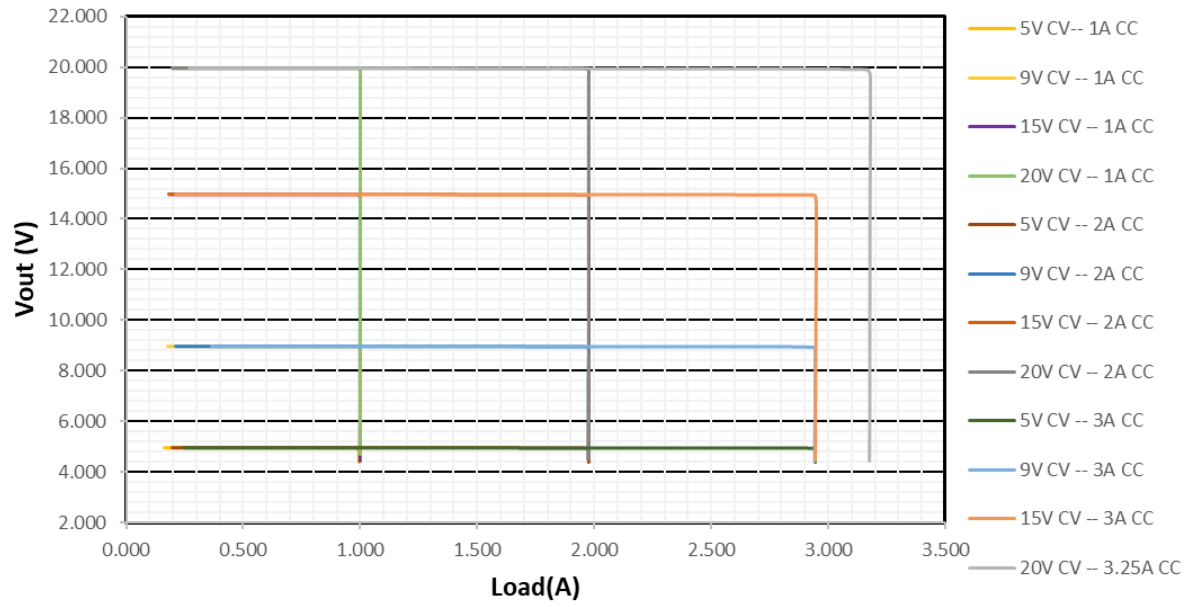


Figure 15 CV-CC regulation curve at 115 V_{AC} 60 Hz

Table 14 CC limits 115 V_{AC} 60 Hz

	1 A	2 A	3 A	3.25 A
5 V	0.996	1.976	2.945	N/A
9 V	0.997	1.977	2.947	N/A
15 V	0.998	1.980	2.952	NA/
20 V	1.000	1.982	2.952	3.184

Power management test results

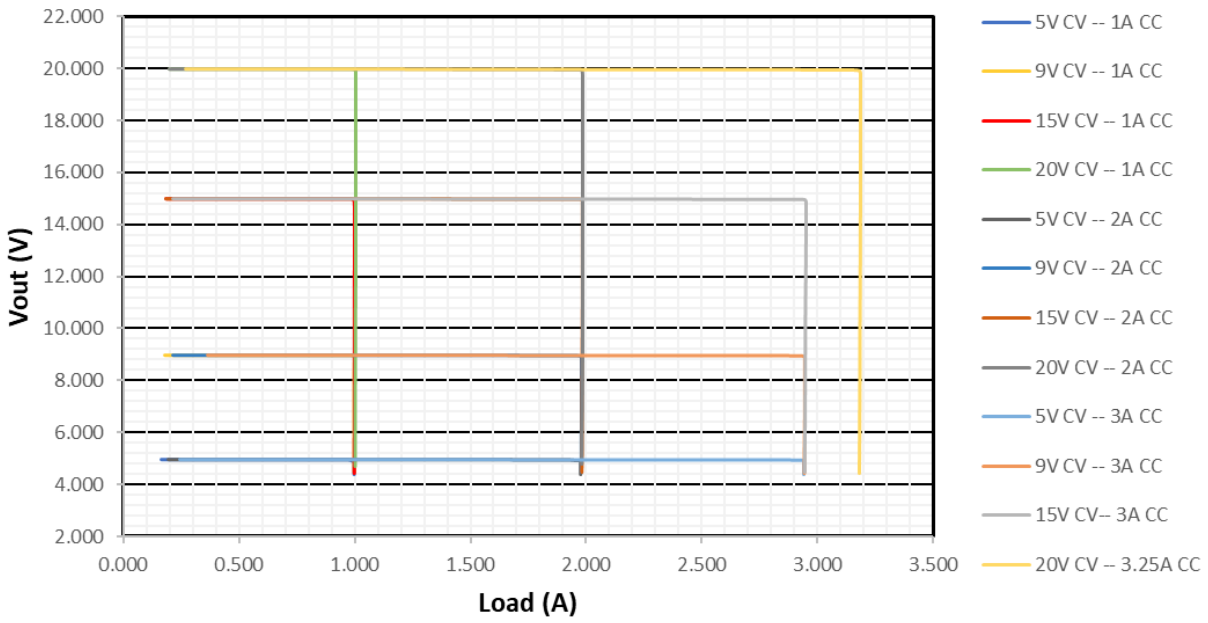


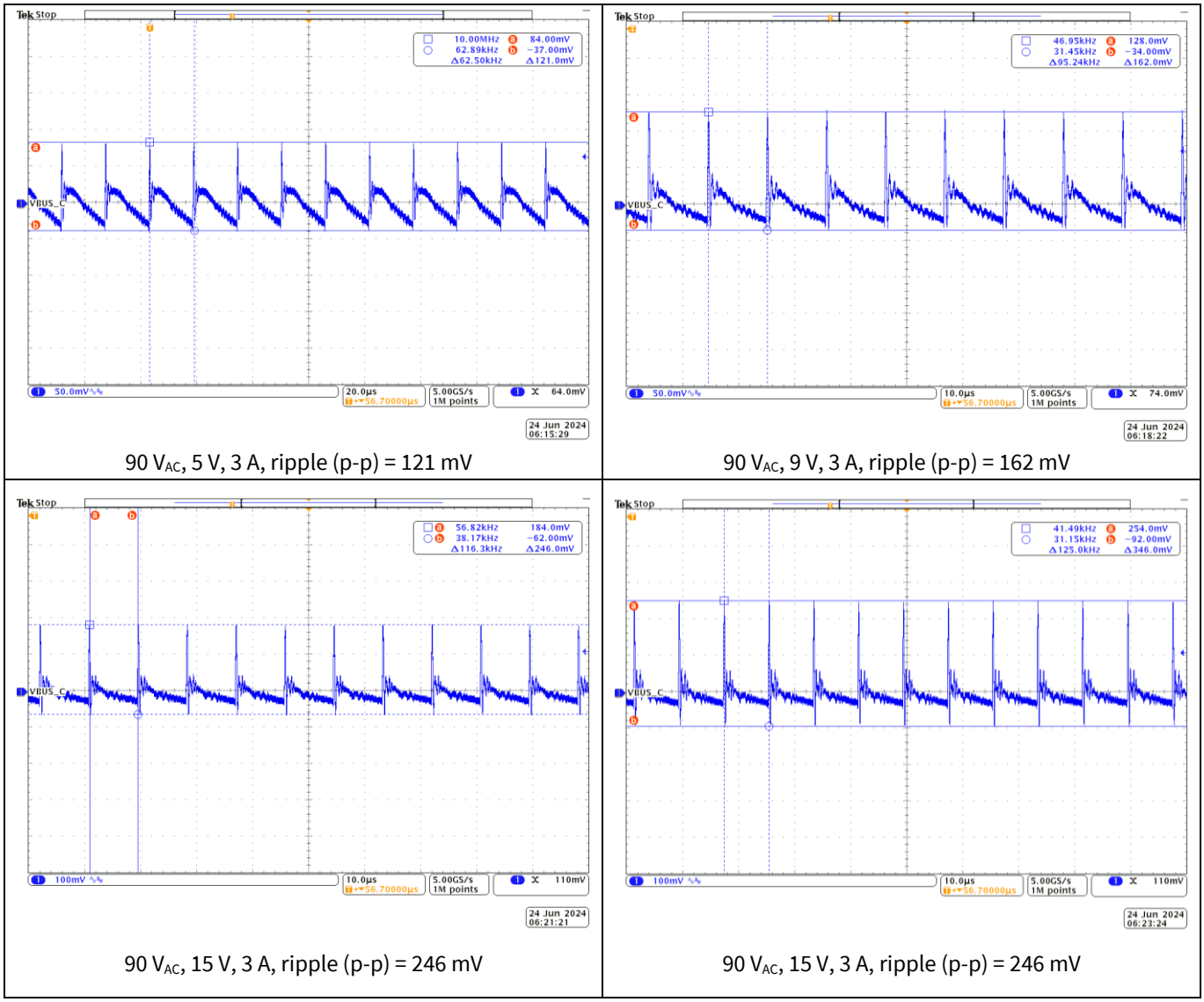
Figure 16 CV-CC regulation curve at 230 V_{AC} 50 Hz

Table 15 CC limits 230 V_{AC} 50 Hz

	1 A	2 A	3 A	3.25 A
5V	0.999	1.975	2.945	NA
9V	0.999	1.977	2.947	NA
15V	1.001	1.981	2.952	NA
20V	1.003	1.987	2.956	3.189

3.4 Output voltage ripple peak-peak

Note: Ripple measurement is done at board end using LeCroy probe adapter pk6-5mm-105.



90 V_{AC}, 5 V, 3 A, ripple (p-p) = 121 mV

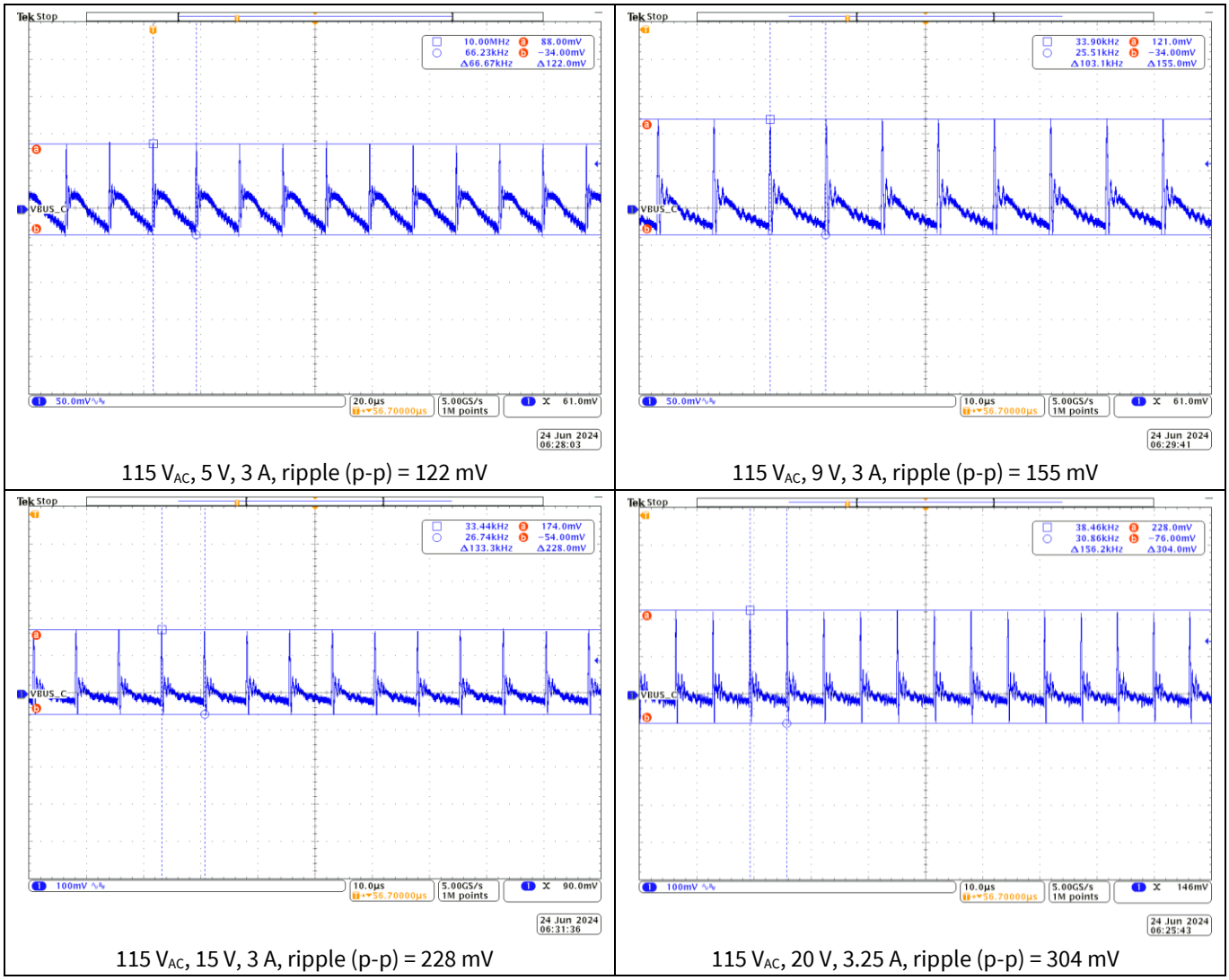
90 V_{AC}, 9 V, 3 A, ripple (p-p) = 162 mV

90 V_{AC}, 15 V, 3 A, ripple (p-p) = 246 mV

90 V_{AC}, 15 V, 3 A, ripple (p-p) = 246 mV

Figure 17 Ripple at 90 V_{AC} 47 Hz (CH1: V_{BUS_C})

Power management test results



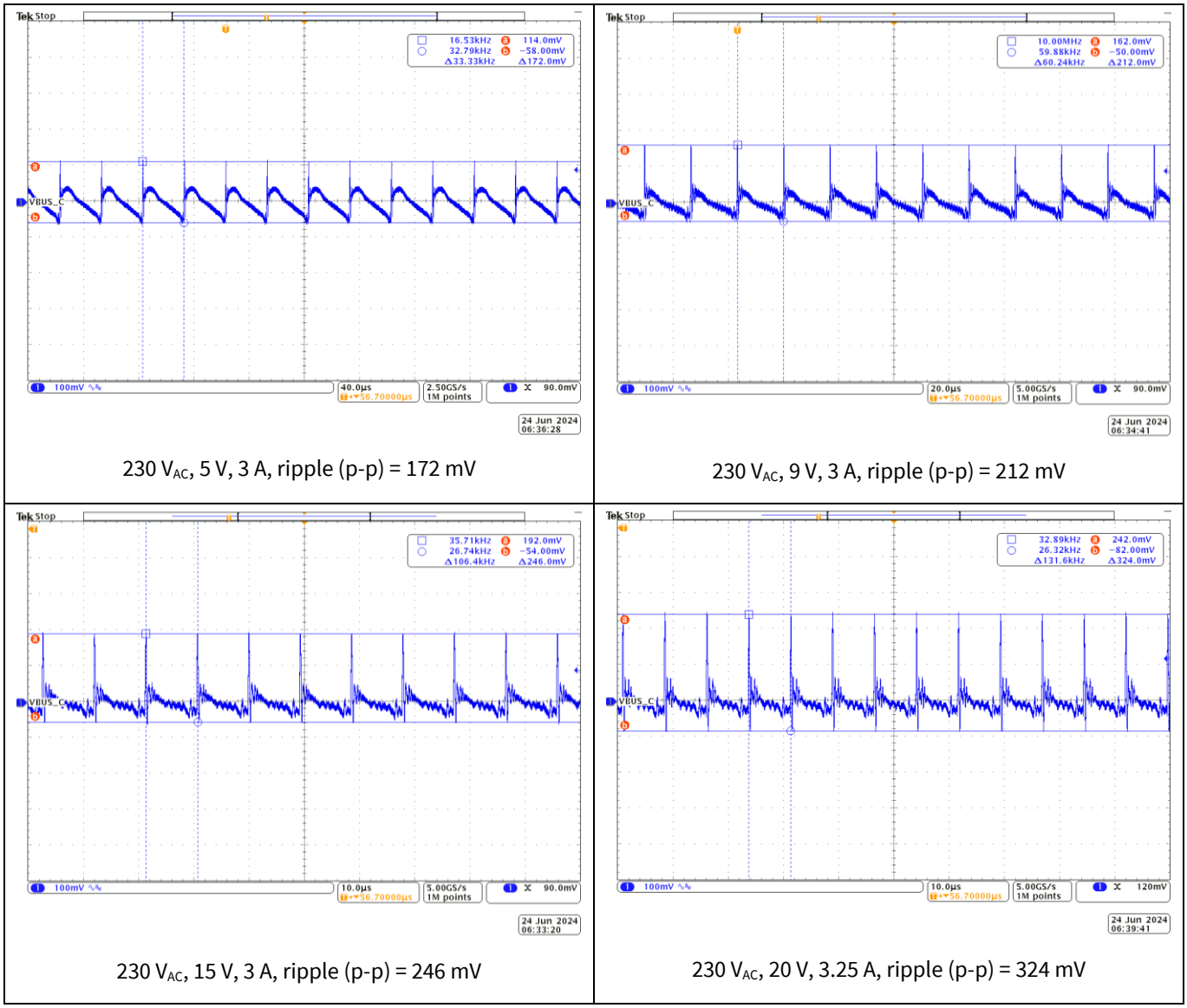
115 V_{AC}, 5 V, 3 A, ripple (p-p) = 122 mV

115 V_{AC}, 9 V, 3 A, ripple (p-p) = 155 mV

115 V_{AC}, 15 V, 3 A, ripple (p-p) = 228 mV

115 V_{AC}, 20 V, 3.25 A, ripple (p-p) = 304 mV

Figure 18 Ripple at 115 V_{AC} 60 Hz (CH3: V_{BUS_C})



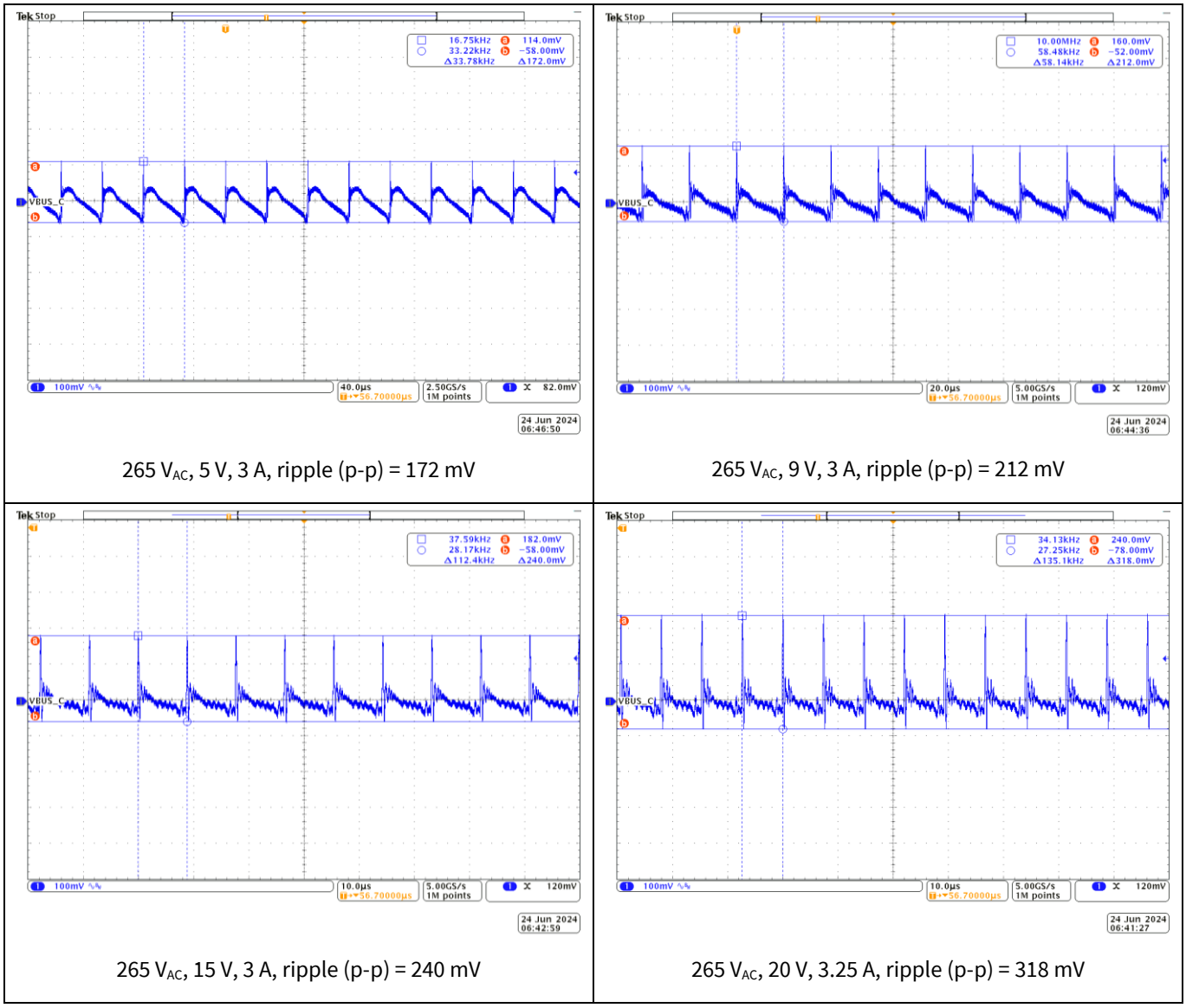
230 V_{AC}, 5 V, 3 A, ripple (p-p) = 172 mV

230 V_{AC}, 9 V, 3 A, ripple (p-p) = 212 mV

230 V_{AC}, 15 V, 3 A, ripple (p-p) = 246 mV

230 V_{AC}, 20 V, 3.25 A, ripple (p-p) = 324 mV

Figure 19 Ripple at 230 V_{AC} 50Hz (CH1: V_{BUS_C})



265 V_{AC}, 5 V, 3 A, ripple (p-p) = 172 mV

265 V_{AC}, 9 V, 3 A, ripple (p-p) = 212 mV

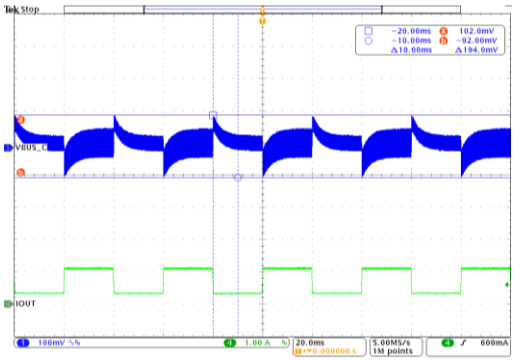
265 V_{AC}, 15 V, 3 A, ripple (p-p) = 240 mV

265 V_{AC}, 20 V, 3.25 A, ripple (p-p) = 318 mV

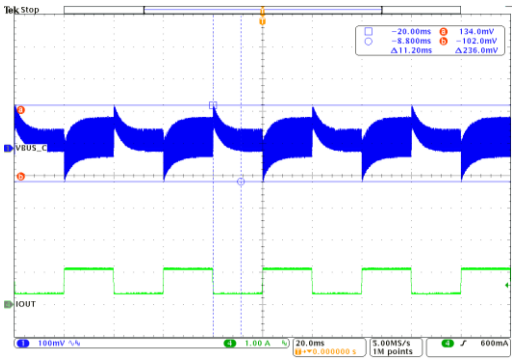
Figure 20 Ripple at 265 V_{AC} 63 Hz (CH1: V_{BUS_C})

Note: Waveforms have been taken by keeping the oscilloscope in 20 MHz bandwidth limitation.

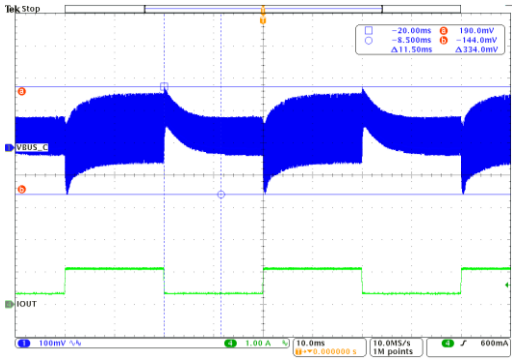
3.5 Output dynamic response settling time



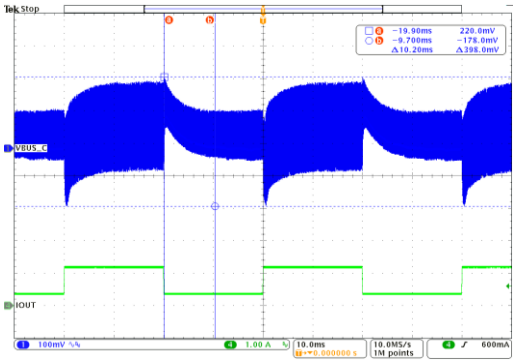
5 V – 0.3 A to 1.05 A, settling time = 10 ms



9 V – 0.3 A to 1.05 A, settling time = 11.2 ms

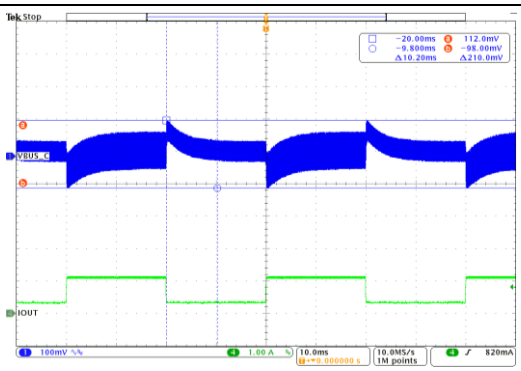


15 V – 0.3 A to 1.05 A, settling time = 11.5ms

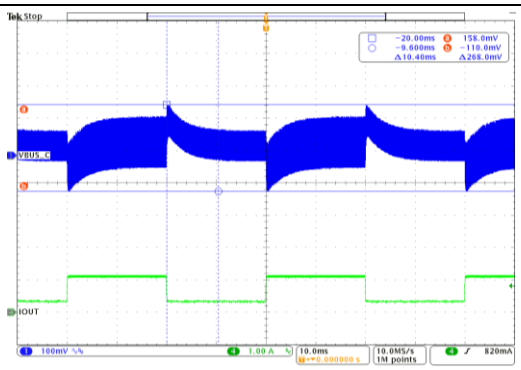


20 V – 0.325 A to 1.14 A, settling time = 10.2 ms

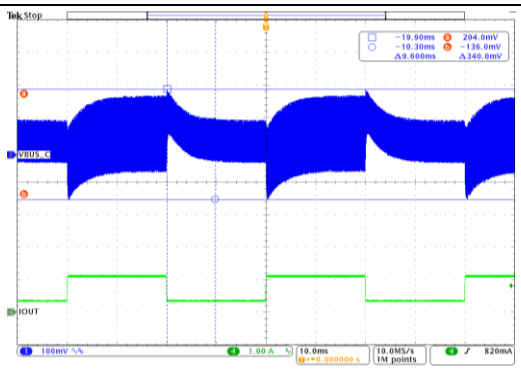
Figure 21 Settling time for 115 V_{AC}, 60 Hz load transition 10% to 35% load (CH1: V_{BUS_C}, CH4: I_{OUT})



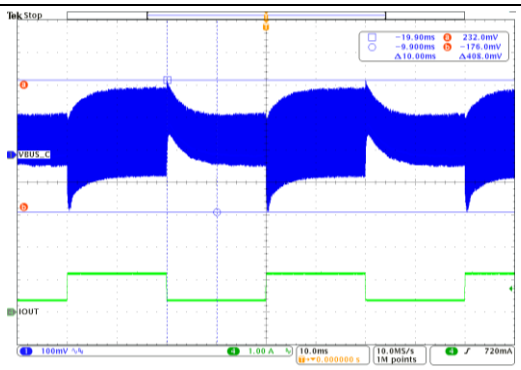
5 V – 0.3 A to 1.05 A, settling time = 10.2 ms



9 V – 0.3 A to 1.05 A, settling time = 10.4 ms

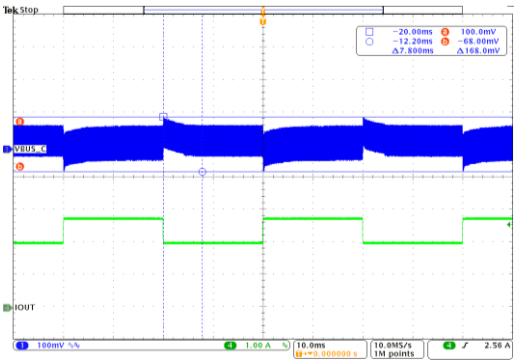


15 V – 0.3 A to 1.05 A, settling time = 9.6 ms

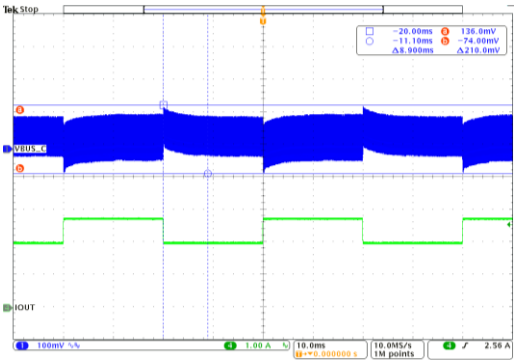


20 V – 0.325 A to 1.14 A, settling time = 10 ms

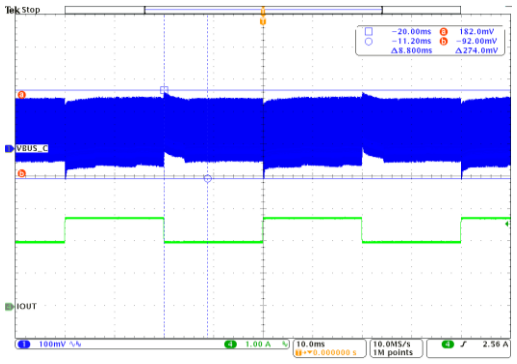
Figure 22 Settling time for 230 V_{AC}, 50 Hz load transition 10% to 35% load (CH1: V_{BUS_C}, CH4: I_{OUT})



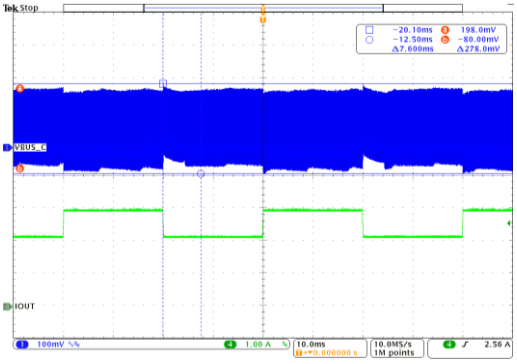
5 V – 1.95 A to 2.7 A, settling time = 7.8 ms



9 V – 1.95 A to 2.7 A, settling time = 8.9 ms

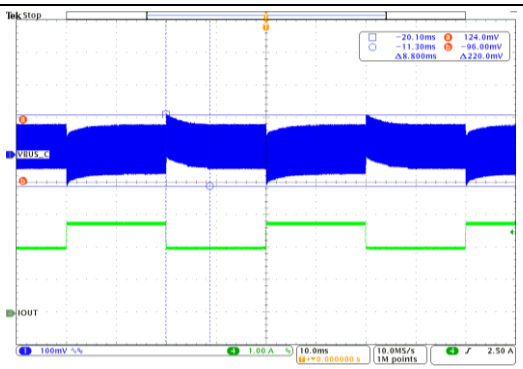


15 V – 1.95 A to 2.7 A, settling time = 8.8 ms

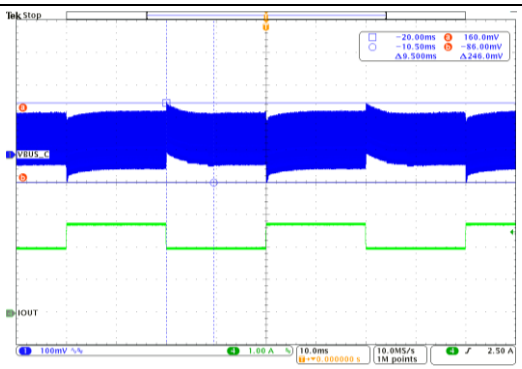


20 V – 2.11 A to 2.93 A, settling time = 4.24 ms

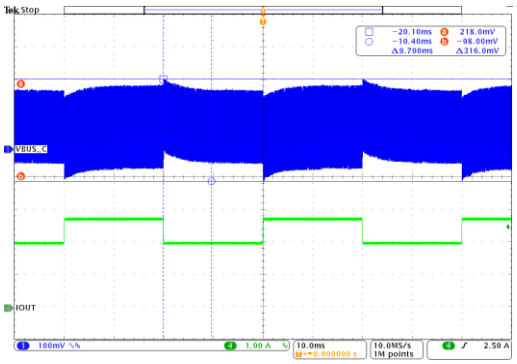
Figure 23 Settling time for 115 V_{AC}, 60 Hz load transition 65% to 90% load (CH1: V_{BUS_C}, CH4: I_{OUT})



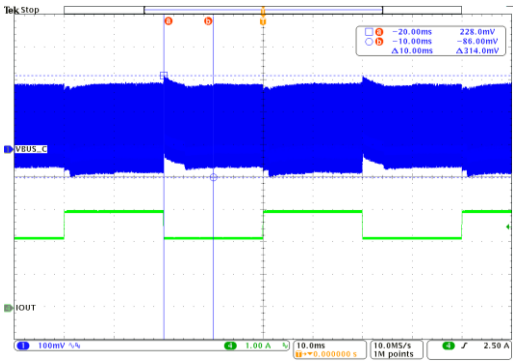
5 V – 1.95A to 2.7A, settling time = 8.8ms



9 V – 1.95 A to 2.7 A, settling time = 9.5ms

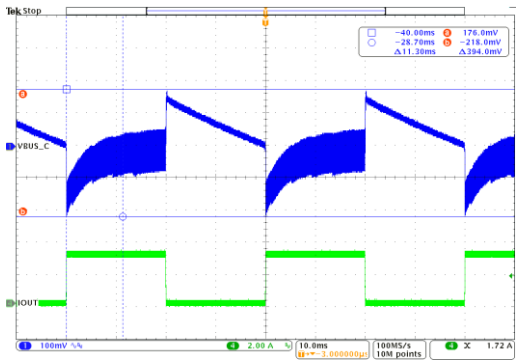


15V – 1.95A to 2.7A, settling time = 9.7ms

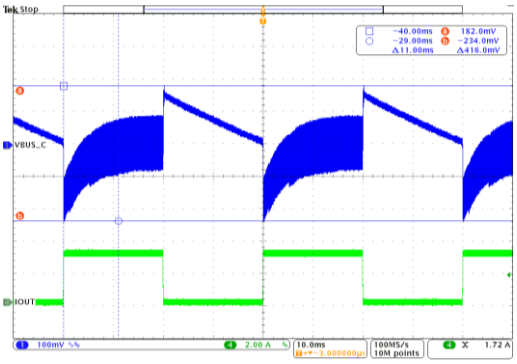


20V – 2.11A to 2.93A, settling time = 6.68ms

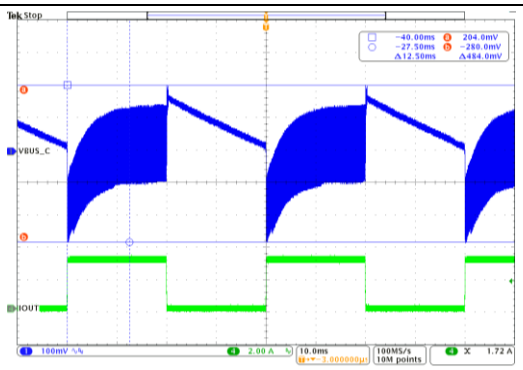
Figure 24 Settling time for 230 V_{AC}, 50 Hz load transition 65% to 90% load (CH1: V_{BUS_C}, CH4: I_{OUT})



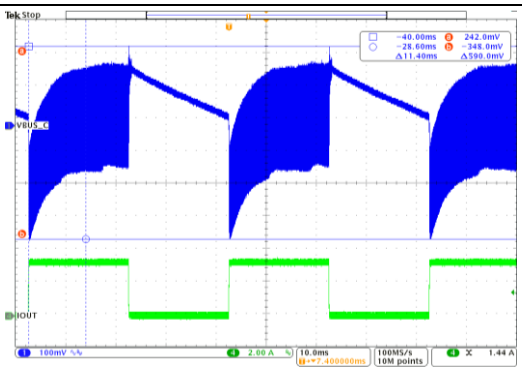
5 V – 0 A to 3 A, settling time = 11.3 ms



9 V – 0 A to 3 A, settling time = 11 ms

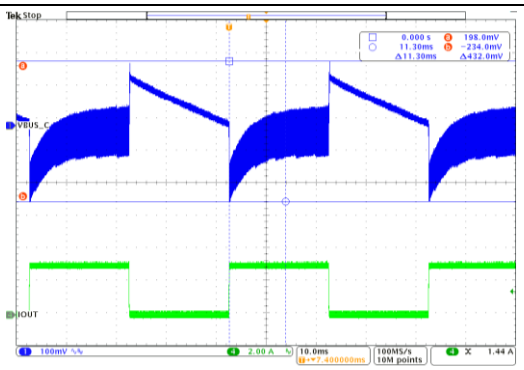


15 V – 0 A to 3 A, settling time = 12.5 ms

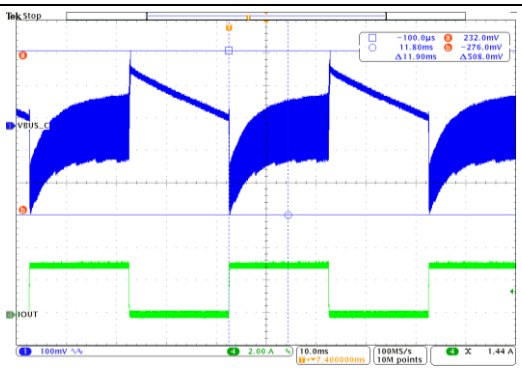


20 V – 0 A to 3.25 A, settling time = 11.4 ms

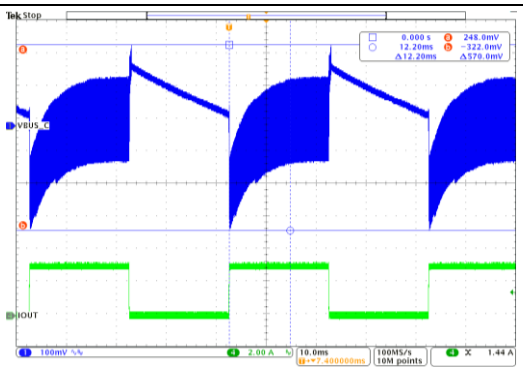
Figure 25 Settling time for 115 V_{AC}, 60 Hz load transition 0% to 100% load (CH1: V_{BUS_C}, CH4: I_{OUT})



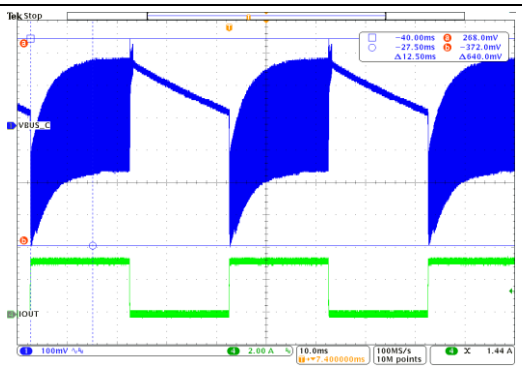
5 V – 0 A to 3 A, settling time = 11.3 ms



9 V – 0 A to 3 A, settling time = 11.9 ms



15 V – 0 A to 3 A, settling time = 12.2 ms



20 V – 0 A to 3.25 A, settling time = 12.5 ms

Figure 26 Settling time for 230 V_{AC}, 50 Hz load transition 0% to 100% load (CH1: V_{BUS_C}, CH4: I_{OUT})

3.6 Output current overshoot and settling time

I_O overshoot tested at 115 V_{AC}, 60 Hz

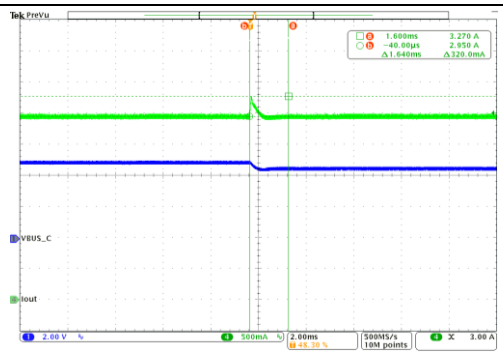
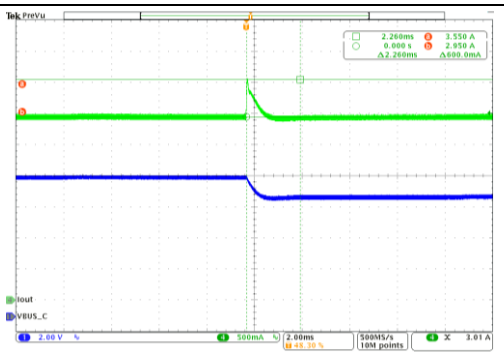
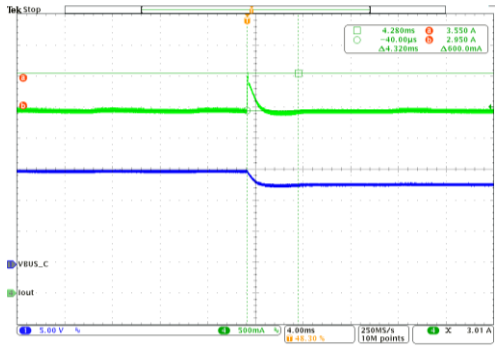
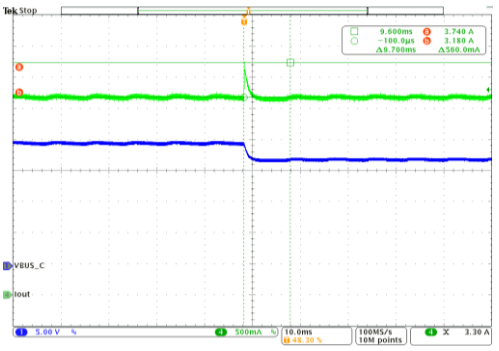
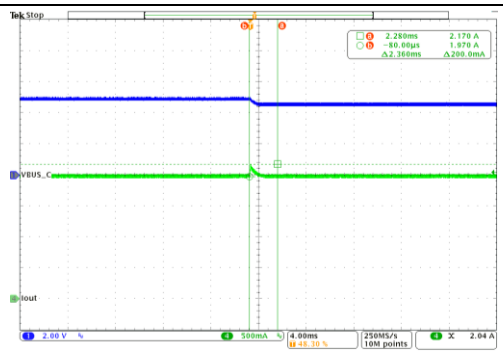
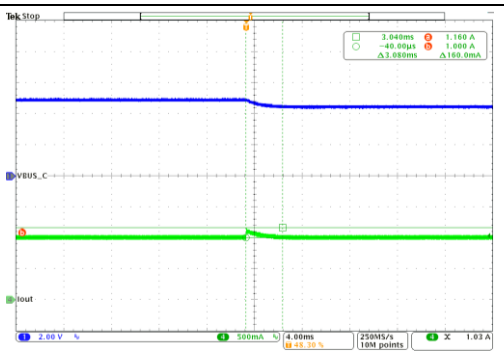
 V_O = 5 V; I_O = 3.1 A to 3.35 A I_O (limit) = 3 A; (CR Mode*: R = 1.581 Ω to 1.452 Ω) I_O overshoot = 320 mA, settling time = 1.64 ms	 V_O = 9 V; I_O = 3.1 A to 3.6 A I_O (limit) = 3 A; (CR Mode*: R = 2.93 Ω to 2.497 Ω) I_O overshoot = 600 mA, settling time = 2.26 ms
 V_O = 15 V; I_O = 3.1 A to 3.6 A I_O (limit) = 3 A; (CR Mode*: R = 4.901 Ω to 4.191 Ω) I_O overshoot = 600 mA, settling time = 4.32 ms	 V_O = 20 V; I_O = 3.35 A to 3.85 A I_O (limit) = 3.25 A; (CR Mode*: R = 6.05 Ω to 5.231 Ω) I_O overshoot = 560 mA, settling time = 9.7 ms
 V_O = 5 V; I_O = 2.1 A to 2.25 A I_O (limit) = 2 A; (CR Mode*: R = 2.388 Ω to 2.219 Ω) I_O overshoot = 200 mA, settling time = 2.36 ms	 V_O = 5 V; I_O = 1.1 A to 1.2 A I_O (limit) = 1 A; (CR Mode*: R = 4.789 Ω to 4.357 Ω) I_O overshoot = 160 mA, settling time = 3.08 ms

Figure 27 I_O overshoot and settling time for 115 V_{AC}, 60 Hz (CH1: I_{OUT}, CH4: V_{BUS_C})

***CR Mode**: This is the mode the Electronic load (E-load) should be set at. The resistance value mentioned is specific to E-loads and length of the cable used from E-load to the DUT end.

Io overshoot tested at 230 V_{AC}, 50 Hz

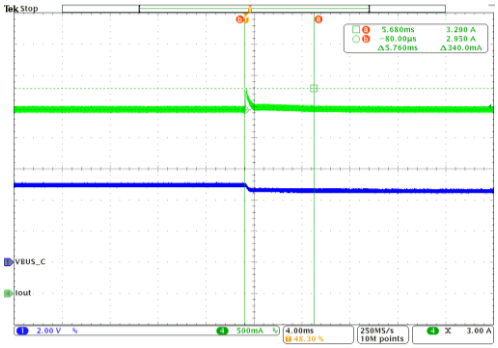
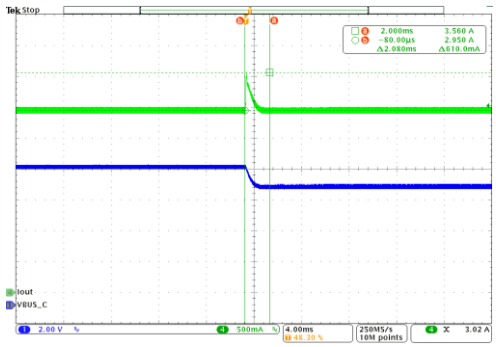
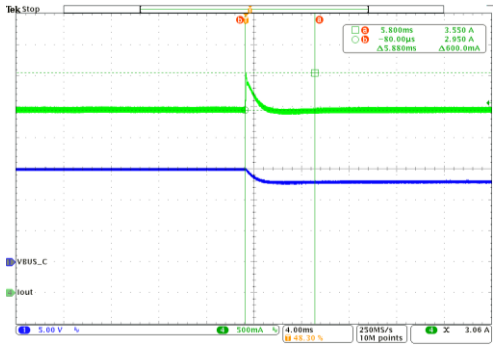
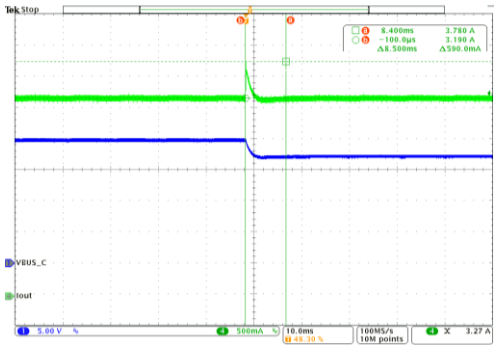
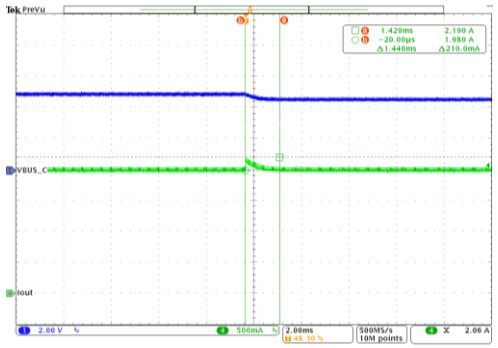
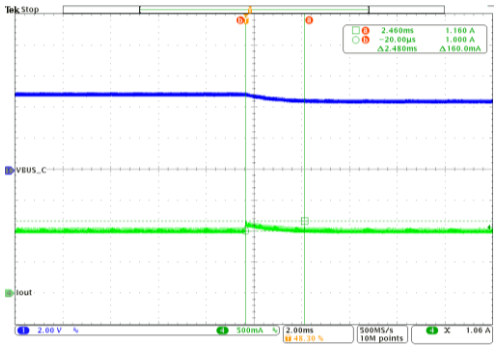
 V_O = 5 V; I_O = 3.1 A to 3.35 A I_O (limit) = 3 A; (CR Mode*: R = 1.581 Ω to 1.451 Ω) I_O overshoot = 340 mA, settling time = 5.76 ms	 V_O = 9 V; I_O = 3.1 A to 3.6 A I_O (limit) = 3 A; (CR Mode*: R = 2.93 Ω to 2.495 Ω) I_O overshoot = 610 mA, settling time = 2.08 ms
 V_O = 15 V; Io= 3.1 A to 3.6 A I_O (limit) = 3 A; (CR Mode*: R = 4.901 Ω to 4.195 Ω) I_O overshoot = 600 mA, settling time = 5.88 ms	 V_O = 20 V; I_O = 3.35 A to 3.85 A I_O (limit) = 3.25 A; (CR Mode*: R = 6.05 Ω to 5.234 Ω) I_O overshoot = 590 mA, settling time = 8.5 ms
 V_O = 5 V; I_O = 2.1 A to 2.25 A I_O (limit) = 2 A; (CR Mode*: R = 2.388 Ω to 2.217 Ω) I_O overshoot = 210 mA, settling time = 1.44 ms	 V_O = 5 V; I_O = 1.1 A to 1.2 A I_O (limit) = 1A; (CR Mode*: R = 4.789 Ω to 4.355 Ω) I_O overshoot = 160 mA, settling time = 2.48 ms

Figure 28 I_O overshoot and settling time for 230 V_{AC}, 50 Hz (CH1: I_{OUT}, CH4: V_{BUS_C})

*__CR Mode__: This is the mode the Electronic load (E-load) should be set at. The resistance value mentioned is specific to E-loads and length of the cable used from E-load to the DUT end.

3.7 Output current undershoot and settling time

I_O undershoot tested at 115 V_{AC}, 60 Hz

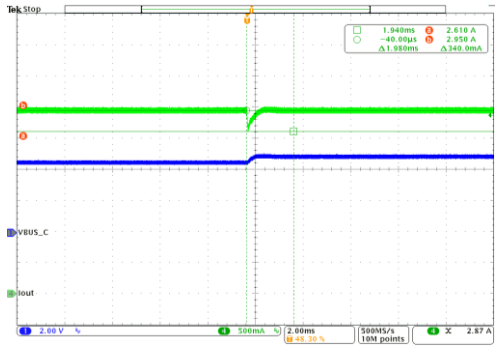
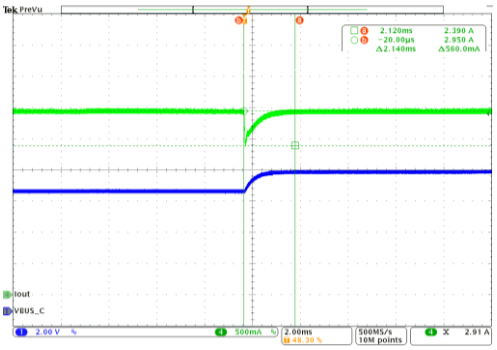
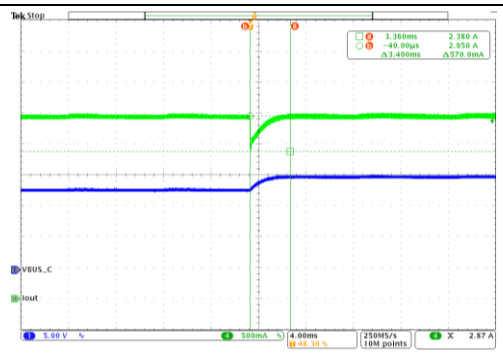
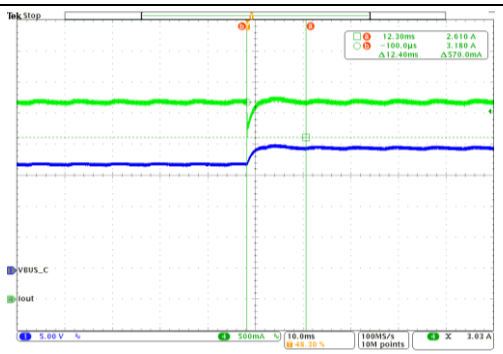
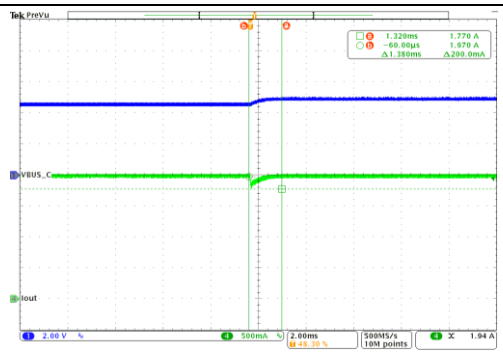
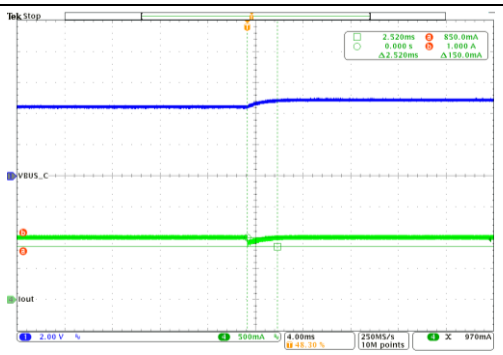
 V_O = 5 V; I_O = 3.35 A to 3.1 A I_O (limit) = 3 A; (CR Mode*: R = 1.452 Ω to 1.581 Ω) I_O undershoot = 340 mA, settling time = 1.98 ms	 V_O = 9 V; I_O = 3.6 A to 3.1 A Io(limit) = 3 A; (CR Mode*: R = 2.497 Ω to 2.93 Ω) Io undershoot = 560 mA, settling time = 2.14 ms
 V_O = 15 V; I_O = 3.6 A to 3.1 A I_O (limit) = 3 A; (CR Mode*: R = 4.191 Ω to 4.901 Ω) I_O undershoot = 570 mA, settling time = 3.4 ms	 V_O = 20V; I_O = 3.85A to 3.35A I_O (limit) = 3.25A; (CR Mode*: R = 5.231 Ω to 6.05 Ω) I_O undershoot = 570 mA, settling time = 12.4 ms
 V_O = 5 V; I_O = 2.25 A to 2.1 A I_O (limit) = 2 A; (CR Mode*: R = 2.219 Ω to 2.388 Ω) I_O undershoot = 200 mA, settling time = 1.38 ms	 V_O = 5 V; I_O = 1.2 A to 1.1 A I_O (limit) = 1 A; (CR Mode*: R = 4.357 Ω to 4.789 Ω) I_O undershoot = 150 mA, settling time = 2.52 ms

Figure 29 I_O undershoot and settling time for 115 V_{AC}, 60 Hz (CH1: I_{OUT}, CH4: V_{BUS_C})

I_O undershoot tested at 230 V_{AC}, 50 Hz

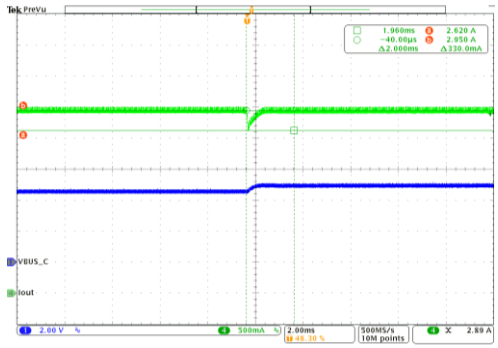
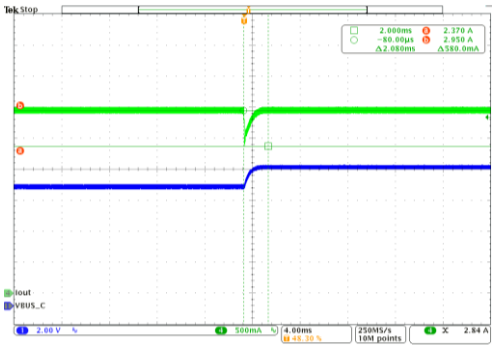
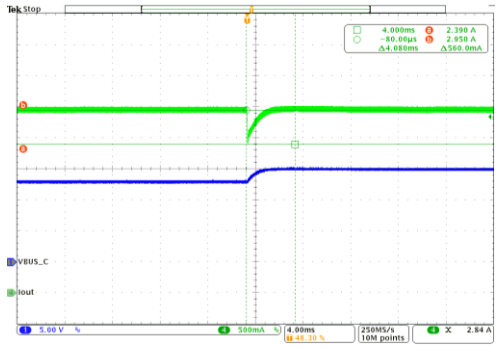
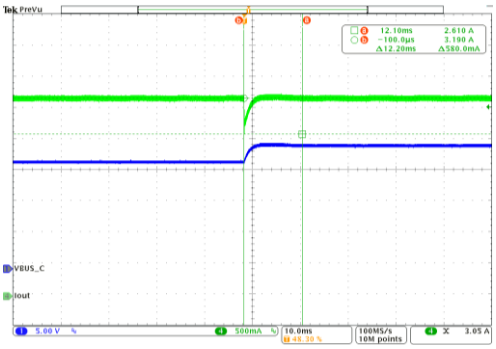
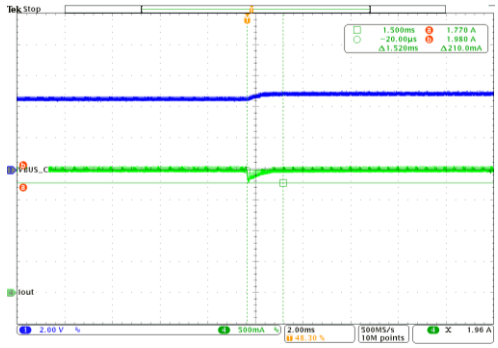
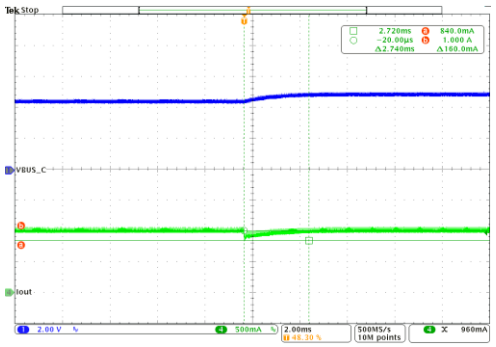
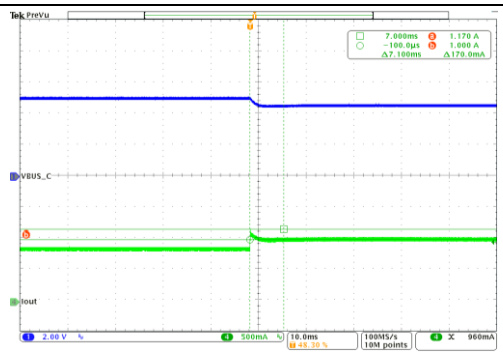
 V_O = 5 V; I_O = 3.35 A to 3.1 A I_O (limit) = 3 A; (CR Mode*: R = 1.451 Ω to 1.581 Ω) I_O undershoot = 330 mA, settling time = 2 ms	 V_O = 9 V; I_O = 3.6 A to 3.1 A I_O (limit) = 3 A; (CR Mode*: R = 2.495 Ω to 2.93 Ω) I_O undershoot = 580 mA, settling time = 2.08 ms
 V_O = 15 V; I_O = 3.6 A to 3.1 A I_O (limit) = 3 A; (CR Mode*: R = 4.195 Ω to 4.901 Ω) I_O undershoot = 560 mA, settling time = 4.08 ms	 V_O = 20 V; I_O = 3.85 A to 3.35 A I_O (limit) = 3.25A; (CR Mode*: R = 5.234 Ω to 6.05 Ω) I_O undershoot = 580 mA, settling time = 12.2 ms
 V_O = 5 V; I_O = 2.25 A to 2.1 A I_O (limit) = 2 A; (CR Mode*: R = 2.217 Ω to 2.388 Ω) I_O undershoot = 210 mA, settling time = 1.52 ms	 V_O = 5 V; I_O = 1.2 A to 1.1 A I_O (limit) = 1 A; (CR Mode*: R = 4.355 Ω to 4.789 Ω) I_O undershoot = 160 mA, settling time = 2.74 ms

Figure 30 I_O undershoot and settling time for 230 V_{AC}, 50 Hz (CH1: I_{OUT}, CH4: V_{BUS_C})

***CR Mode**: This is the mode the Electronic load (E-load) should be set at. The resistance value mentioned is specific to E-loads and length of the cable used from E-load to the DUT end.

3.8 CV-CC transition time

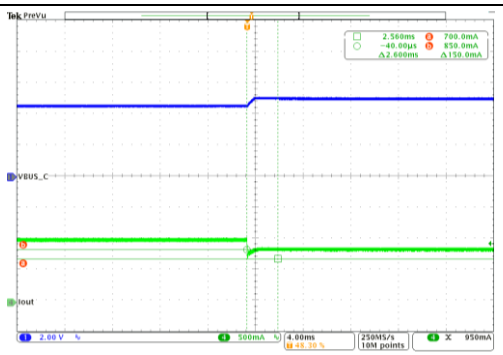
CV-CC transition tested at 115 V_{AC}, 60 Hz



V_O = 5 V; I_O = 0.85 A to 1.1 A

I_O (limit) = 1 A; (CR Mode*: R = 5.773 Ω to 4.435 Ω)

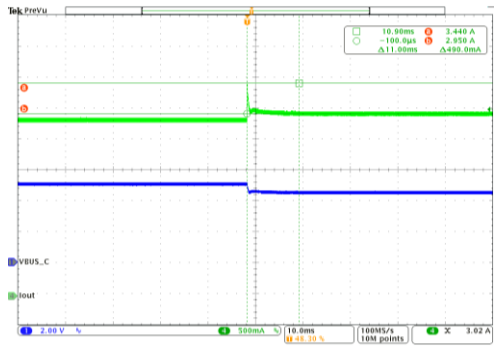
I_O overshoot = 170 mA; settling time = 7.1 ms



V_O = 5 V; I_O = 1.1 A to 0.85 A

I_O (limit) = 1 A; (CR Mode*: R = 4.435 Ω to 5.773 Ω)

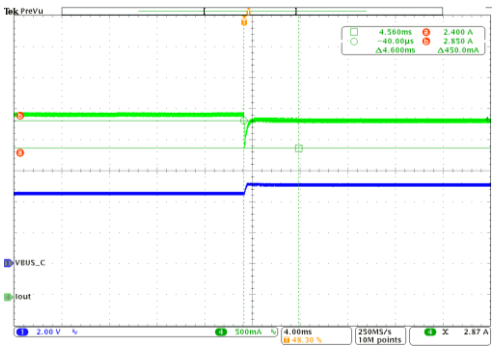
I_O undershoot = 150 mA; settling time = 2.6 ms



V_O = 5 V; I_O = 2.85 A to 3.35 A

I_O (limit) = 3 A; (CR Mode*: R = 1.663 Ω to 1.419 Ω)

I_O overshoot = 490mA; settling time = 11ms



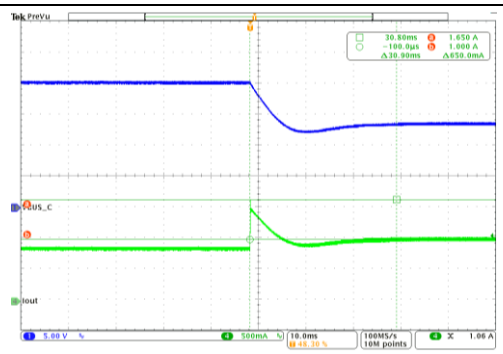
V_O = 5V; I_O = 3.35A to 2.85A

I_O (limit) = 3A; (CR Mode*: R = 1.419 Ω to 1.663 Ω)

I_O undershoot = 450 mA; settling time = 4.6 ms

Figure 31 Output current dynamic response for 5 V output at 115 V_{AC}, 60 Hz (CH1: I_{OUT}, CH4: V_{BUS_C})

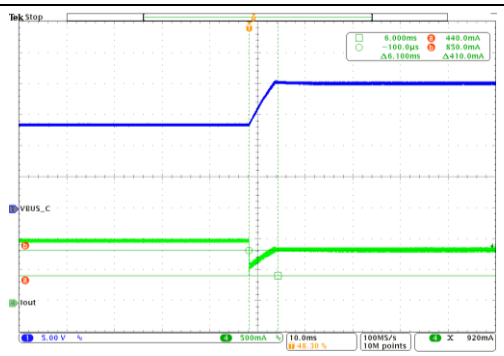
***CR Mode**: This is the mode the Electronic load (E-load) should be set at. The resistance value mentioned is specific to E-loads and length of the cable used from E-load to the DUT end.



V_O = 20 V; I_O = 0.85 A to 1.5 A

I_O (limit) = 1 A; (CR Mode*: R = 23.148 Ω to 13.1 Ω)

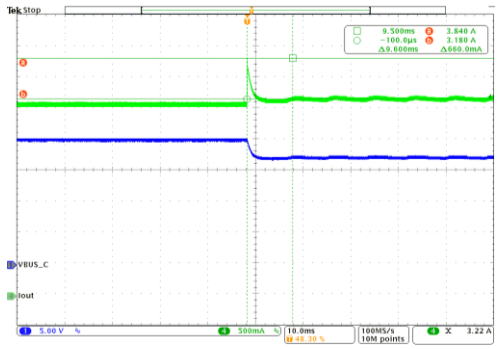
I_O overshoot = 650 mA; settling time = 30.9 ms



V_O = 20 V; I_O = 1.5 A to 0.85 A

I_O (limit) = 1 A; (CR Mode*: R = 13.1 Ω to 23.148 Ω)

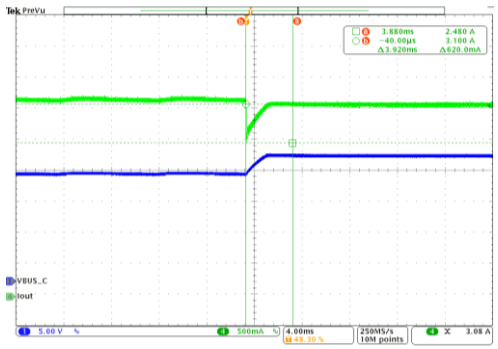
I_O undershoot = 410 mA; settling time = 6.1 ms



V_O = 20 V; I_O = 3.1 A to 3.75 A

I_O (limit) = 3.25 A; (CR Mode*: R = 6.345 Ω to 5.293 Ω)

I_O overshoot = 660 mA; settling time = 9.6 ms



V_O = 20 V; I_O = 3.75 A to 3.1 A

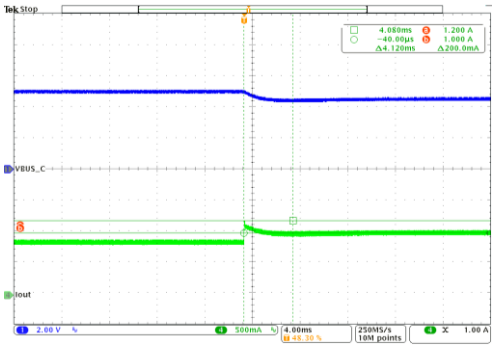
I_O (limit) = 3.25 A; (CR Mode*: R = 5.29 Ω to 6.345 Ω)

I_O undershoot = 620mA; settling time = 3.92 ms

Figure 32 Output current dynamic response for 20 V output at 115 V_{AC}, 60 Hz (CH1: I_{OUT}, CH4: V_{BUS_C})

***CR Mode**: This is the mode the Electronic load (E-load) should be set at. The resistance value mentioned is specific to E-loads and length of the cable used from E-load to the DUT end.

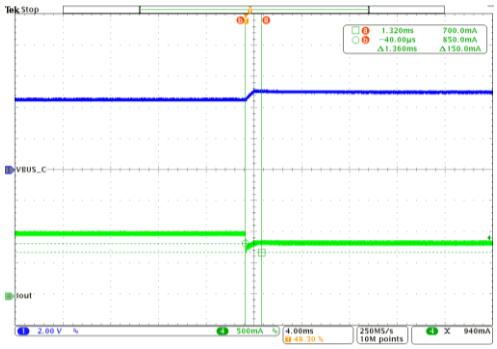
CV-CC transition tested at 230 V_{AC}, 50 Hz



V_O = 5 V; I_O = 0.85 A to 1.1 A

I_O (limit) = 1 A; (CR Mode*: R = 5.773 Ω to 4.409 Ω)

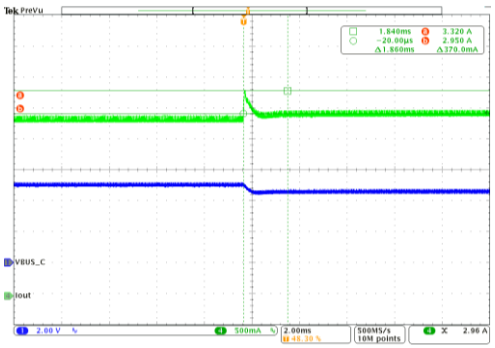
I_O overshoot = 200 mA; settling time = 4.12 ms



V_O = 5 V; I_O = 1.1 A to 0.85 A

I_O (limit) = 1 A; (CR Mode*: R = 4.409 Ω to 5.773 Ω)

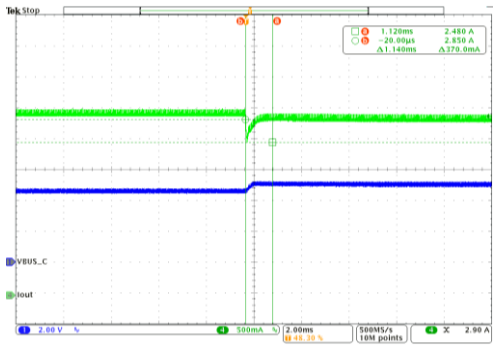
I_O undershoot = 150 mA; settling time = 1.36 ms



V_O = 5 V; I_O = 2.85 A to 3.25 A

I_O (limit) = 3 A; (CR Mode*: R = 1.663 Ω to 1.464 Ω)

I_O overshoot = 370mA; settling time = 1.86 ms



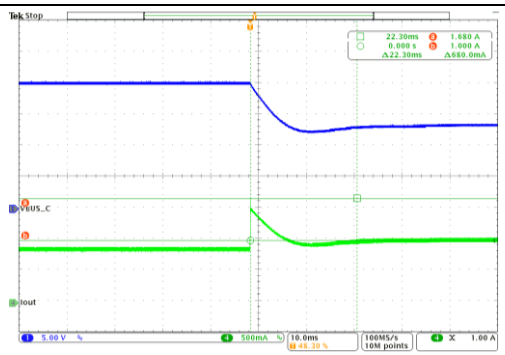
V_O = 5 V; I_O = 3.25 A to 2.85 A

I_O (limit) = 3 A; (CR Mode*: R = 1.464 Ω to 1.663 Ω)

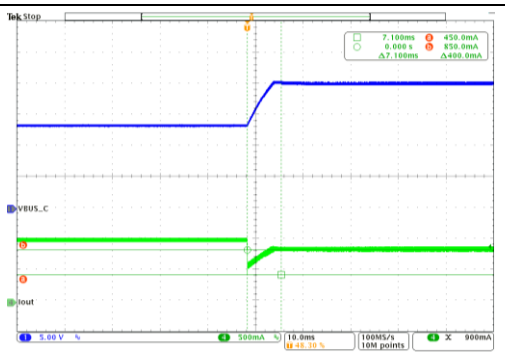
I_O undershoot = 370 mA; settling time = 1.14 ms

Figure 33 Output current dynamic response for 5 V output at 230 V_{AC}, 50 Hz (CH1: I_{OUT}, CH4: V_{BUS_C})

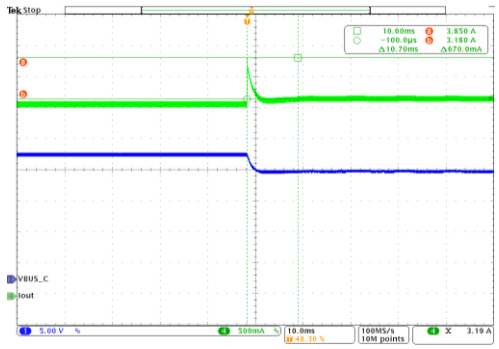
***CR Mode**: This is the mode the Electronic load (E-load) should be set at. The resistance value mentioned is specific to E-loads and length of the cable used from E-load to the DUT end.



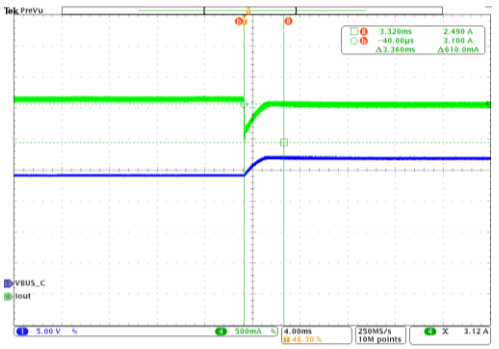
V_O = 20 V; I_O = 0.85 A to 1.5 A
I_O (limit) = 1 A; (CR Mode*: R = 23.148 Ω to 13 Ω)
I_O overshoot = 680 mA; settling time = 22.3 ms



V_O = 20 V; I_O = 1.5 A to 0.85 A
I_O (limit) = 1 A; (CR Mode*: R = 13 Ω to 23.148 Ω)
I_O undershoot = 400 mA; settling time = 7.1 ms



V_O = 20 V; I_O = 3.1 A to 3.75 A
I_O (limit) = 3.25 A; (CR Mode*: R = 6.345 Ω to 5.276 Ω)
I_O overshoot = 670 mA; settling time = 10.7 ms

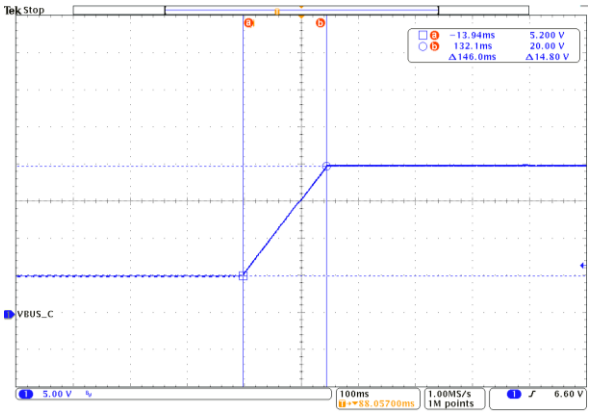


V_O = 20 V; I_O = 3.75 A to 3.1 A
I_O (limit) = 3.25 A; (CR Mode*: R = 5.27 Ω to 6.345 Ω)
I_O undershoot = 610 mA; settling time = 3.36 ms

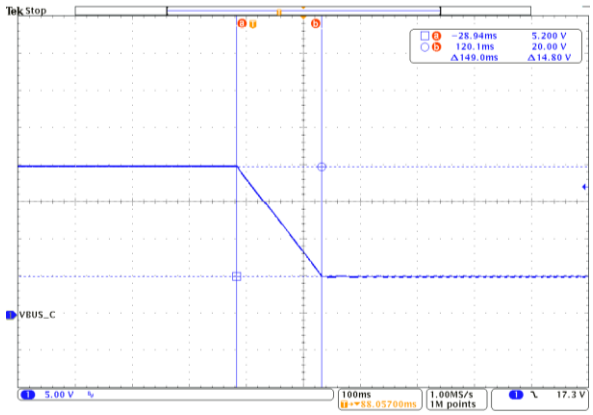
Figure 34 Output current dynamic response for 20V output at 230 V_{AC}, 50 Hz (CH1: I_{OUT}, CH4: V_{BUS_C})

***CR Mode**: This is the mode the Electronic load (E-load) should be set at. The resistance value mentioned is specific to E-loads and length of the cable used from E-load to the DUT end.

3.9 Output voltage transfer transition

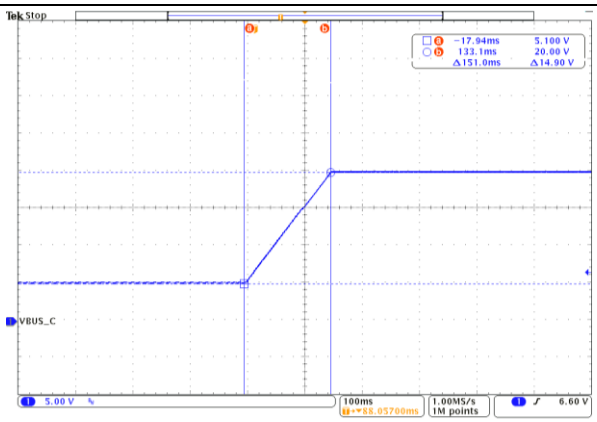


V_{OUT} = 5 V to 20 V, I_{OUT} = 0 A
Transition time: 146 ms
Slew rate: 101.36 V/s

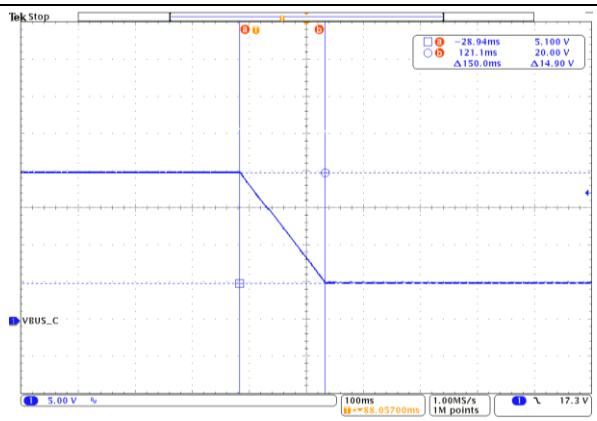


V_{OUT} = 20 V to 5 V, I_{OUT} = 0 A
Transition time: 149 ms
Slew rate: -99.33 V/s

Figure 35 Output voltage transition at no load for 115 V_{AC}, 60 Hz; (CH3: V_{BUS_C})



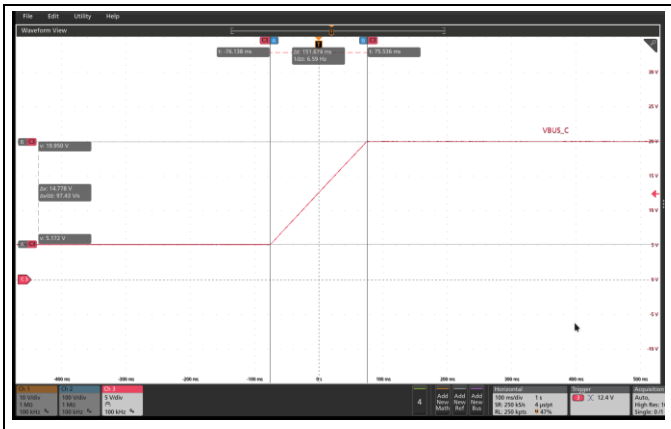
V_{OUT} = 5 V to 20 V, I_{OUT} = 0 A
Transition time: 151 ms
Slew rate: 98.67 V/s



V_{OUT} = 20 V to 5 V, I_{OUT} = 0 A
Transition time: 150 ms
Slew rate: -99.33 V/s

Figure 36 Output voltage transition at no load for 230 V_{AC}, 50 Hz; (CH3: V_{BUS_C})

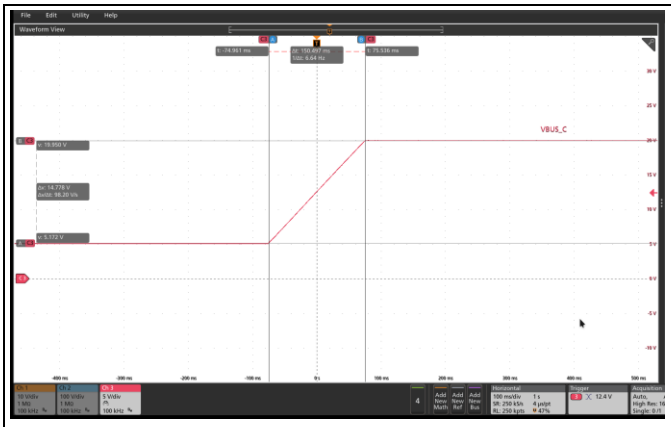
Power management test results



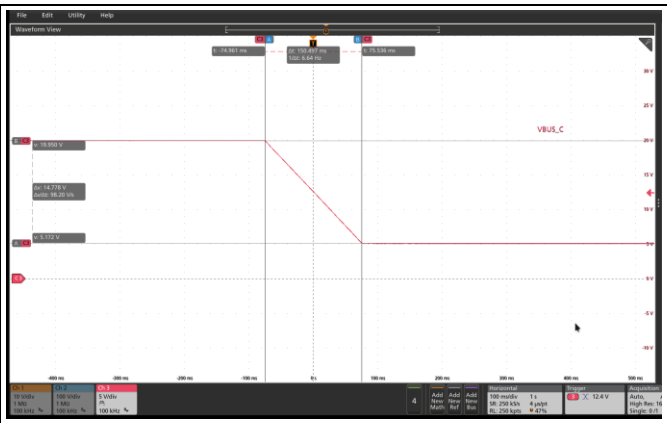
V_{OUT} = 5 V to 20 V, I_{OUT} = 3 A
Transition time: 151.6 ms
Slew rate: 97.43 V/s

V_{OUT} = 20 V to 5 V, I_{OUT} = 3 A
Transition time: 151.6 ms
Slew rate: -97.43 V/s

Figure 37 Output voltage transition at 3 A load for 115 V_{AC}, 60 Hz; (CH3: V_{BUS_C})



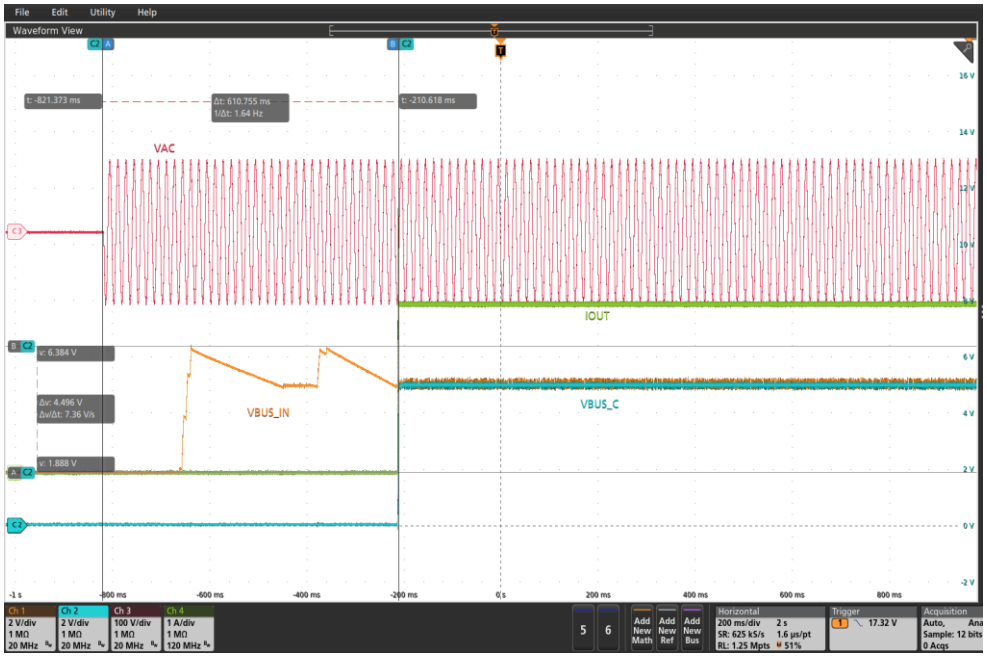
V_{OUT} = 5 V to 20 V, I_{OUT} = 3 A
Transition time: 150.49 ms
Slew rate: 98.20 V/s



V_{OUT} = 20 V to 5 V, I_{OUT} = 3 A
Transition time: 150.49 ms
Slew rate: -98.20 V/s

Figure 38 Output voltage transition at 3 A load for 230 V_{AC}, 50 Hz; (CH3: V_{BUS_C})

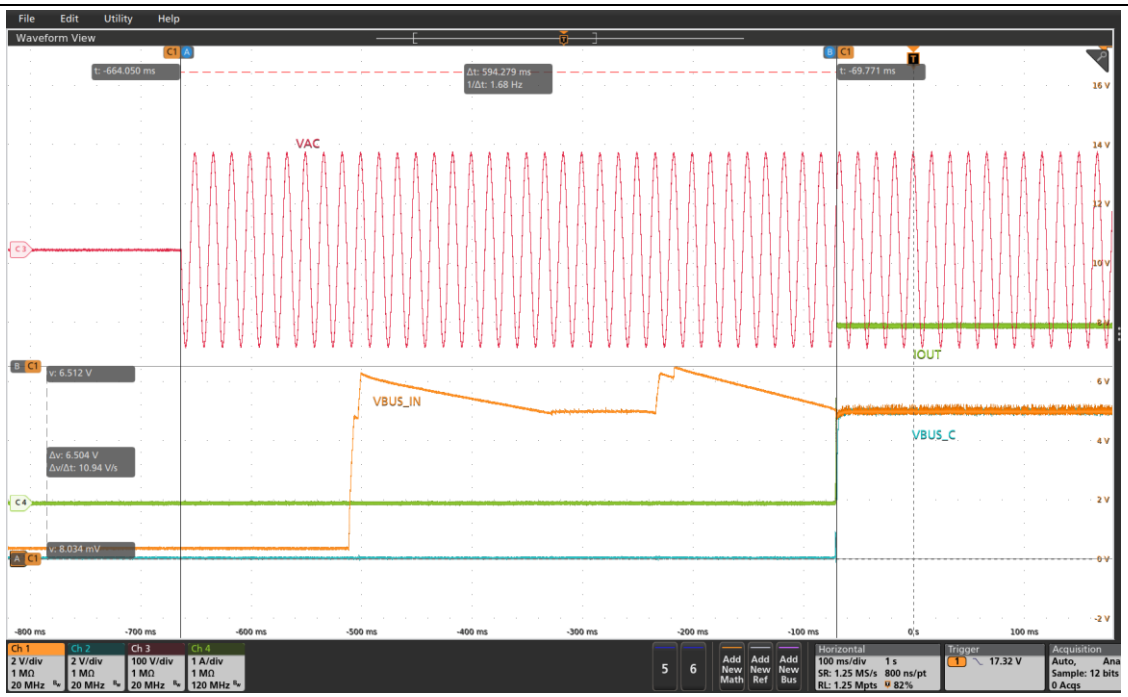
3.10 Start-up turn-on delay and startup rise time



V_{OUT} = 5 V, I_{OUT} = 3 A, start-up delay time = 610.75 ms

Start-up rise time = 2.597ms, V_{BUS_IN} overshoot = 6.384 V

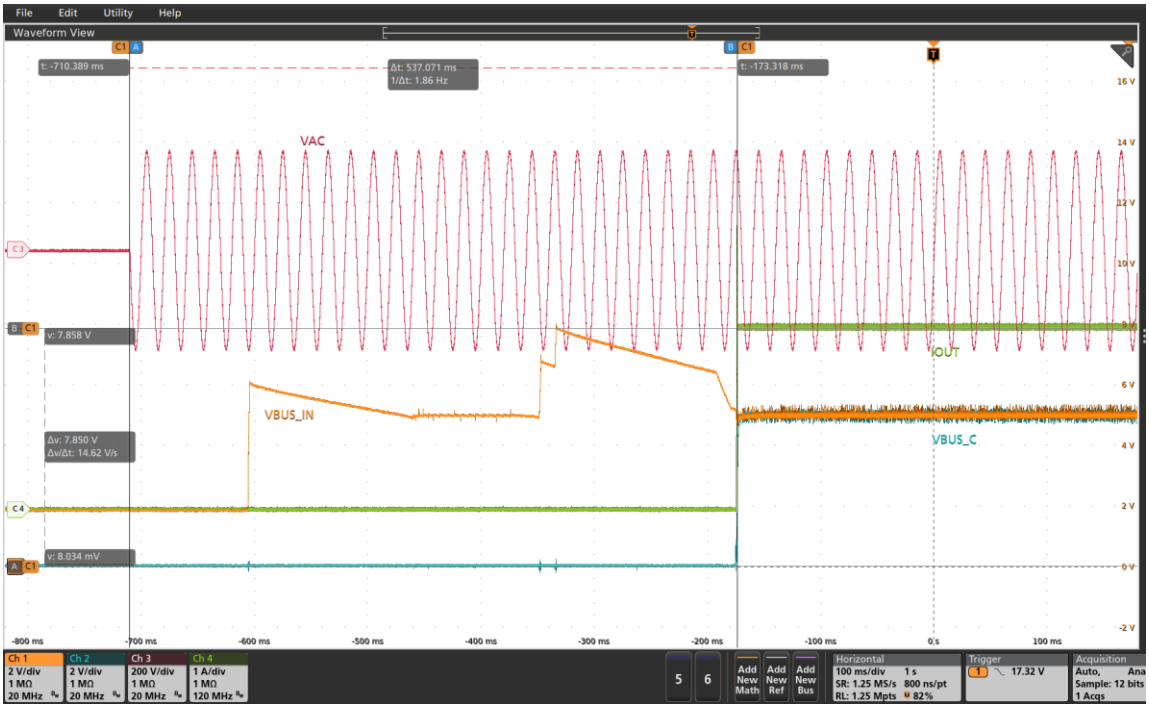
Figure 39 Start-up turn-on delay at 90 V_{AC}, 47 Hz (CH1: V_{BUS_IN}, CH2: V_{BUS_C}, CH3: V_{AC}, CH4: I_{OUT})



V_{OUT} = 5 V, I_{OUT} = 3 A, start-up delay time = 594.28 ms

Start-up rise time = 2.77 ms, V_{BUS_IN} overshoot = 6.512 V

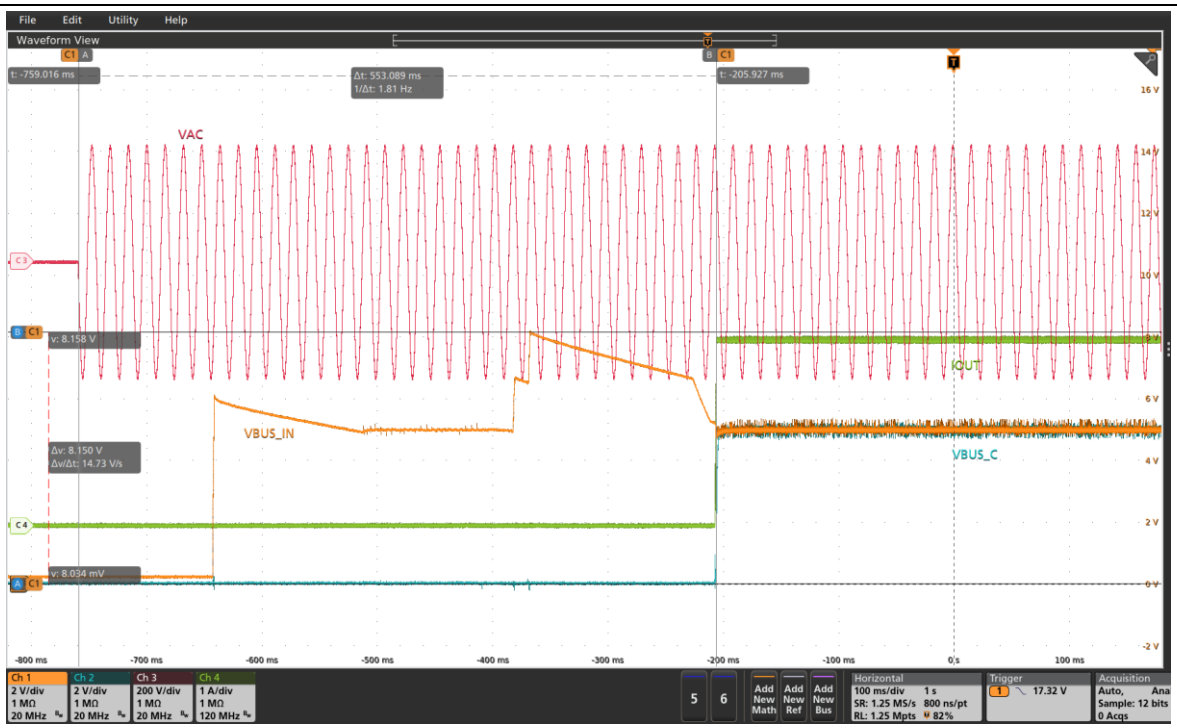
Figure 40 Start-up turn-on delay at 115 V_{AC}, 60 Hz (CH1: V_{BUS_IN}, CH2: V_{BUS_C}, CH3: V_{AC}, CH4: I_{OUT})



V_{OUT} = 5 V, I_{OUT} = 3 A, start-up delay time = 537.07 ms

Start-up rise time = 2.626 ms, V_{BUS_IN} overshoot = 7.858 V

Figure 41 Start-up turn-on delay at 230 V_{AC}, 50 Hz (CH1: V_{BUS_IN}, CH2: V_{BUS_C}, CH3: V_{AC}, CH4: I_{OUT})

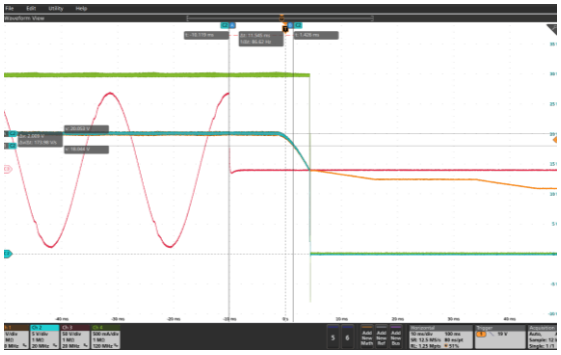


V_{OUT} = 5 V, I_{OUT} = 3 A, start-up delay time = 553.09 ms

Start-up rise time = 2.683 ms, V_{BUS_IN} overshoot = 8.158 V

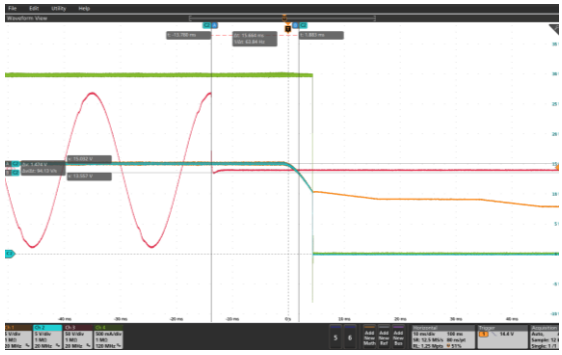
Figure 42 Start-up turn-on delay at 265 V_{AC}, 63 Hz (CH1: V_{BUS_IN}, CH2: V_{BUS_C}, CH3: V_{AC}, CH4: I_{OUT})

3.11 Hold-up time



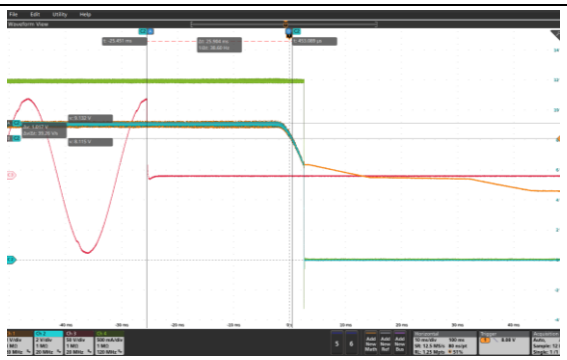
V_O = 20 V; I_O = 3.25

Hold-up time = 11.545 ms



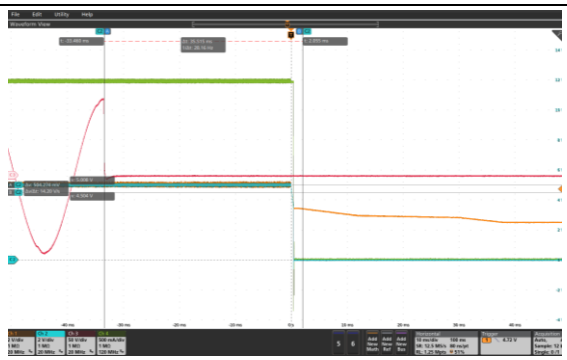
V_O = 15 V; I_O = 3.0

Hold-up time = 15.664 ms



V_O = 9 V; I_O = 3.0

Hold-up time = 25.904 ms

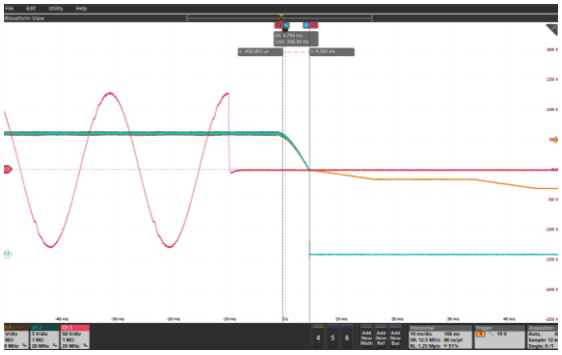


V_O = 5 V; I_O = 3.0

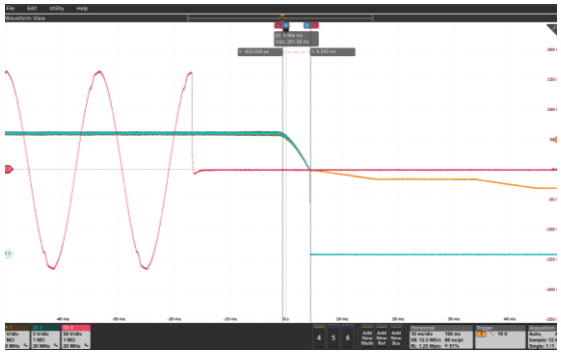
Hold-up time = 35.515 ms

Figure 43 Hold-up time at 90 V_{AC}, 47 Hz (CH1: V_{BUS_IN}, CH2: V_{BUS_C}, CH3: V_{IN_AC}, CH4: I_{OUT})

3.12 Shut-down fall time

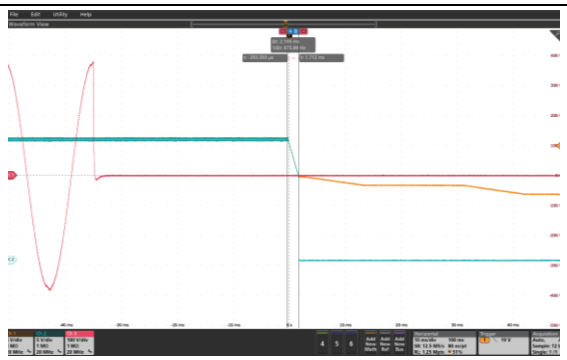


90 V_{AC}, 47 Hz, V_O = 20 V; I_O = 3.25
Shut-down fall time = 4.79 ms



115 V_{AC}, 60 Hz, V_O = 20 V; I_O = 3.25
Shut-down fall time = 4.97 ms

230 V_{AC}, 50 Hz, V_O = 20 V; I_O = 3.25
Shut-down fall time = 2.05ms

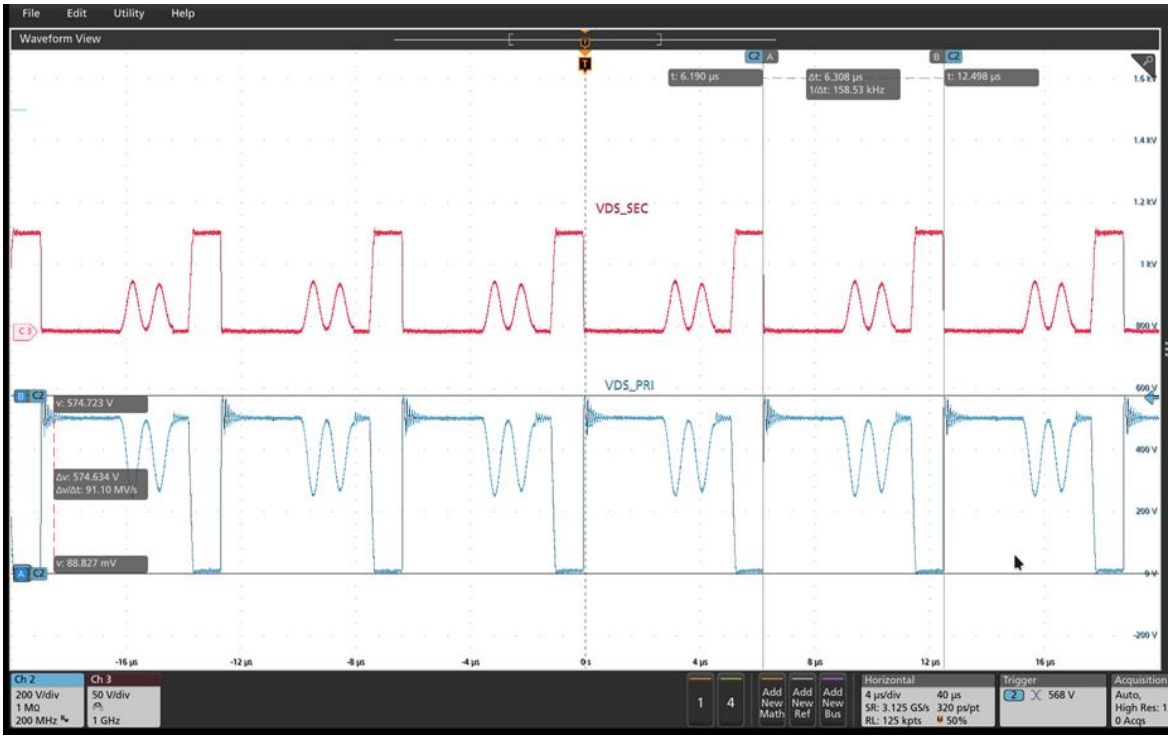


265 V_{AC}, 63 Hz, V_O = 20 V; I_O = 3.25
Shut-down fall time = 2.11 ms

Figure 44 Shut-down fall time at different line conditions for 20 V, 3.25 A (CH1: V_{BUS_IN}, CH2: V_{BUS_C}, CH3: V_{IN_AC})

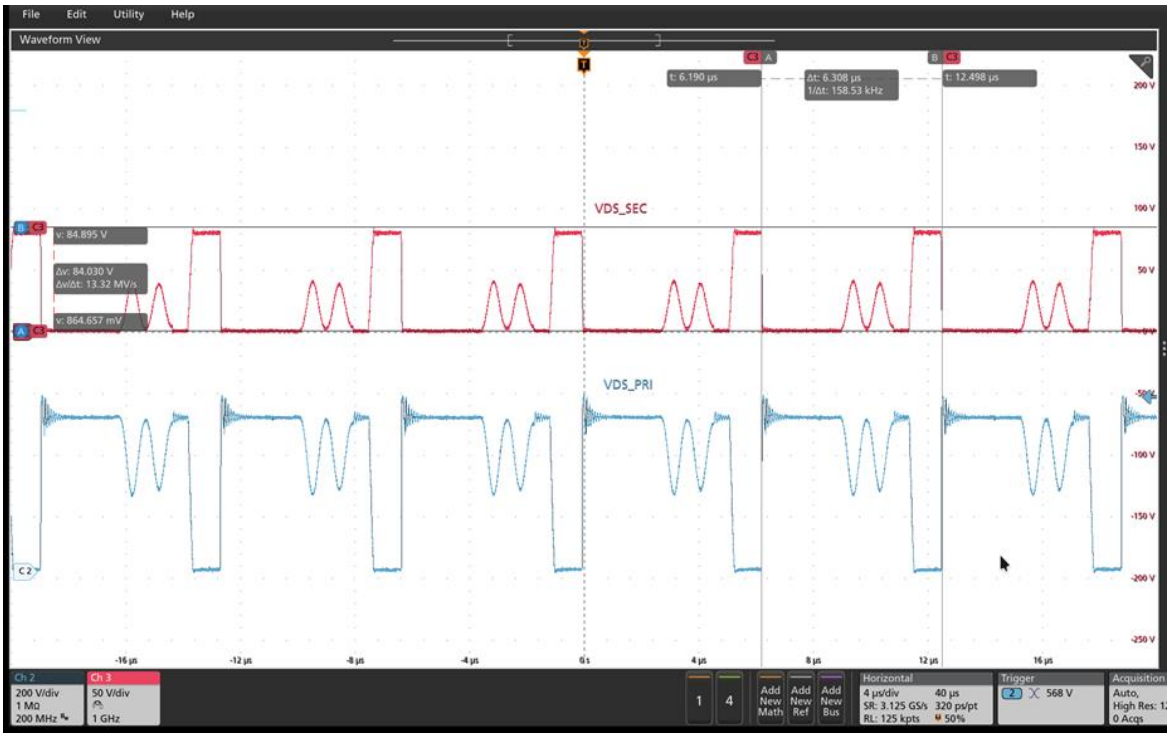
3.13 Switch voltage stress

Test Condition: V_{IN} = 265 V_{AC}, 63 Hz, V_{OUT} = 20 V, I_{OUT} = 3.25 A



V_{PRI_DRAIN} = 574 V

Figure 45 Switch voltage stress on primary FET (CH2: V_{PRI_DRAIN}, CH3: V_{SR_SEC})

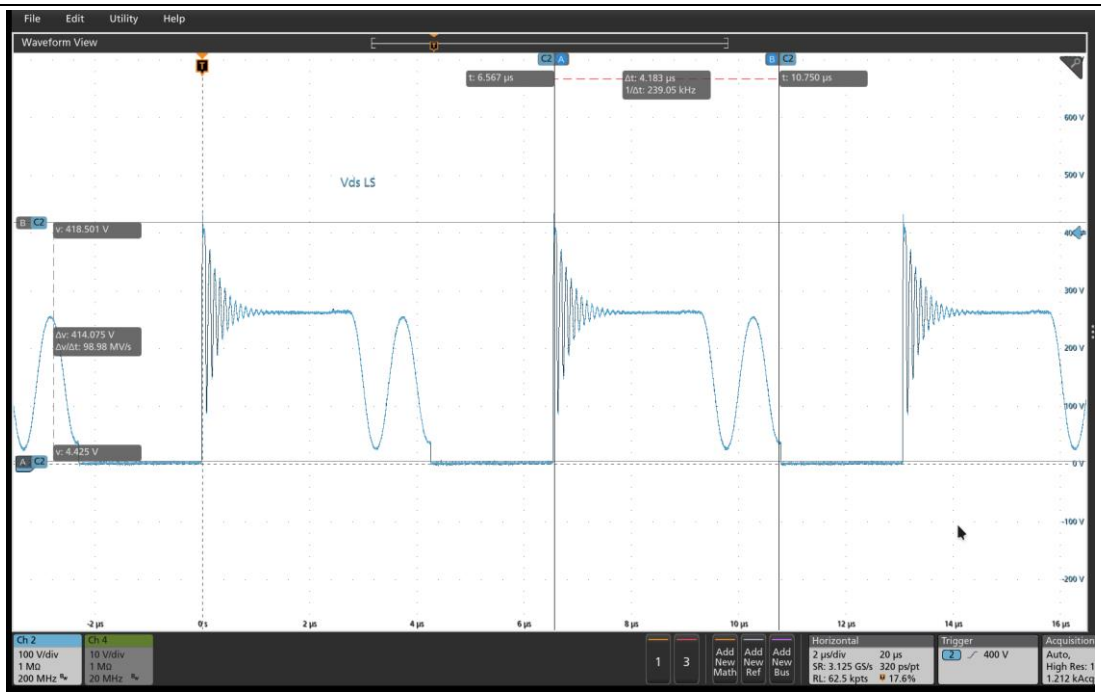


V_{SR_DRAIN} = 85 V

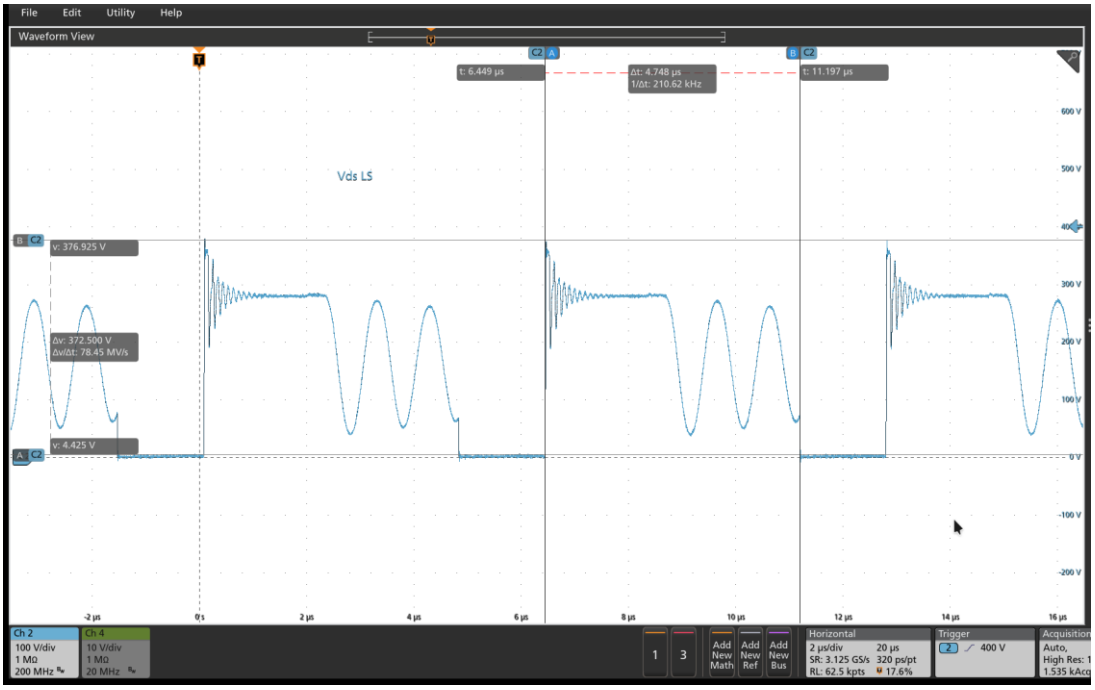
Figure 46 Switch voltage stress on secondary FET

3.14 QR and ZVS operation

The system is designed to work in QR mode at low line (<150 V_{AC}) and in QR-ZVS mode in high line (>150 V_{AC}) to achieve the maximum possible efficiency.

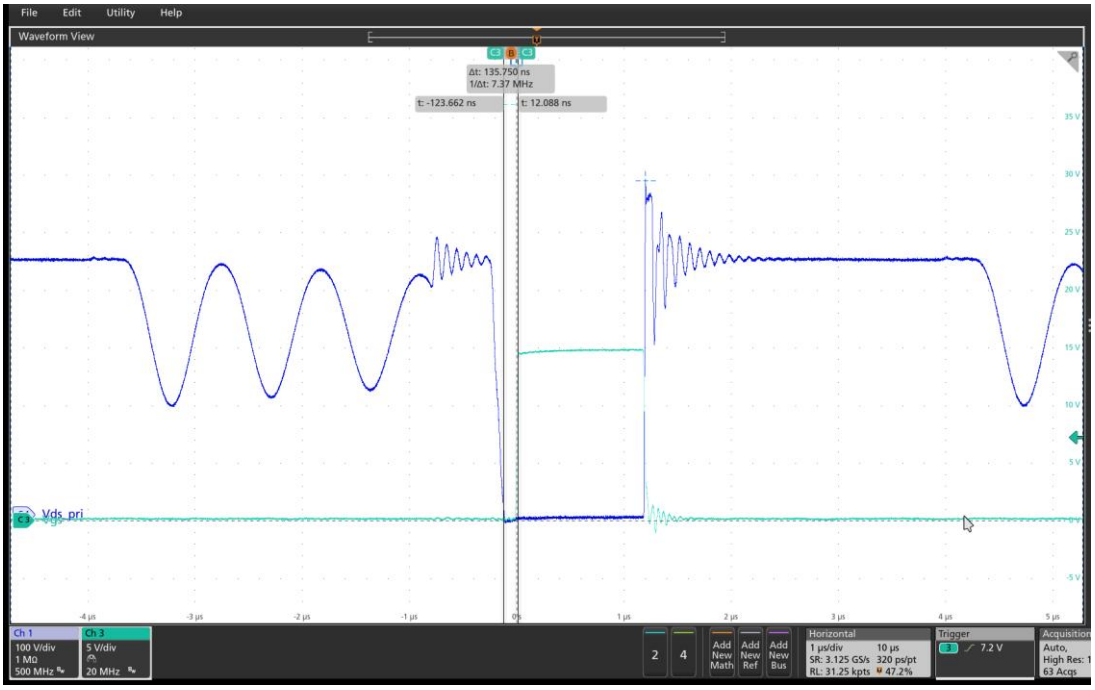


V_{AC} = 115 V, V_{OUT} = 20 V, I_{OUT} = 3.25 A, Mode = QR, Valley No = 2

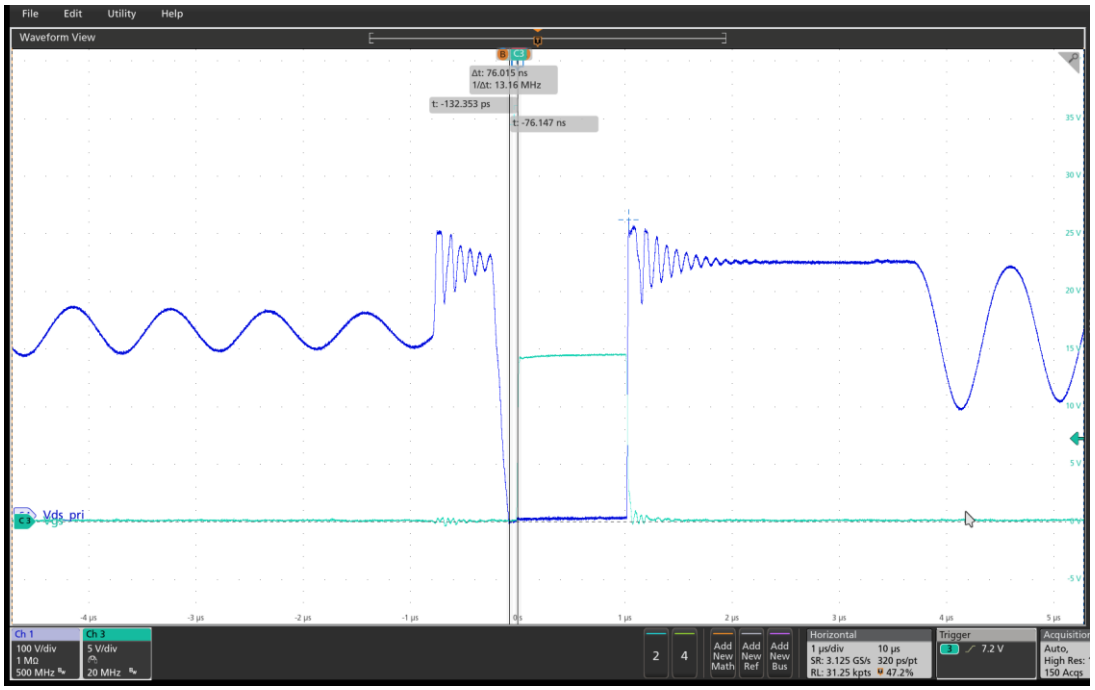


V_{AC} = 115 V, V_{OUT} = 20 V, I_{OUT} = 2.2 A, Mode = QR, Valley No = 3

Figure 47 Primary V_{DS} at 115 V_{AC}, 60 Hz

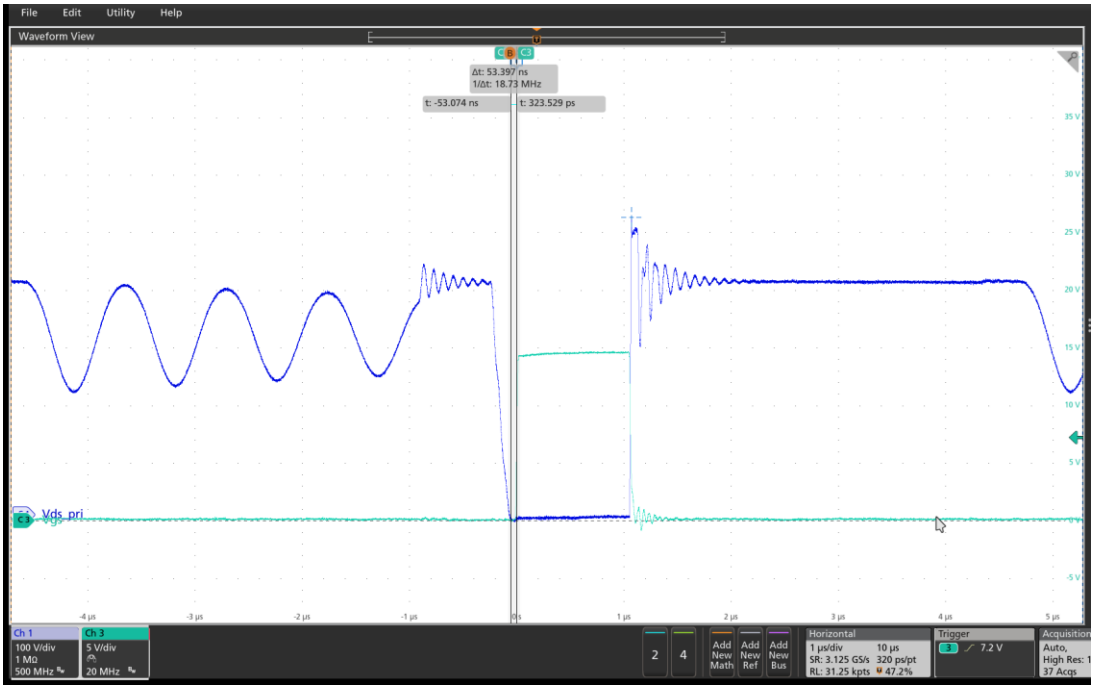


V_{AC} = 230 V, V_{OUT} = 20 V, I_{OUT} = 3.25 A, Mode = ZVS, ZVS pulse width = 550 ns, Dead time = 200 ns

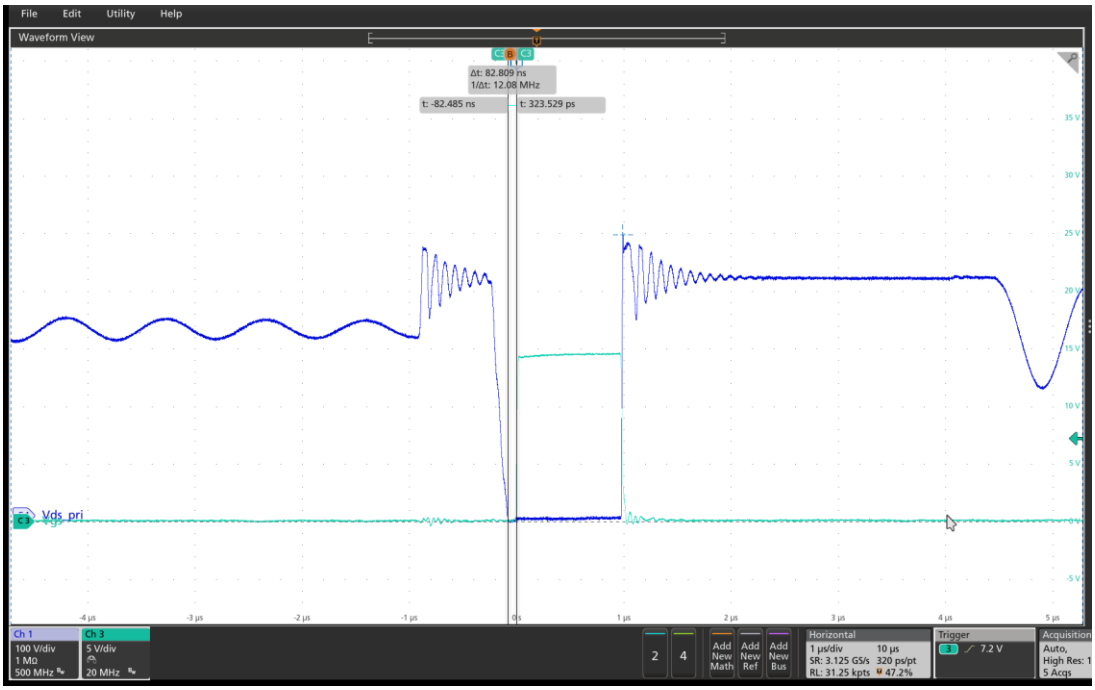


V_{AC} = 230 V, V_{OUT} = 20 V, I_{OUT} = 1 A, Mode = ZVS, ZVS pulse width = 550 ns, Dead time = 200 ns

Figure 48 Primary V_{DS} and V_{GS} for 20 V output at 230 V_{AC}, 50 Hz (CH1: V_{DS_PRI}, CH3: GDL)



V_{AC} = 230 V, V_{OUT} = 15 V, I_{OUT} = 3 A, Mode = ZVS, ZVS pulse width = 650 ns, Dead time = 200 ns

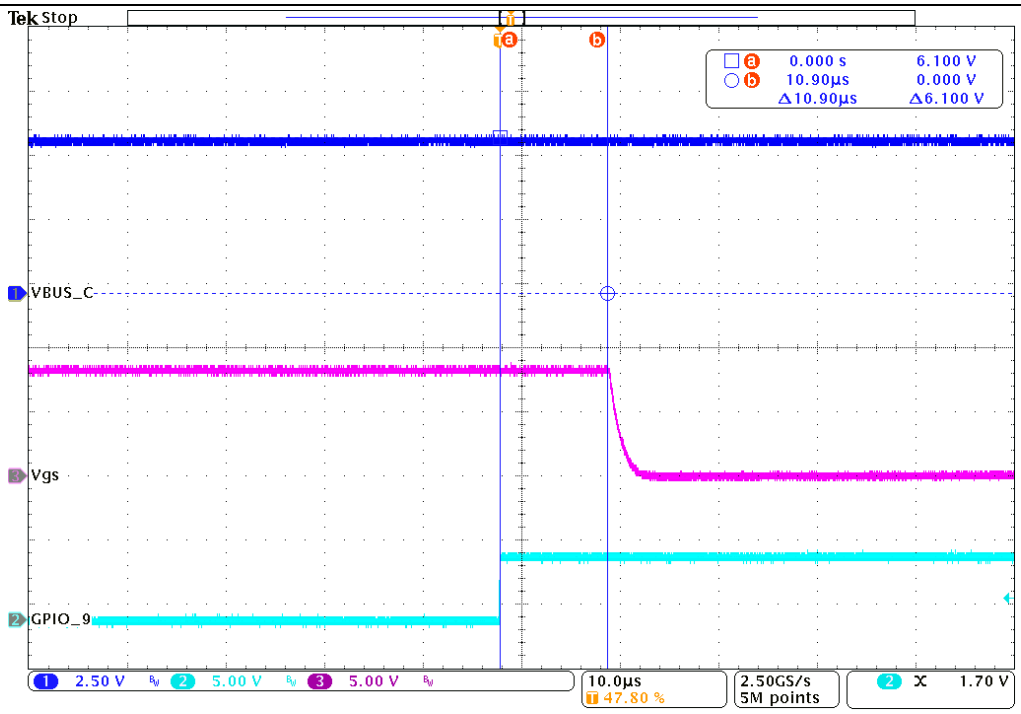


V_{AC} = 230 V, V_{OUT} = 15 V, I_{OUT} = 1 A, Mode = ZVS, ZVS pulse width = 650 ns, Dead time = 200 ns

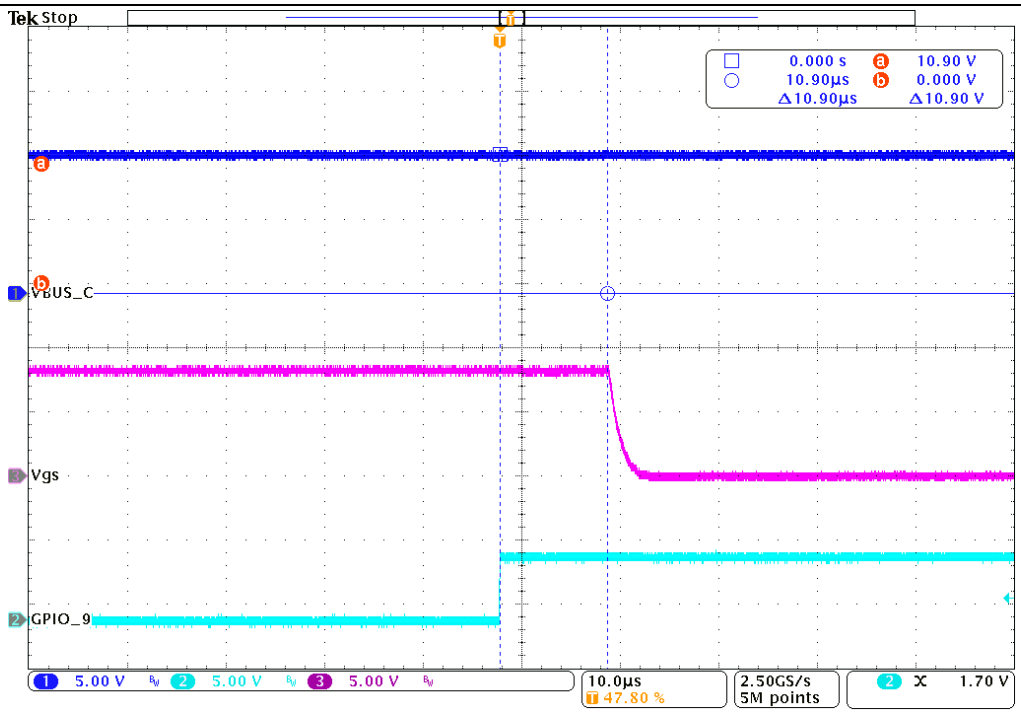
Figure 49 Primary V_{DS} and V_{GS} for 15 V output at 230 V_{AC}, 50 Hz (CH1: V_{DS_PRI}, CH3: GDL)

3.15 Overvoltage protection (OVP)

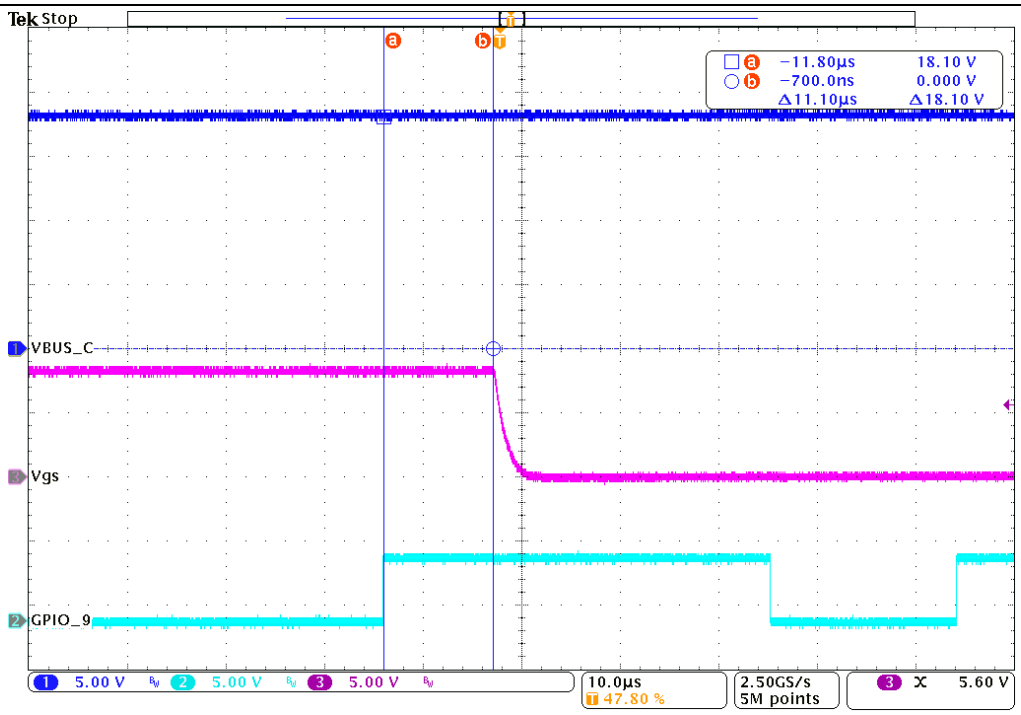
OVP tested at 115 V_{AC} 60 Hz



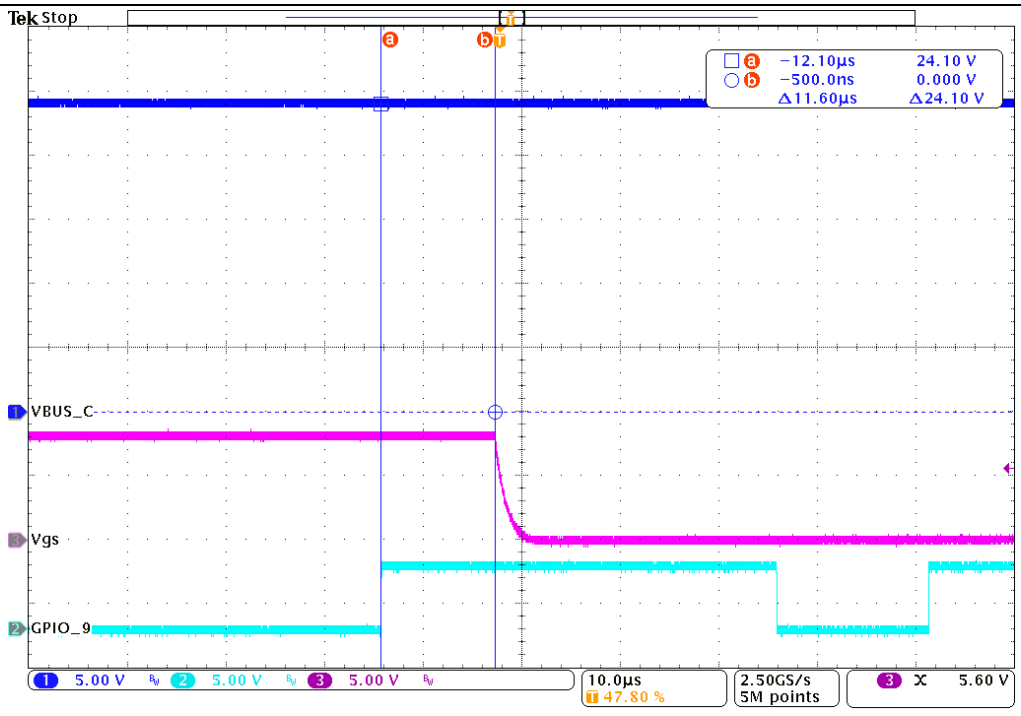
V_{OUT} = 5 V, OVP_limit = 6.1 V, OVP_response time = 10.9 µs



V_{OUT} = 9 V, OVP_limit = 10.8 V, OVP_response time = 10.9 µs



V_{OUT} = 15 V, OVP_limit = 18.1 V, OVP_response time = 11.1 µs



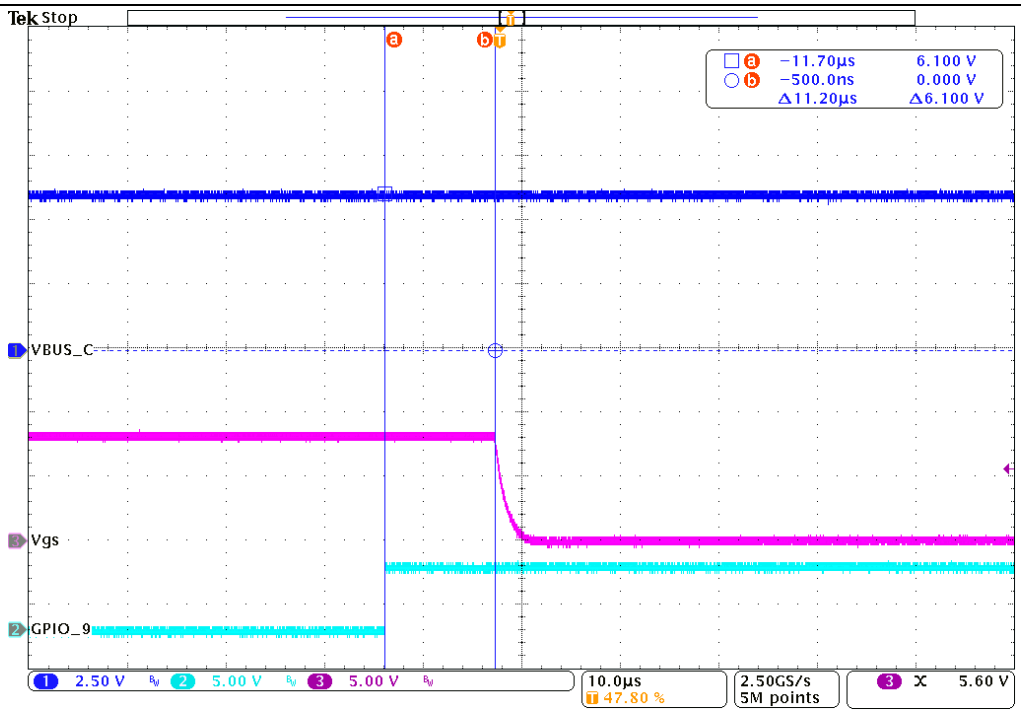
V_{OUT} = 20 V, OVP_limit = 24.1 V, OVP_response time = 11.6 µs

Figure 50 OVP at 115 V_{AC}, 60 Hz (CH3: NFET[1]; CH2: GPIO9; CH1: V_{BUS_C})

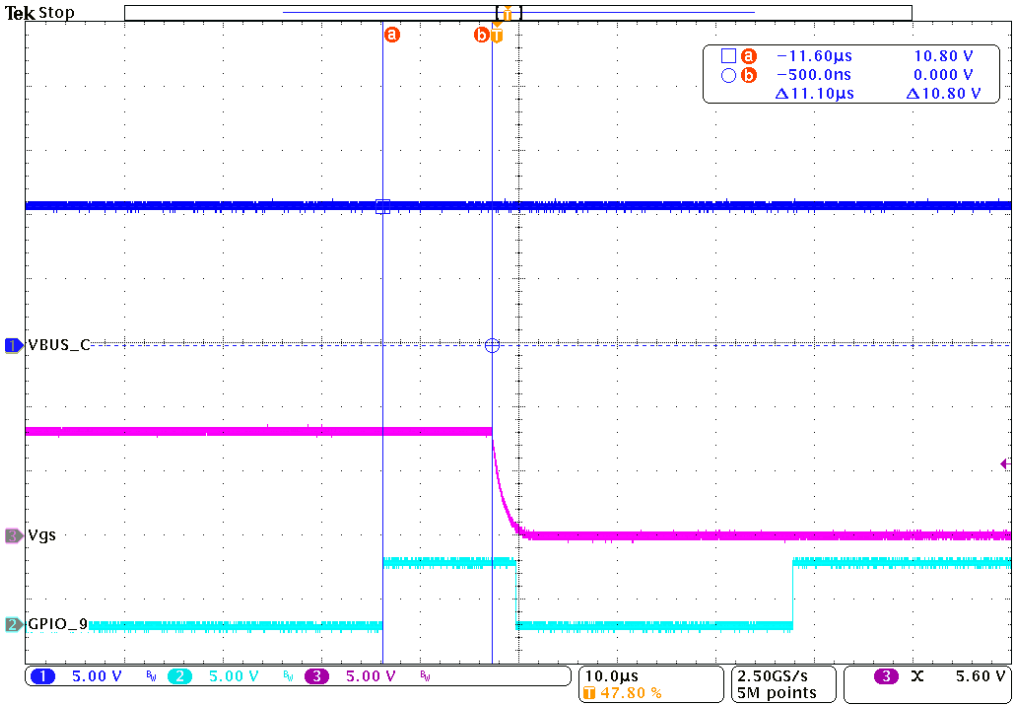
[1] NFET - Provider FET(Q2) gate to source waveform.

Power management test results

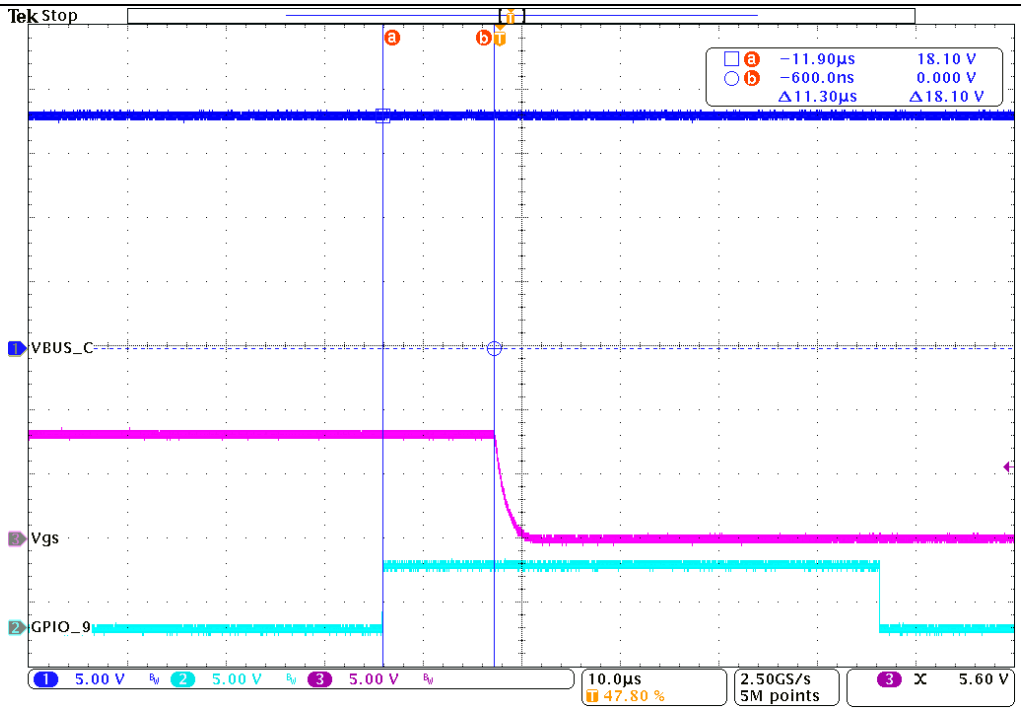
OVP tested at 230 V_{AC} 50 Hz



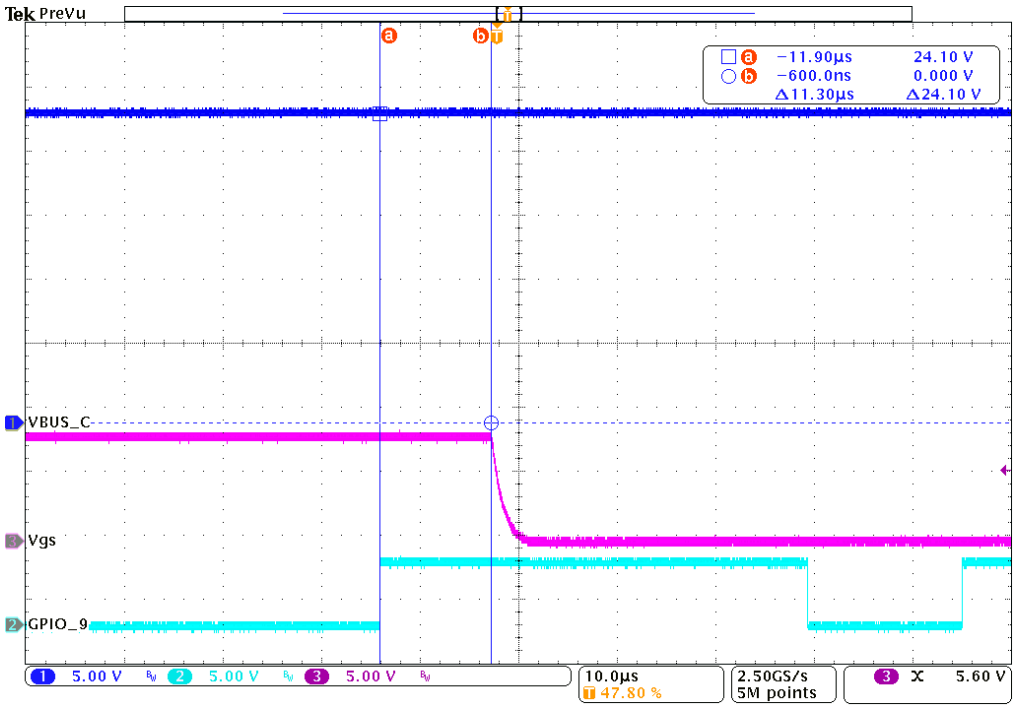
V_{OUT} = 5 V, OVP_limit = 6.1 V, OVP_response time = 11.2 µs



V_{OUT} = 9 V, OVP_limit = 10.8 V, OVP_response time = 11.1 µs



V_{OUT} = 15 V, OVP_limit = 18.1 V, OVP_response time = 11.2 µs



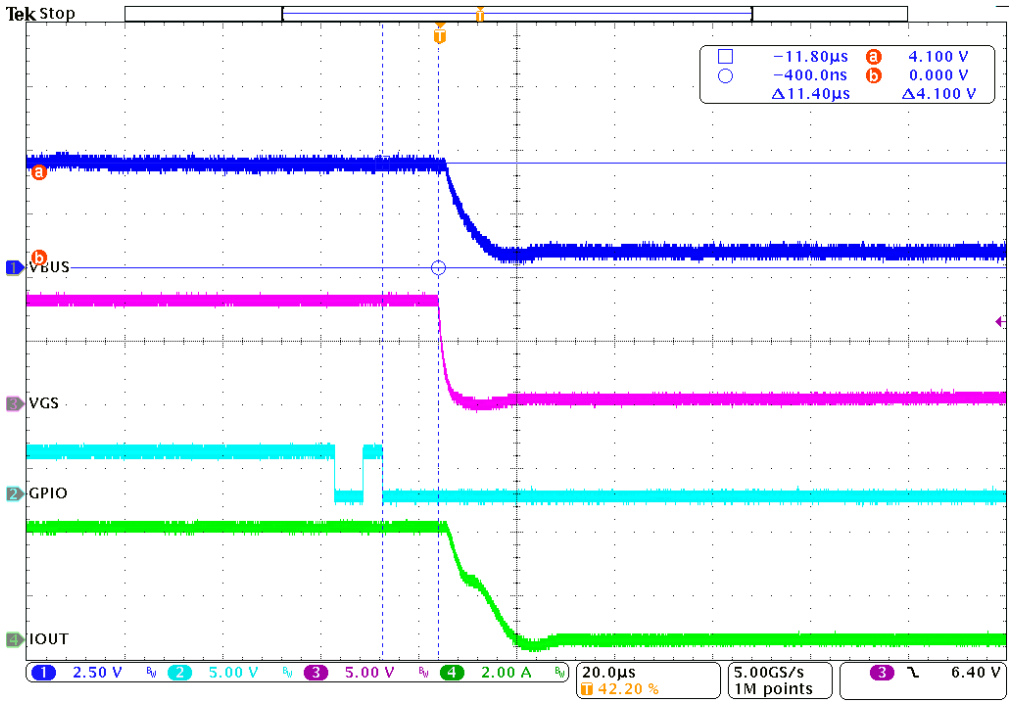
V_{OUT} = 20 V, OVP_limit = 24.1 V, OVP_response time = 11.3 µs

Figure 51 OVP at 230 V_{AC}, 50 Hz (CH3: NFET[1]; CH2: GPIO9; CH1: V_{BUS_C})

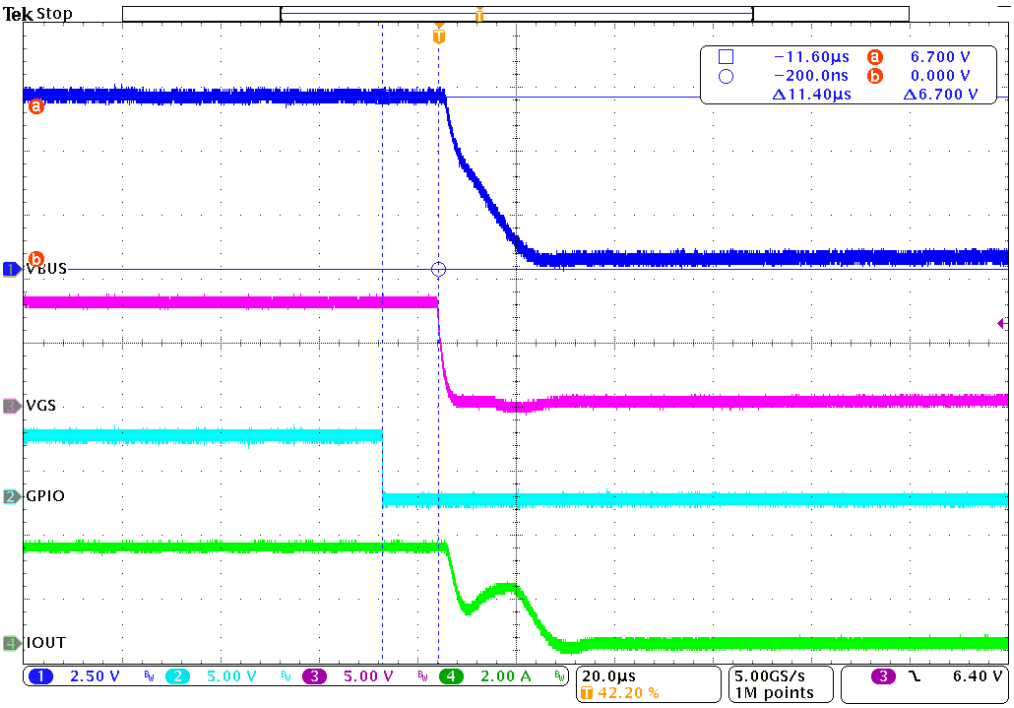
[1] NFET - Provider FET(Q2) gate to source waveform.

3.16 Undervoltage protection (UVP)

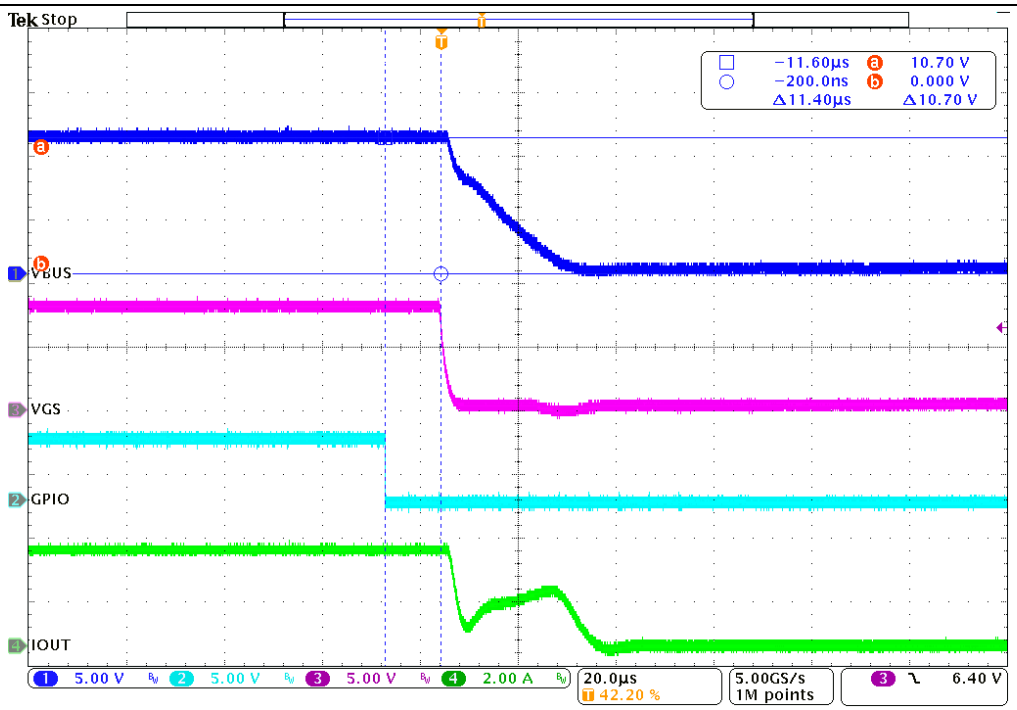
UVP tested at 115 V_{AC} 60 Hz



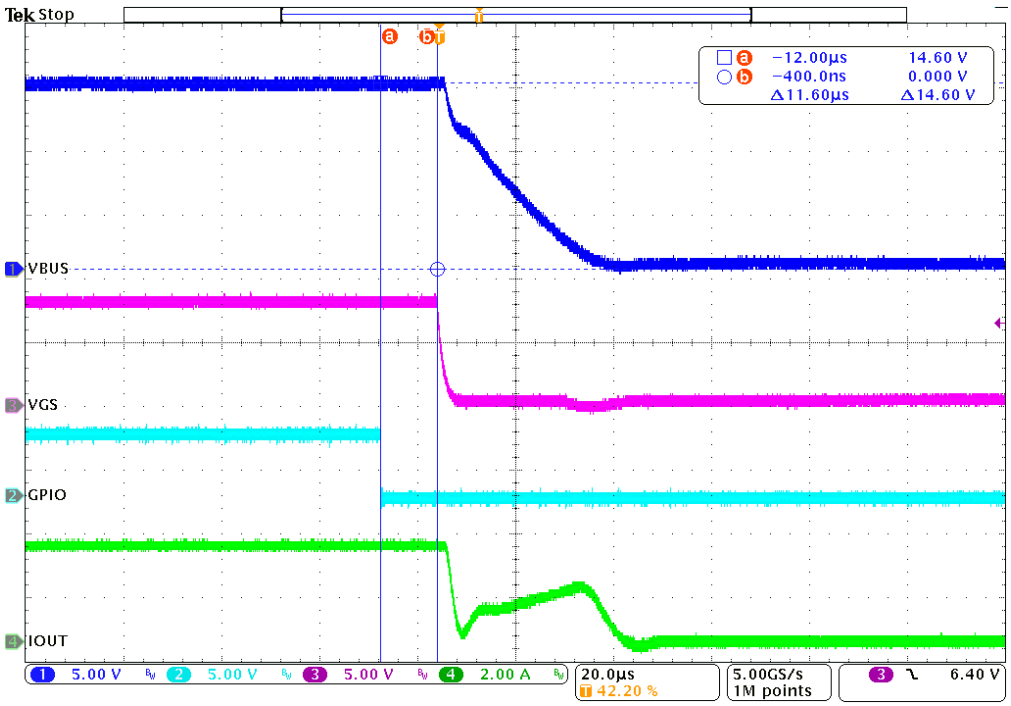
V_{OUT} = 5 V, UVP_limit = 4.1 V, UVP_response time = 11.4 µs



V_{OUT} = 9 V, UVP_limit = 6.7 V, UVP_response time = 11.4 µs



V_{OUT} = 15 V, UVP_limit = 10.7 V, UVP_response time = 11.4 µs



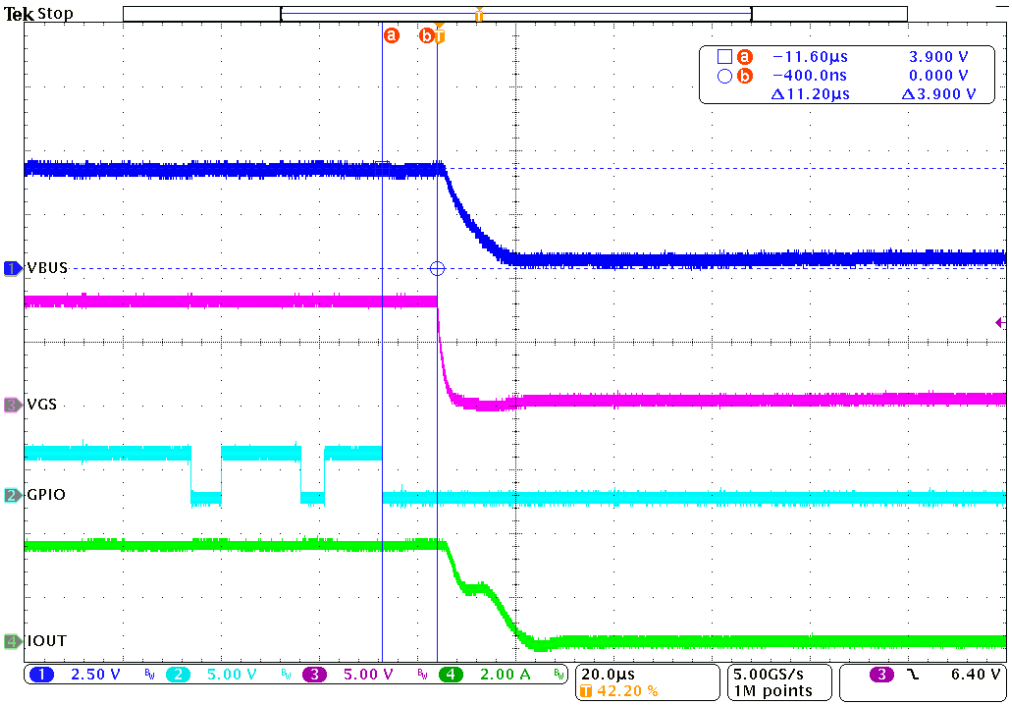
V_{OUT} = 20 V, UVP_limit = 14.6 V, UVP_response time = 11.6 µs

Figure 52 UVP at 115 V_{AC}, 60 Hz (CH4: I_{OUT}; CH2: GPIO9; CH1: V_{BUS_C}; CH3: NFET[1])

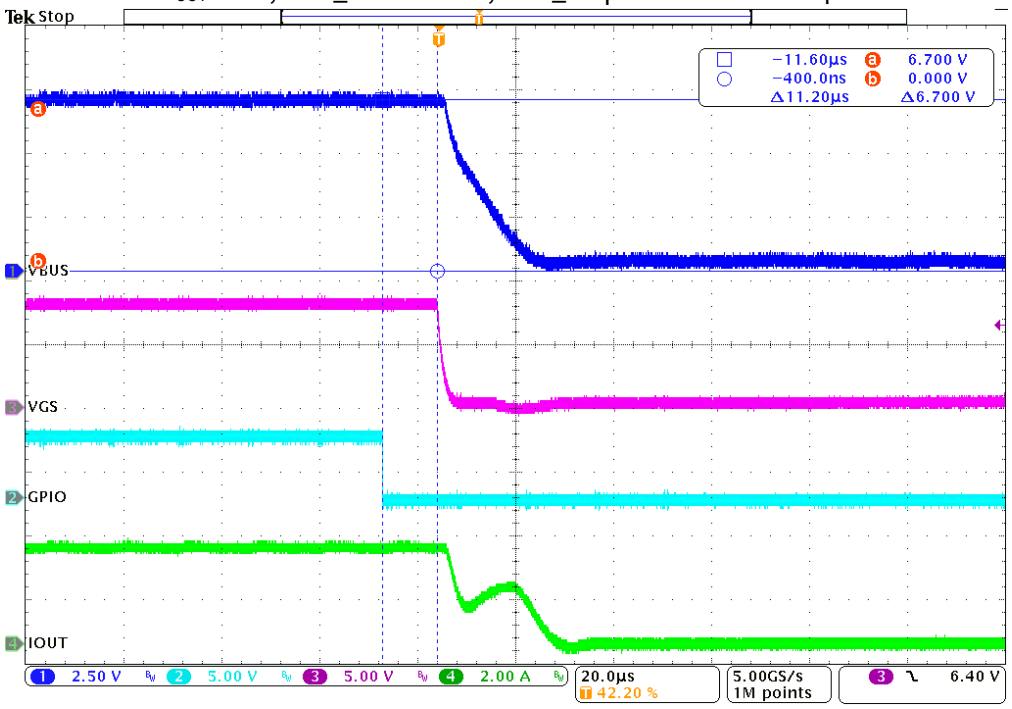
[1] NFET - Provider FET(Q1) gate to source waveform.

Power management test results

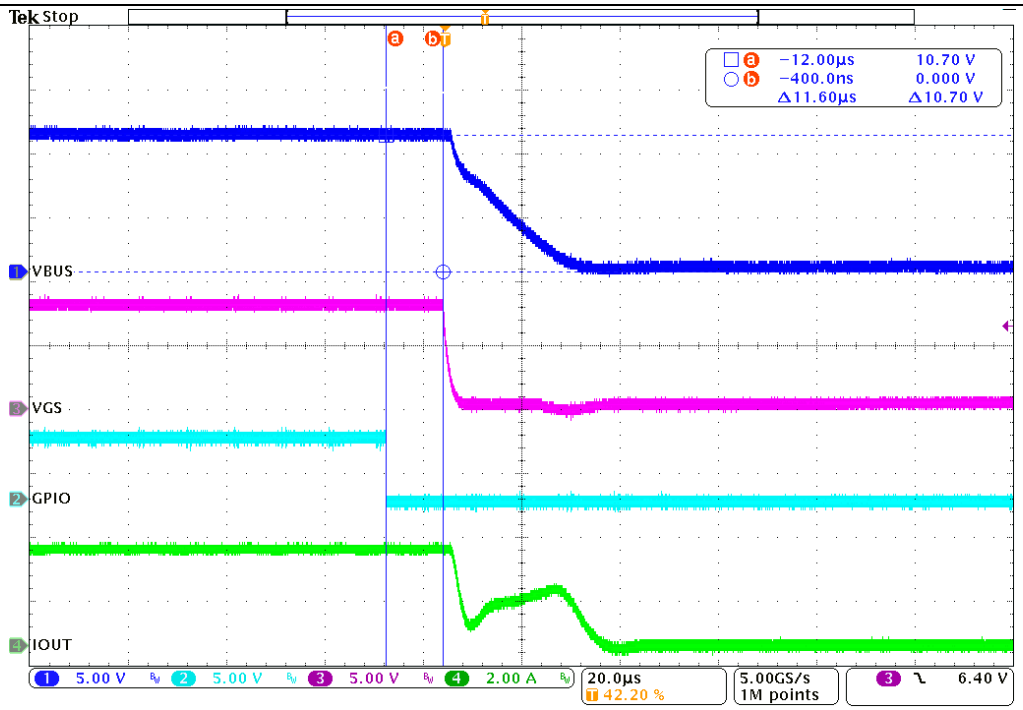
UVP tested at 230 V_{AC} 50 Hz



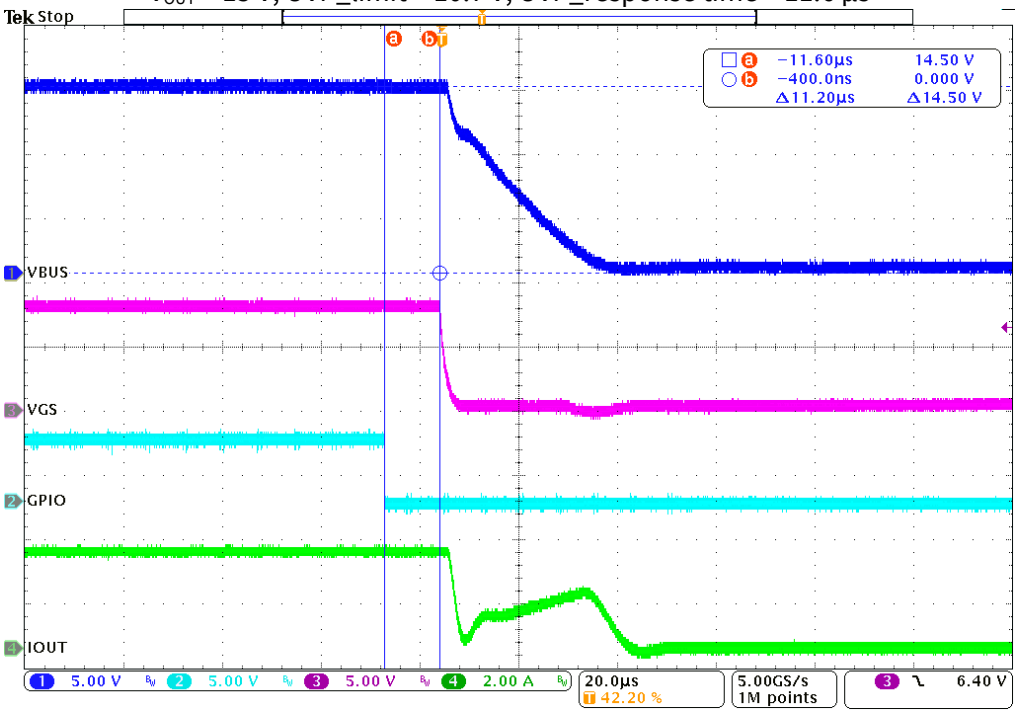
V_{OUT} = 5 V, UVP_limit = 3.9 V, UVP_response time = 11.2 µs



V_{OUT} = 9 V, UVP_limit = 6.7 V, UVP_response time = 11.2 µs



V_{OUT} = 15 V, UVP_limit = 10.7 V, UVP_response time = 11.6 µs



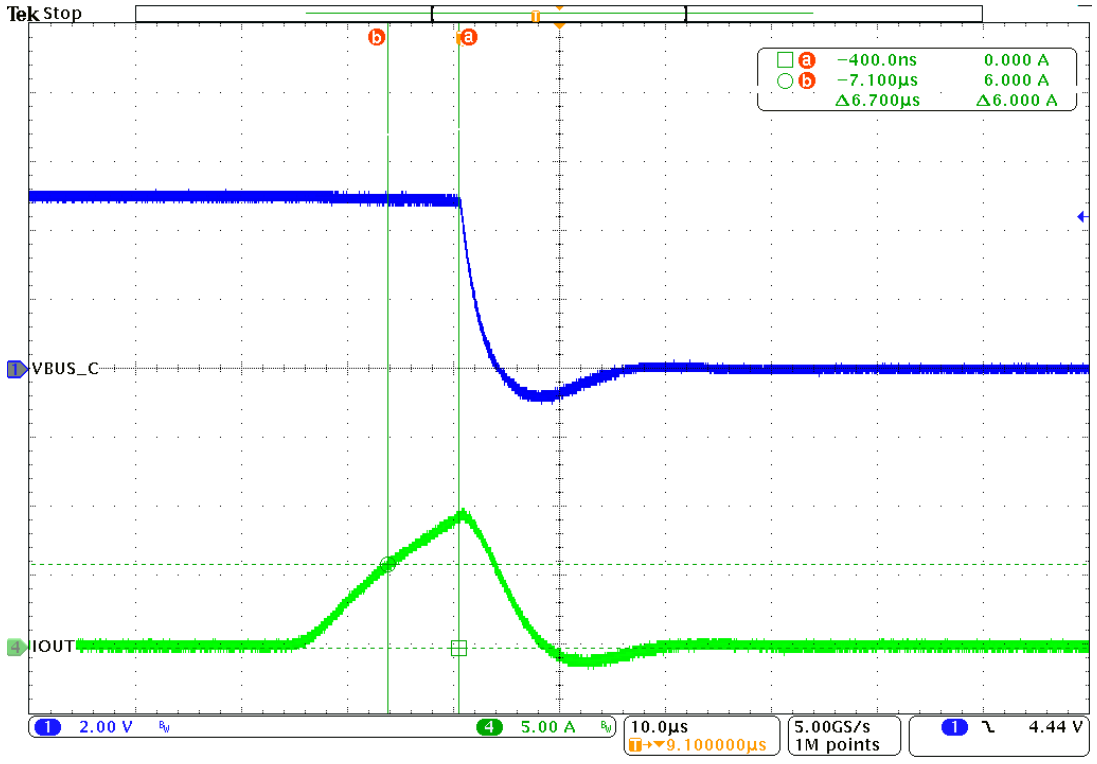
V_{OUT} = 20 V, UVP_limit = 14.5 V, UVP_response time = 11.2 µs

Figure 53 UVP at 230 V_{AC}, 50 Hz (CH4: I_{OUT}; CH2: GPIO9; CH1: V_{BUS_C}; CH3: NFET[1])

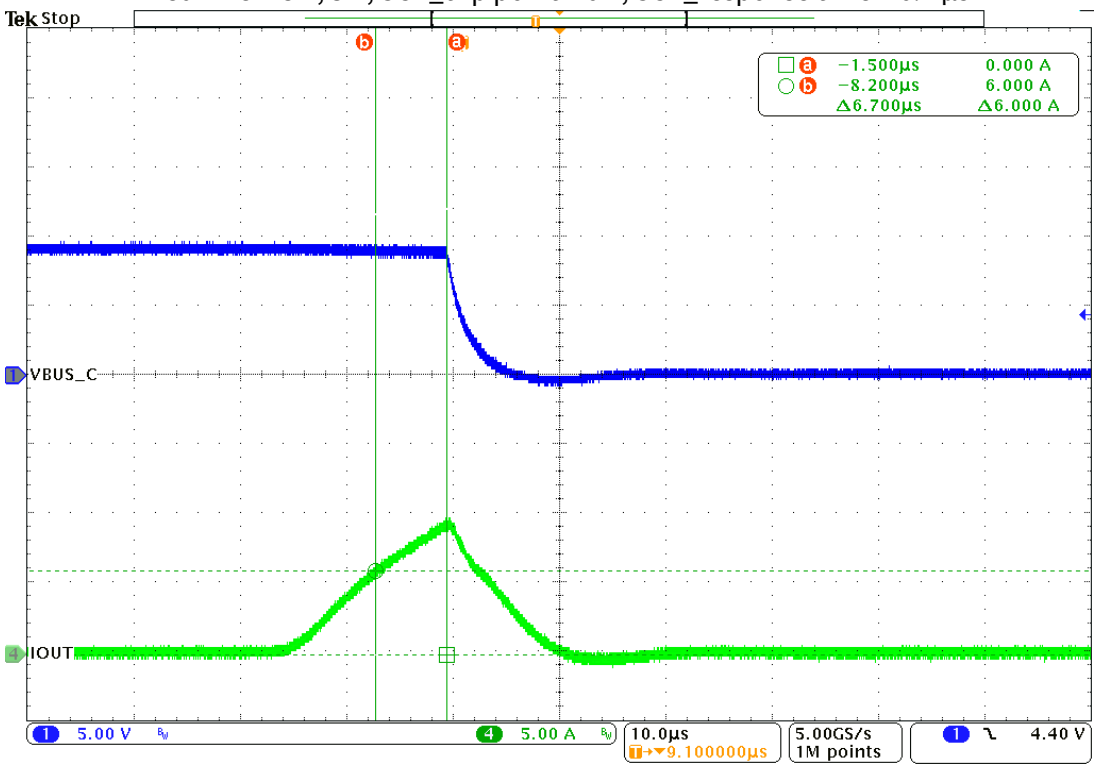
[1] NFET - Provider FET(Q1) Gate to source waveform.

3.17 Short-circuit protection (SCP)

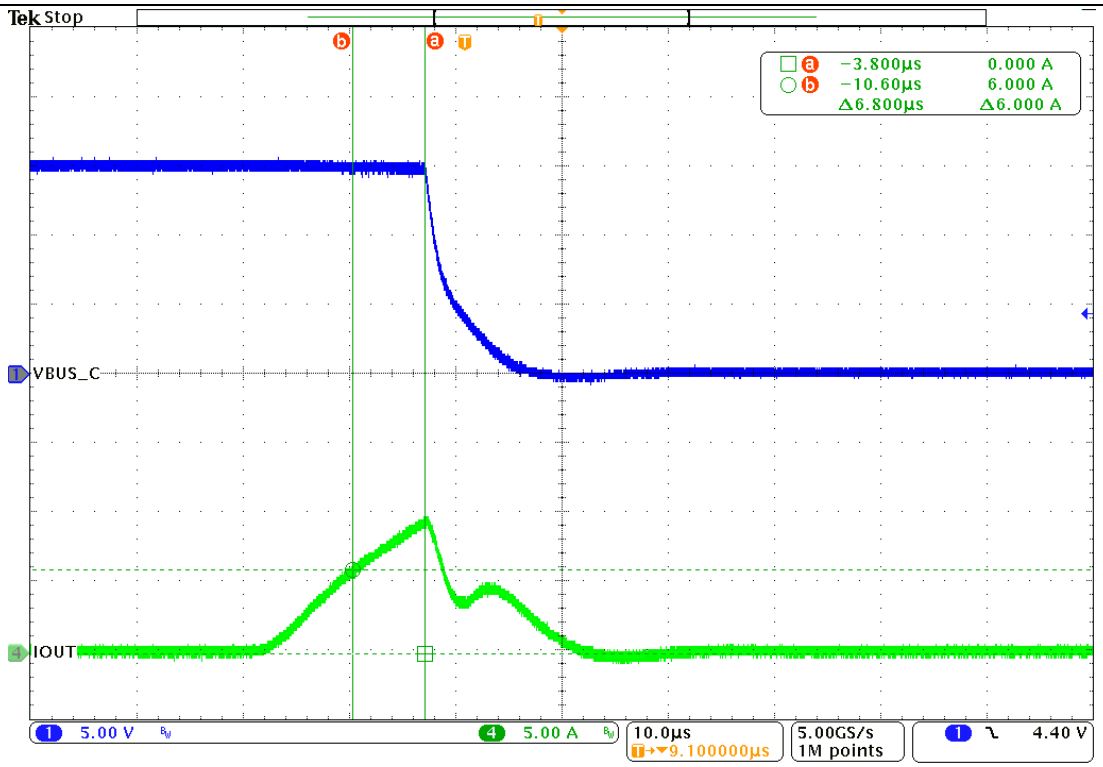
SCP tested at 115 V_{AC} 60 Hz



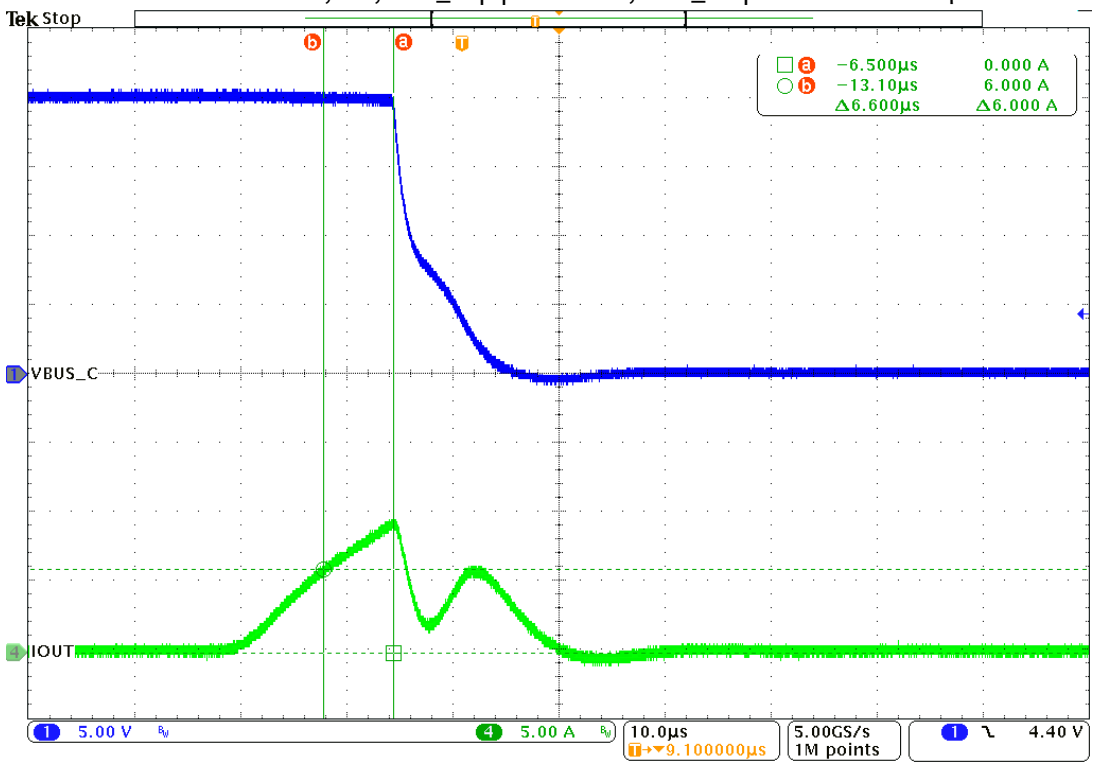
Fixed PDO = 5 V, 3 A; SCP_trip point = 6 A; SCP_response time = 6.7 µs



Fixed PDO = 9 V, 3 A; SCP_trip point = 6 A; SCP_response time = 6.7 µs



Fixed PDO = 15 V, 3 A; SCP_trip point = 6 A; SCP_response time = 6.8 µs

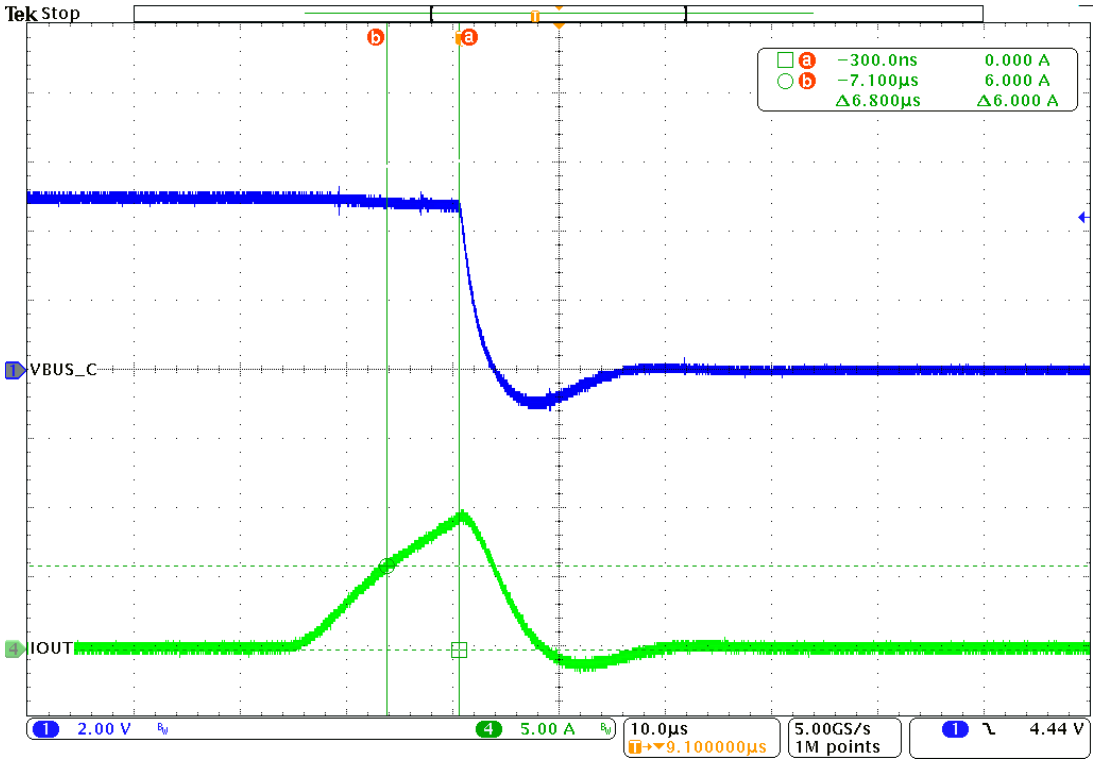


Fixed PDO = 20 V, 3.25 A; SCP_trip point = 6 A; SCP_response time = 6.6 µs

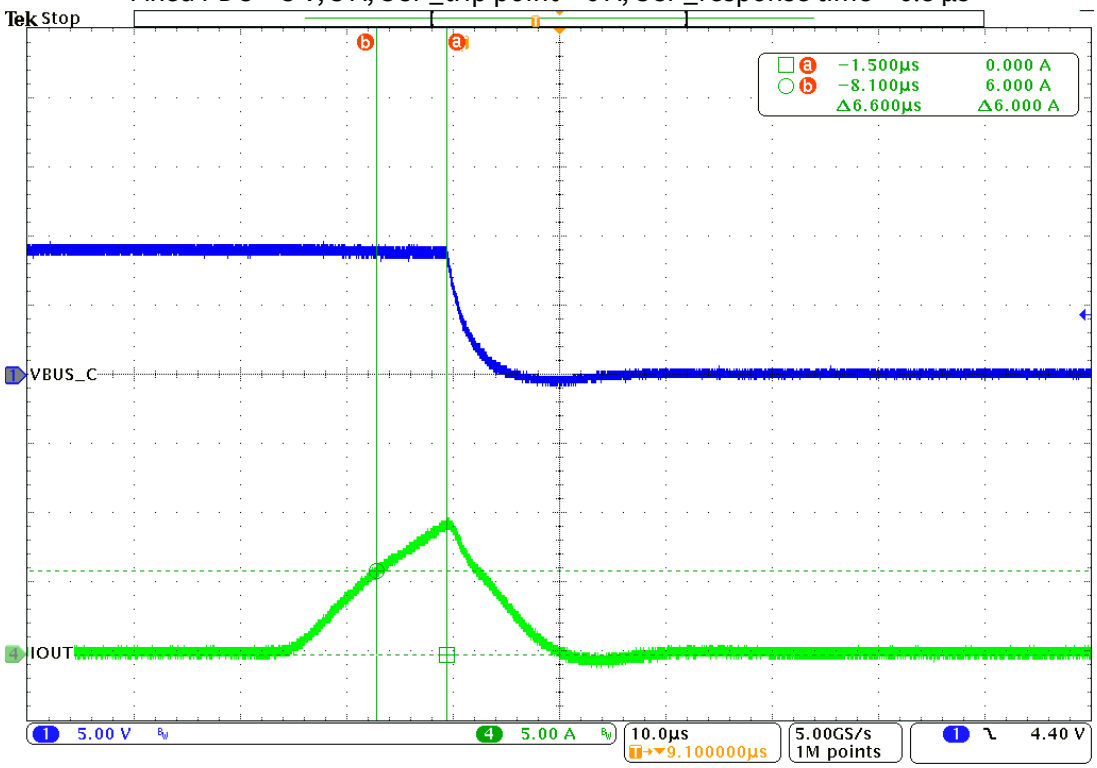
Figure 54 SCP at 115 V_{AC}, 60 Hz (CH2: V_{BUS_C}; CH4: I_{OUT})

Power management test results

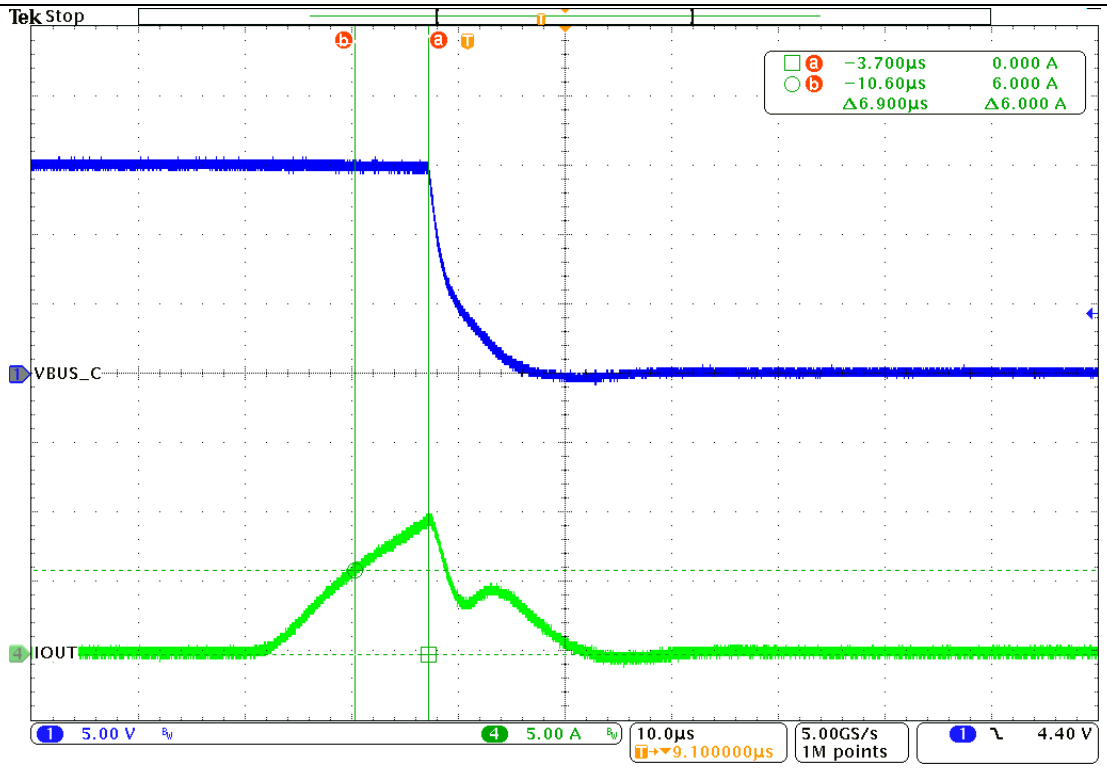
SCP tested at 230 V_{AC} 50 Hz



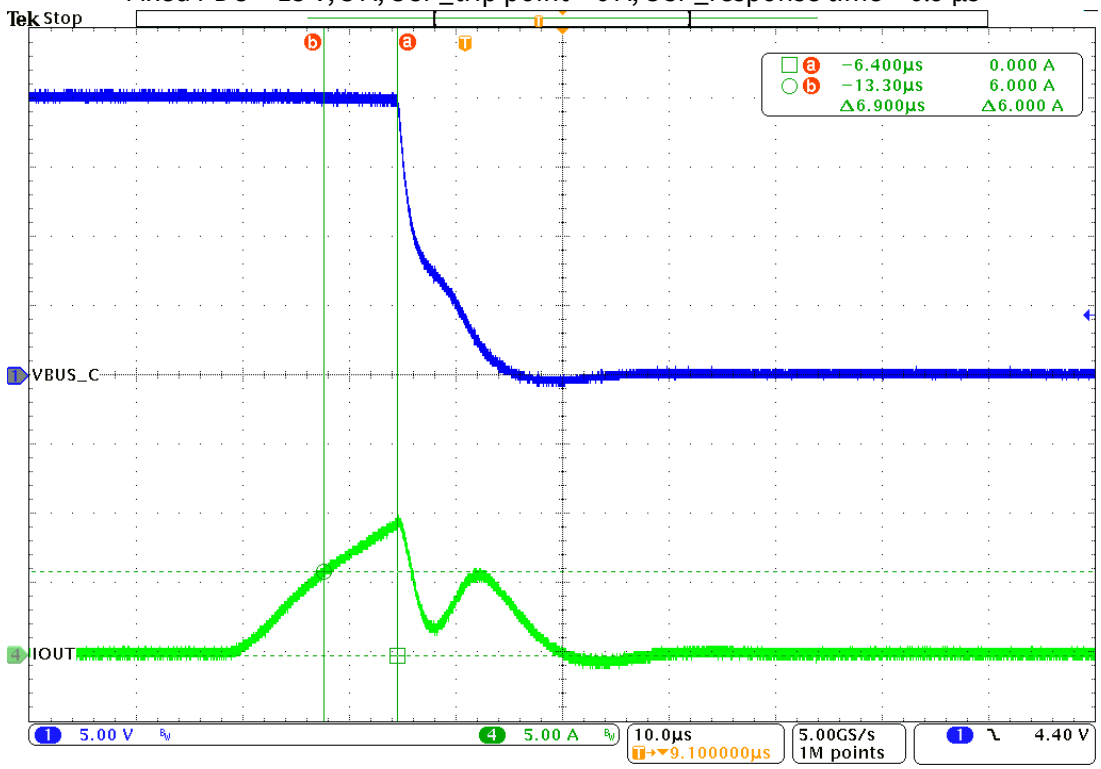
Fixed PDO = 5 V, 3 A; SCP_trip point = 6 A; SCP_response time = 6.8 µs



Fixed PDO = 9 V, 3 A; SCP_trip point = 6 A; SCP_response time = 6.6 µs



Fixed PDO = 15 V, 3 A; SCP_trip point = 6 A; SCP_response time = 6.9 µs

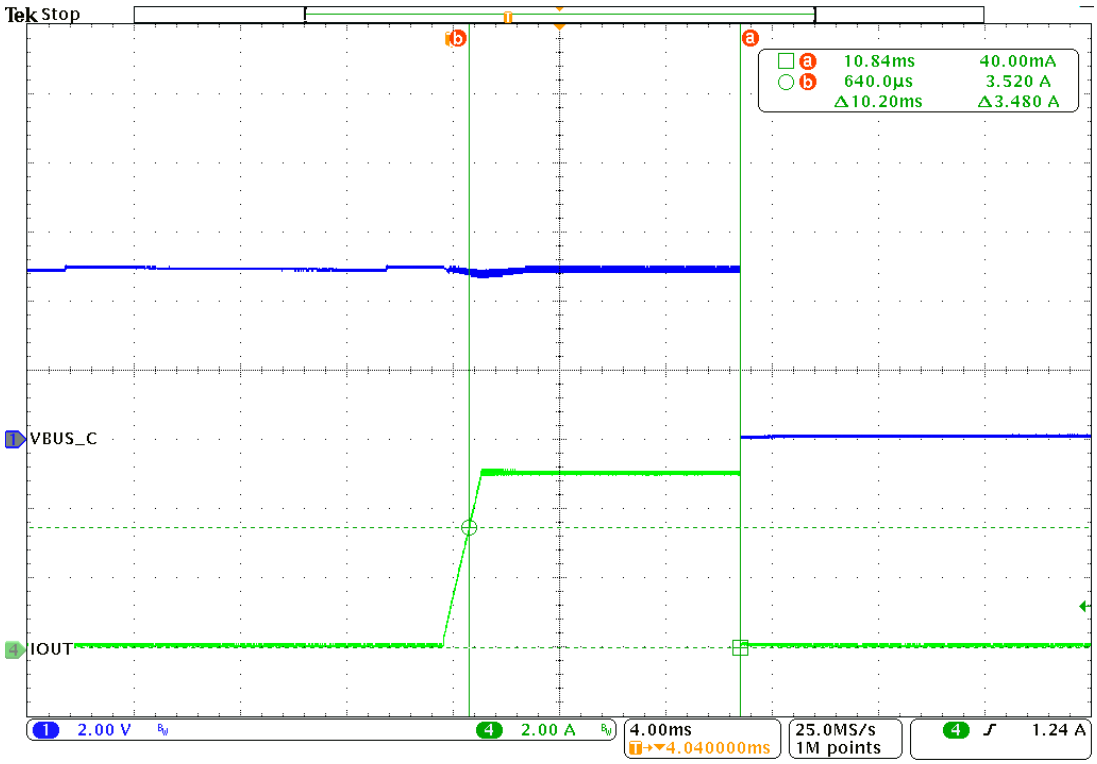


Fixed PDO = 20 V, 3.25 A; SCP_trip point = 6 A; SCP_response time = 6.9 µs

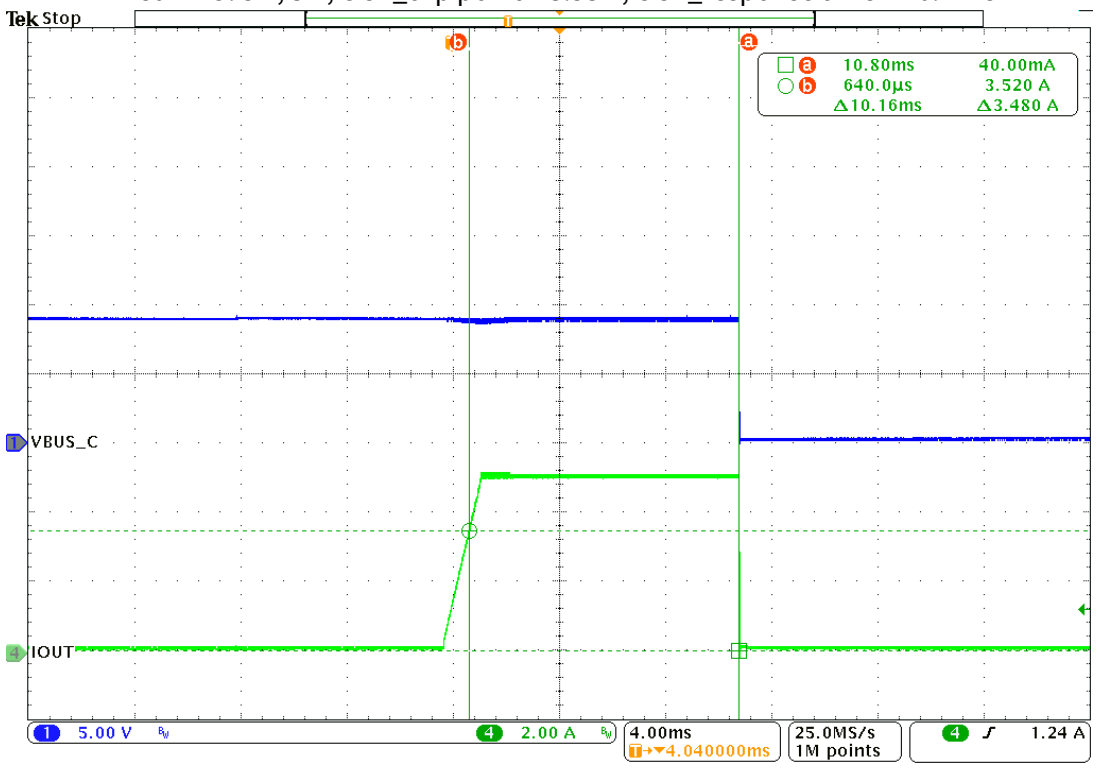
Figure 55 SCP at 230 V_{AC}, 50 Hz (CH2: V_{BUS_C}; CH4: I_{OUT})

3.18 Overcurrent protection (OCP)

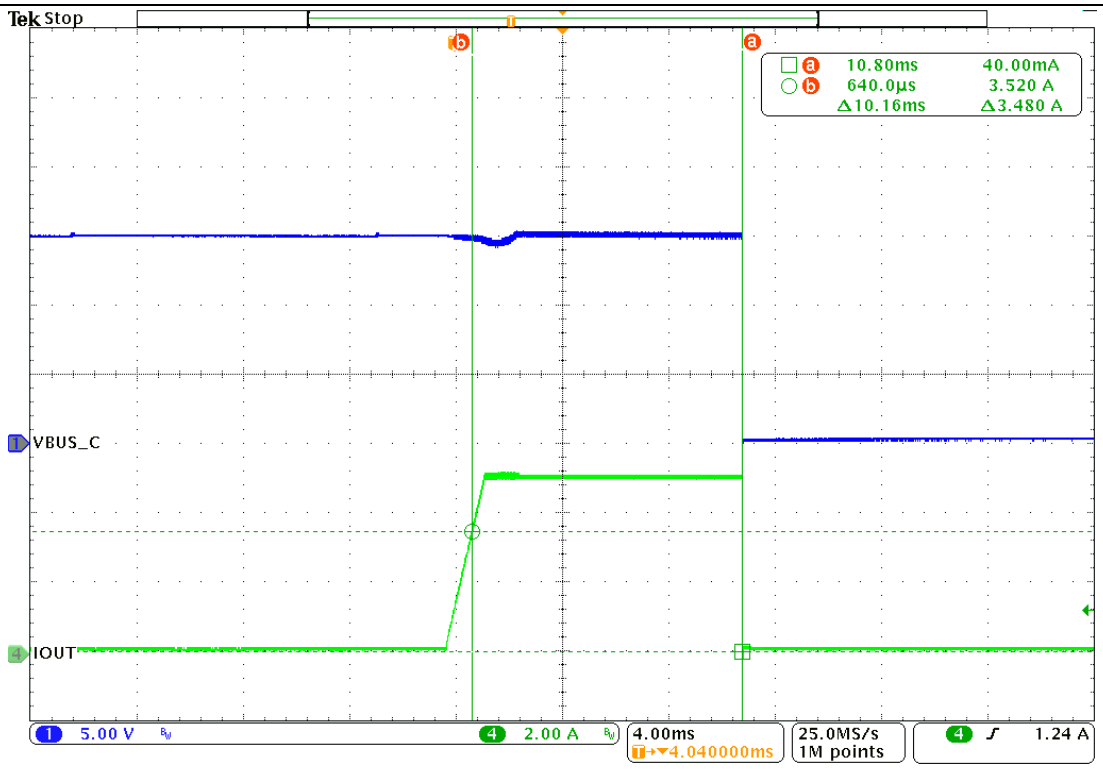
OCP tested at 115 V_{AC} 60 Hz



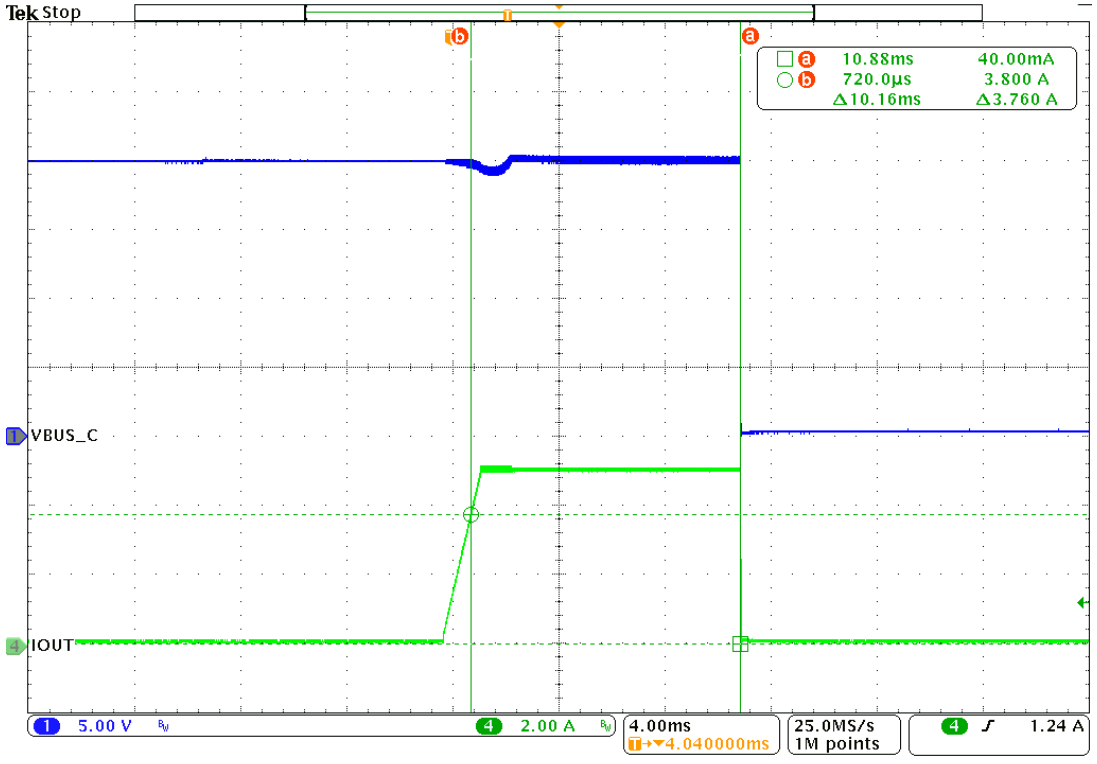
Fixed PDO: 5 V, 3 A; OCP_trip point = 3.53 A; OCP_response time = 10.2 ms



Fixed PDO: 9 V, 3 A; OCP_trip point = 3.53 A; OCP_response time = 10.16 ms



Fixed PDO: 15 V, 3 A; OCP_trip point = 3.53 A; OCP_response time = 10.16 ms

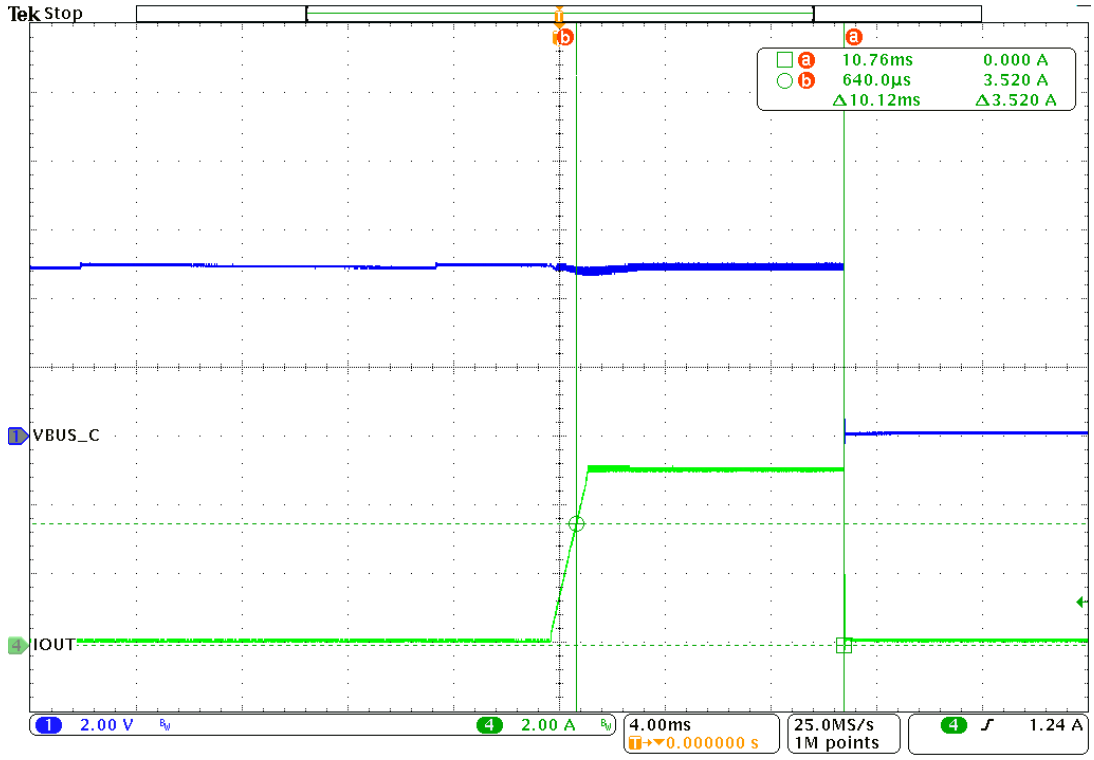


Fixed PDO: 20 V, 3.25 A; OCP_trip point = 3.81 A; OCP_response time = 10.16 ms

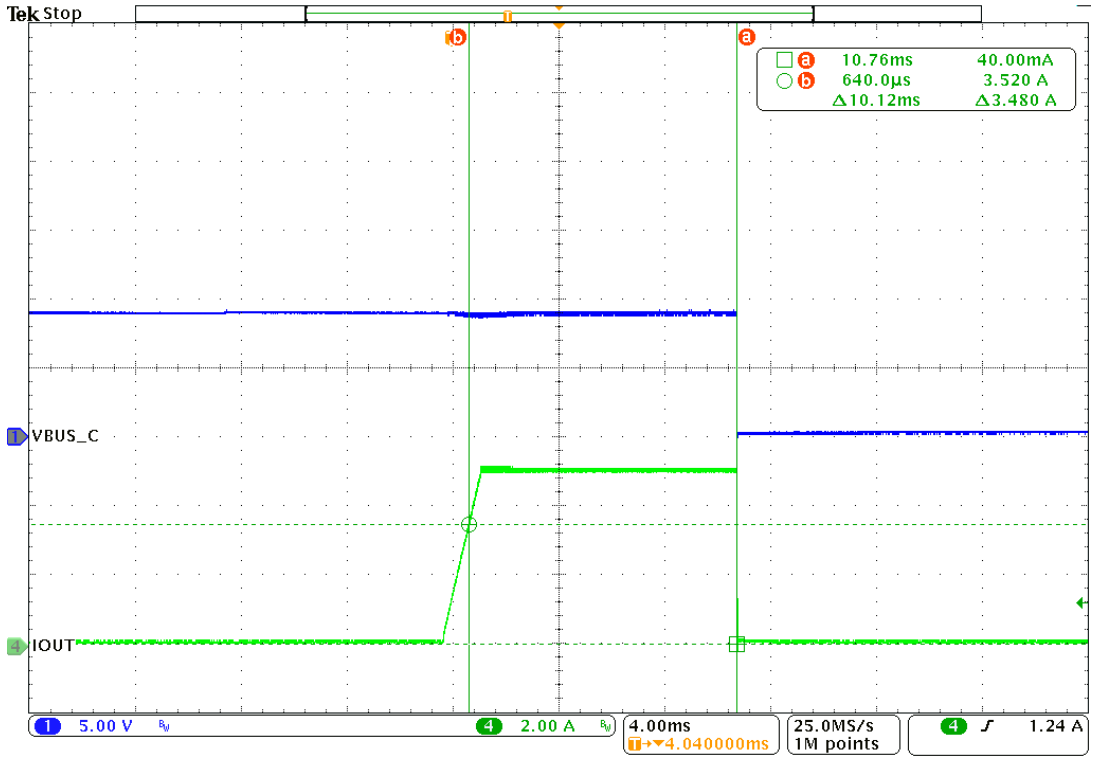
Figure 56 OCP at 115 V_{AC}, 60 Hz (CH1: V_{BUS_C}; CH3: I_{OUT})

Power management test results

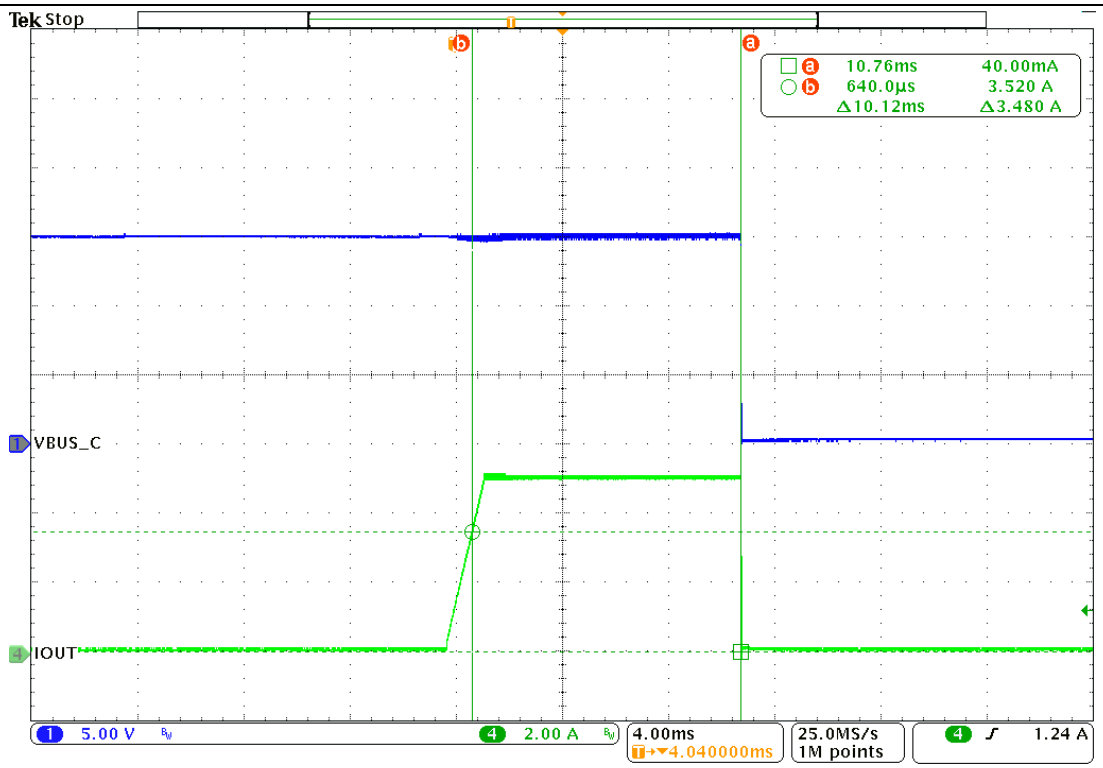
OCP tested at 230 V_{AC} 50 Hz



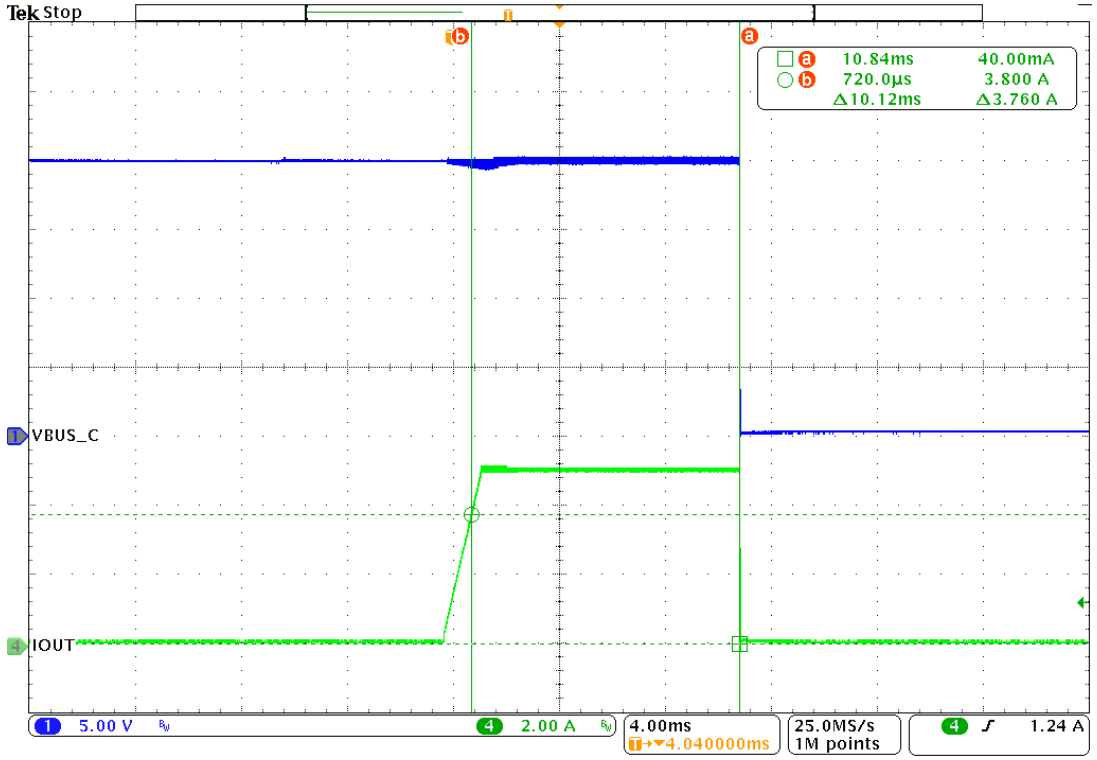
Fixed PDO: 5 V, 3 A; OCP_trip point = 3.53 A; OCP_response time = 10.12 ms



Fixed PDO: 9 V, 3 A; OCP_trip point = 3.53 A; OCP_response time = 10.12 ms



Fixed PDO: 15 V, 3 A; OCP_trip point = 3.53 A; OCP_response time = 10.12 ms



Fixed PDO: 20 V, 3.25 A; OCP_trip point = 3.82 A; OCP_response time = 10.12 ms

Figure 57 OCP at 230 V_{AC}, 50 Hz (CH1: V_{BUS_C}; CH3: I_{OUT})

3.19 Thermal stress

- **Test condition**: V_{IN_AC} = 90 V_{AC}-47 Hz, V_{OUT} = 20 V, I_{OUT} = 3.25 A
- **Lab ambient temperature**: 24°C and in open frame
- **Run time**: 60 minutes

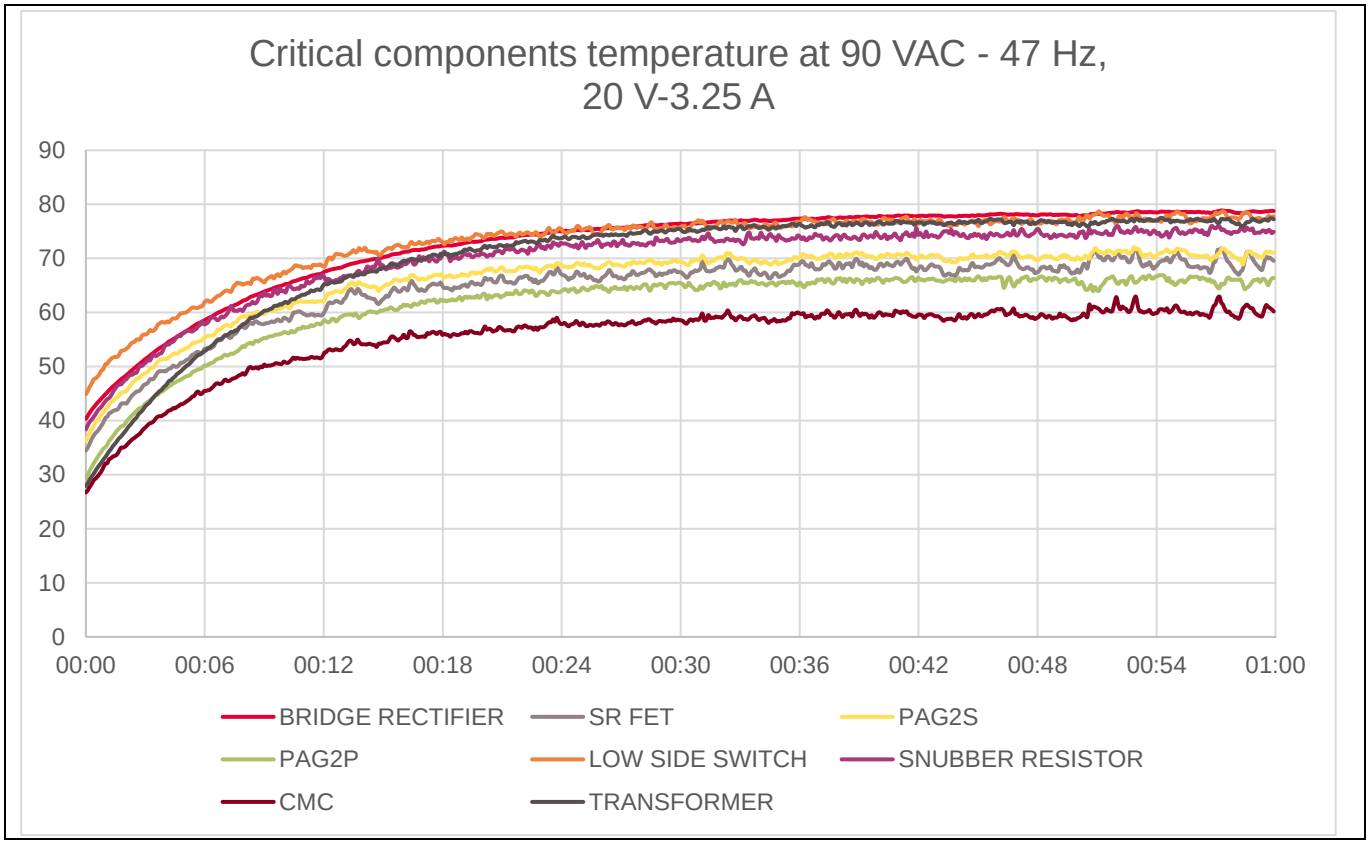


Figure 58 Thermal data logging of various components with time at 90 V_{AC} - 47 Hz, 20 V, 3.25 A

Table 16 Thermal data logging of various components at the end of 60 mins at 90 V_{AC} - 47 Hz, 20 V, 3.25 A

Sl. No.	Component	Max temp in °C at the end of 60 mins
1	Bridge rectifier	78.16
2	SR FET	69.53
3	CMC	60.18
4	Transformer	77.21
5	PAG2P (Primary IC)	66.37
6	PAG2S (Secondary IC)	71.01
7	Low side switch	77.80
8	Snubber resistor	74.91

Power management test results

- **Test condition**: V_{IN_AC} = 115 V_{AC} -60Hz, V_{OUT} = 20V, I_{OUT} = 3.25 A
- **Lab ambient temperature**: 24°C and in open frame
- **Run time**: 60 minutes

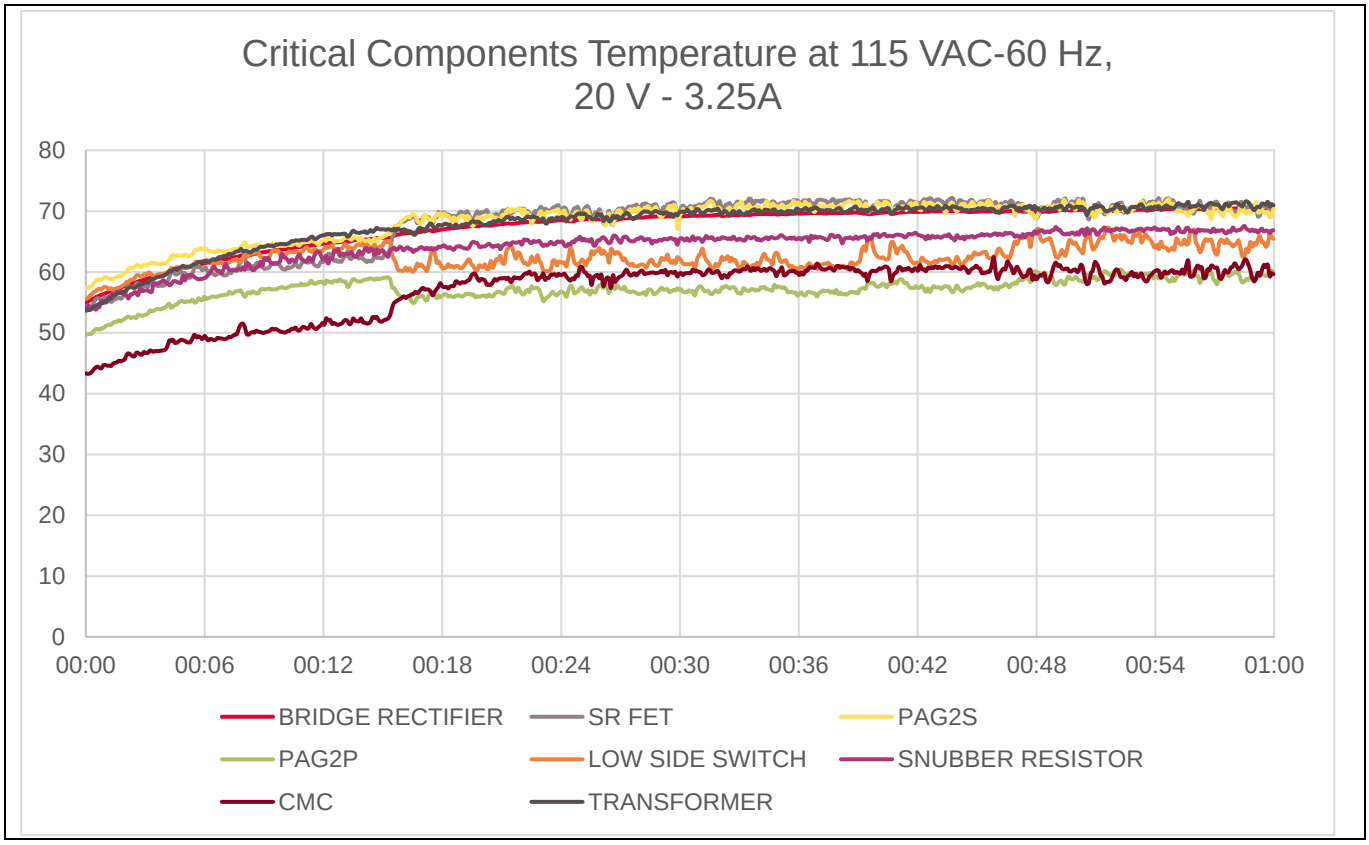


Figure 59 Thermal data logging of various components with time at 115 V_{AC} - 60 Hz, 20 V, 3.25 A

Table 17 Thermal data logging of various components at the end of 60 mins at 115 V_{AC} – 60 Hz, 20 V, 3.25 A

Sl. No.	Component	Max temp in °C at the end of 60 mins
1	Bridge rectifier	70.38
2	SR FET	70.96
3	CMC	59.60
4	Transformer	70.96
5	PAG2P (Primary IC)	60.00
6	PAG2S (Secondary IC)	70.36
7	Low side switch	65.43
8	Snubber resistor	66.84

Power management test results

- **Test condition**: V_{IN_AC} = 230 V_{AC}-50 Hz, V_{OUT} = 20 V, I_{OUT} = 3.25 A
- **Lab ambient temperature**: 24°C and in open frame
- **Run time**: 60 minutes

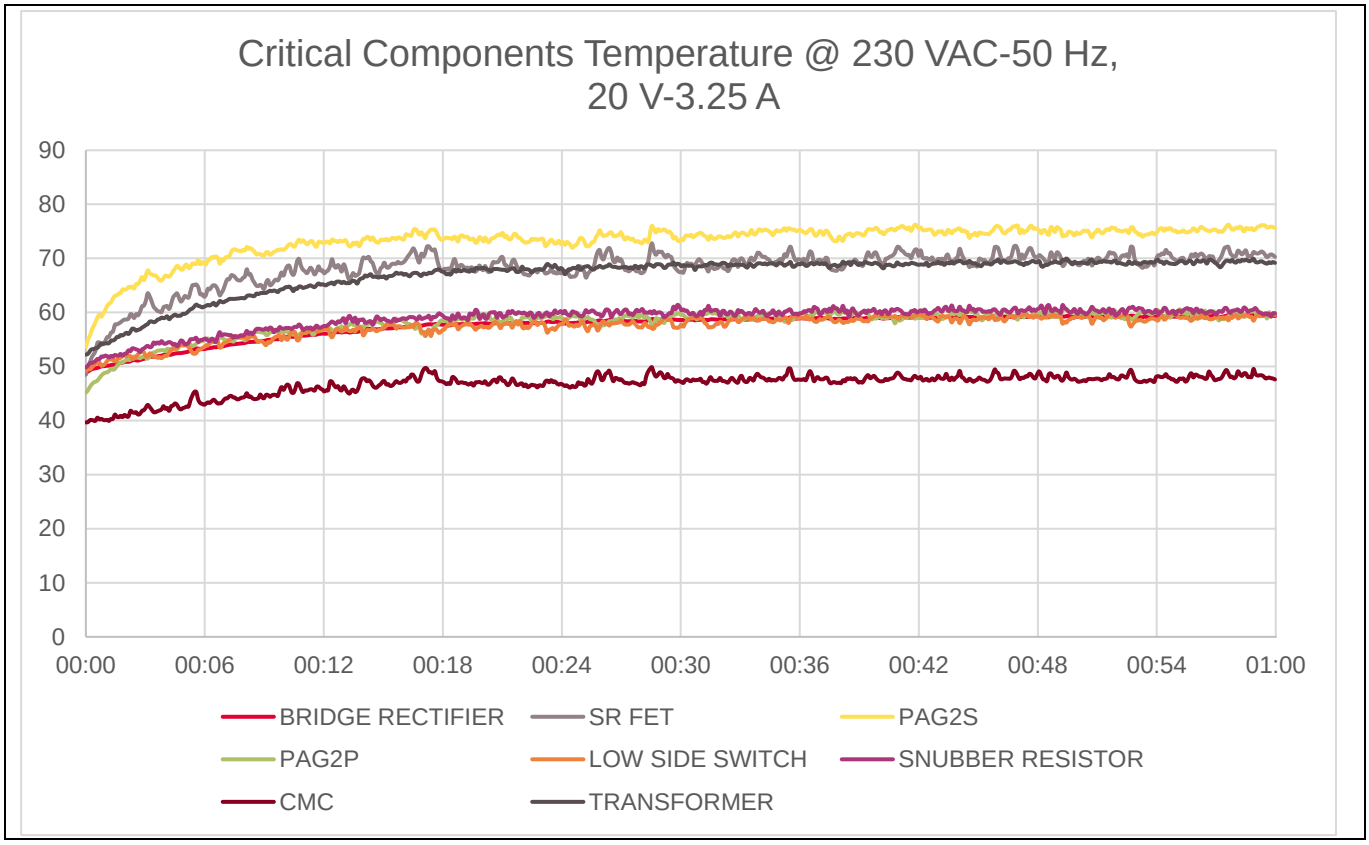


Figure 60 Thermal data logging of various components with time at 230 V_{AC} - 50 Hz, 20 V, 3.25 A

Table 18 Thermal data logging of various components at the end of 60 mins at 230 V_{AC} - 50 Hz, 20 V, 3.25 A

Sl. No.	Component	Max. temp in °C at the end of 60 mins
1	Bridge rectifier	59.34
2	SR FET	70.28
3	CMC	47.60
4	Transformer	69.16
5	PAG2P (Primary IC)	59.89
6	PAG2S (Secondary IC)	75.57
7	Low side switch	59.56
8	Snubber resistor	59.84

Power management test results

- **Test condition**: V_{IN_AC} = 265 V_{AC}-63 Hz, V_{OUT} = 20 V, I_{OUT} = 3.25 A
- **Lab ambient temperature**: 24°C and in open frame
- **Run time**: 60 minutes

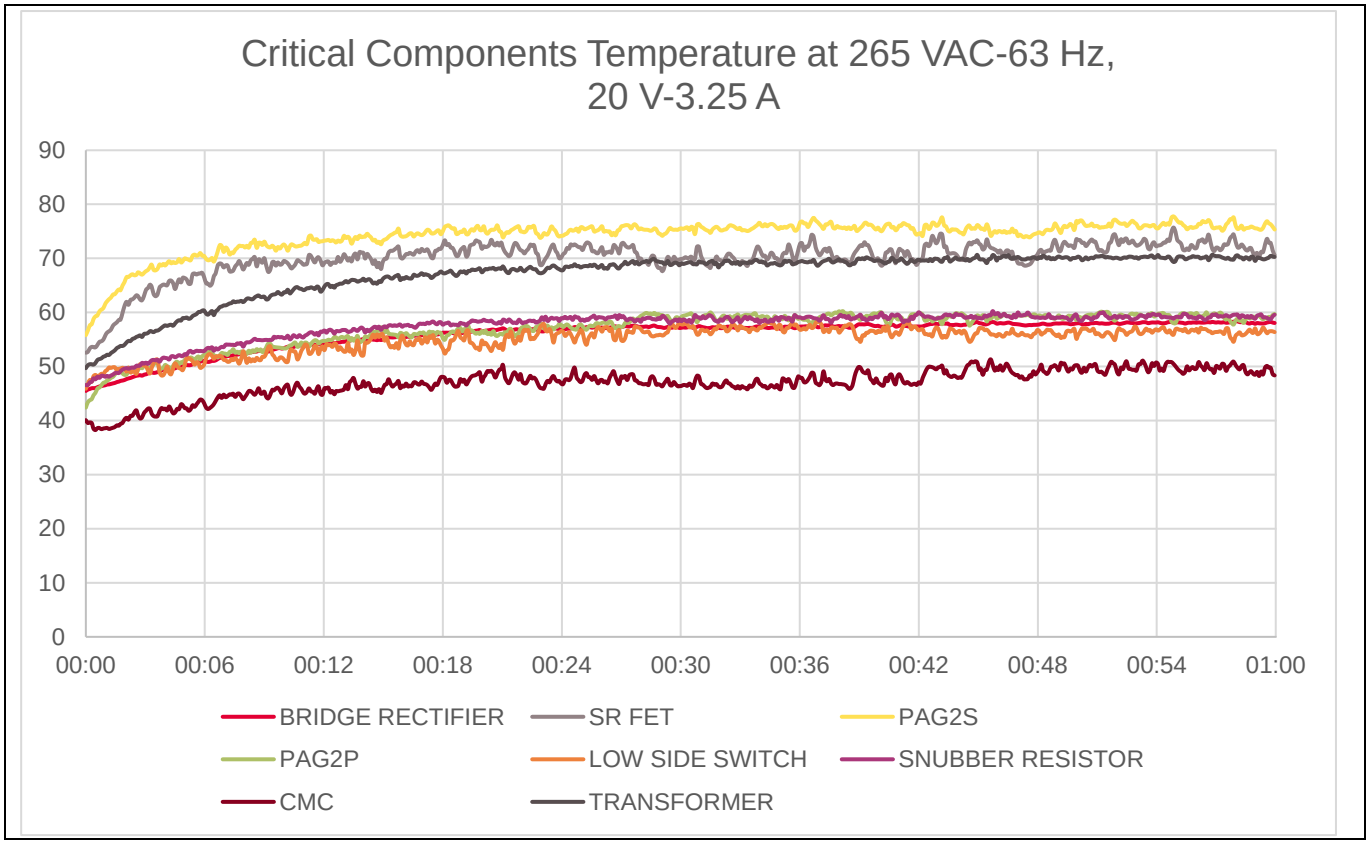


Figure 61 Thermal data logging of various components with time at 265 V_{AC} – 63 Hz, 20 V, 3.25 A

Table 19 Thermal data logging of various components at the end of 60 mins at 265 V_{AC}-63 Hz, 20 V, 3.25 A

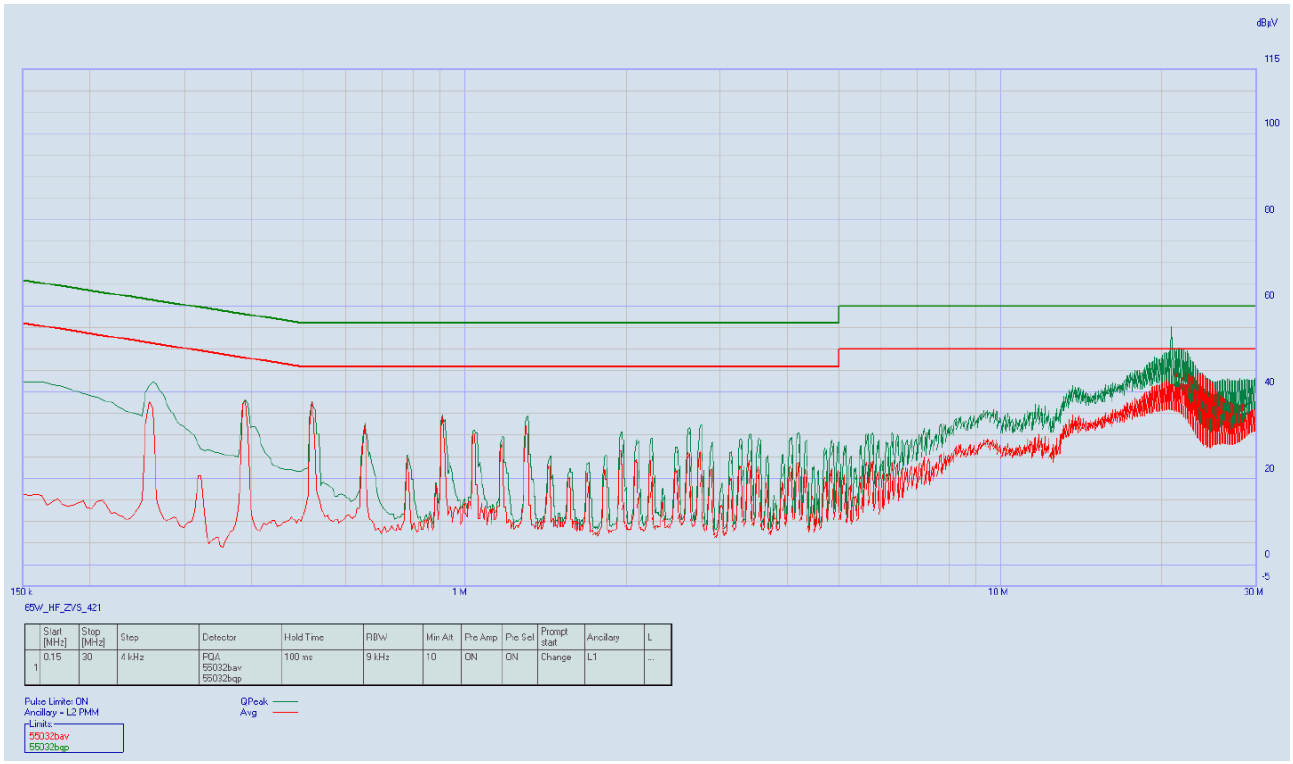
Sl. No.	Component	Max. temp in °C at the end of 60 mins
1	Bridge rectifier	58.04
2	SR FET	70.58
3	CMC	48.35
4	Transformer	70.26
5	PAG2P (Primary IC)	59.70
6	PAG2S (Secondary IC)	75.34
7	Low side switch	56.36
8	Snubber resistor	59.58

3.20 EMI/EMC

3.20.1 Conducted emission

Requirements: Class B CISPR 32, EN55032 – 4 dB margin at 115/230 V_{AC}
Remarks: The CE results are captured with an additional shield on the transformer and CMC, refer to the image below.

Conducted emission L1 at 230 V_{AC} 50 Hz



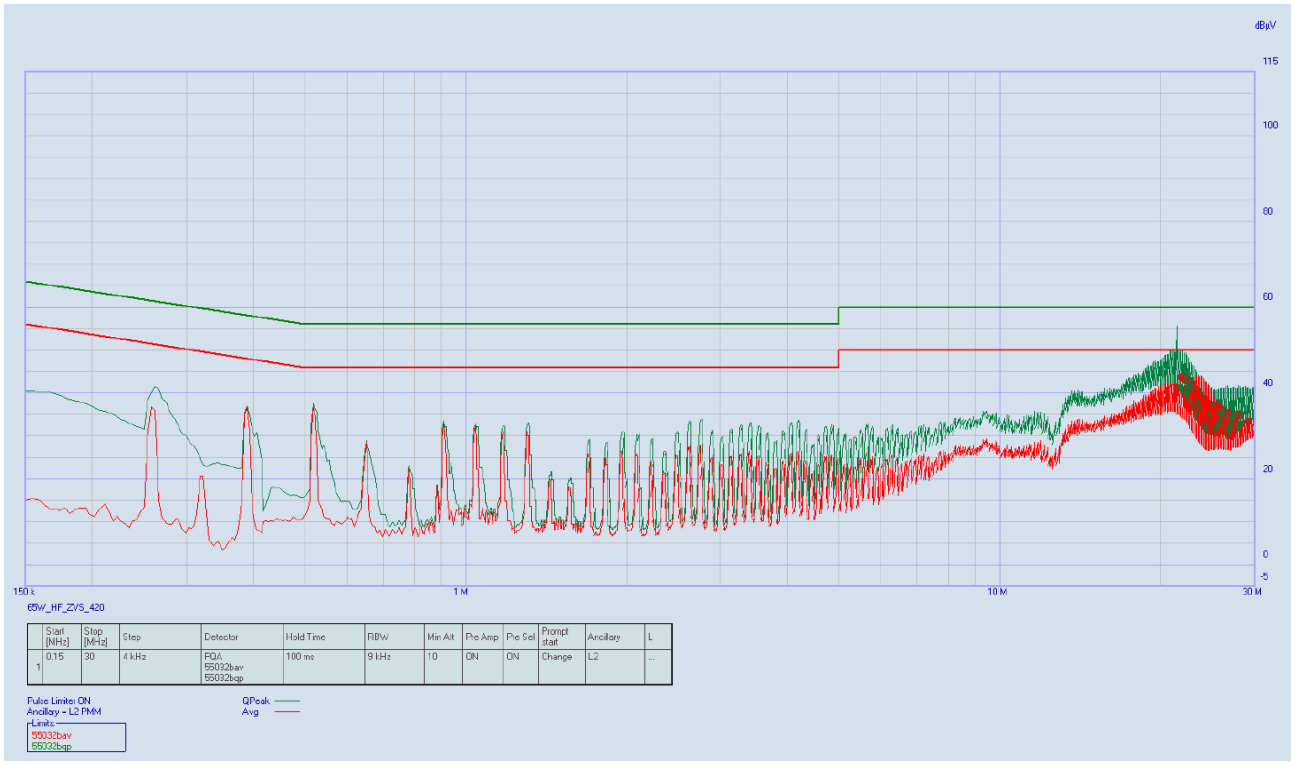
	Frequency [MHz]	Avg [dBµV]	Limit 55032bav [dBµV]	Delta [dB]	QPeak [dBµV]	Limit 55032bqp [dBµV]	Delta [dB]
1	20.754	42.99	50.00	---	55.35	60.00	-4.65
2	20.758	42.05	50.00	---	55.22	60.00	-4.78
3	21.386	44.64	50.00	-5.36	48.95	60.00	---
4	21.514	44.52	50.00	-5.48	48.84	60.00	---
5	21.53	44.52	50.00	-5.48	49.98	60.00	---
6	22.042	44.57	50.00	-5.43	48.09	60.00	---

QP: 4.65dB PASS

Figure 62 CE at 230 V_{AC} 20 V full load with trace L1

Power management test results

Conducted Emission L2 at 230 V_{AC} 50 Hz



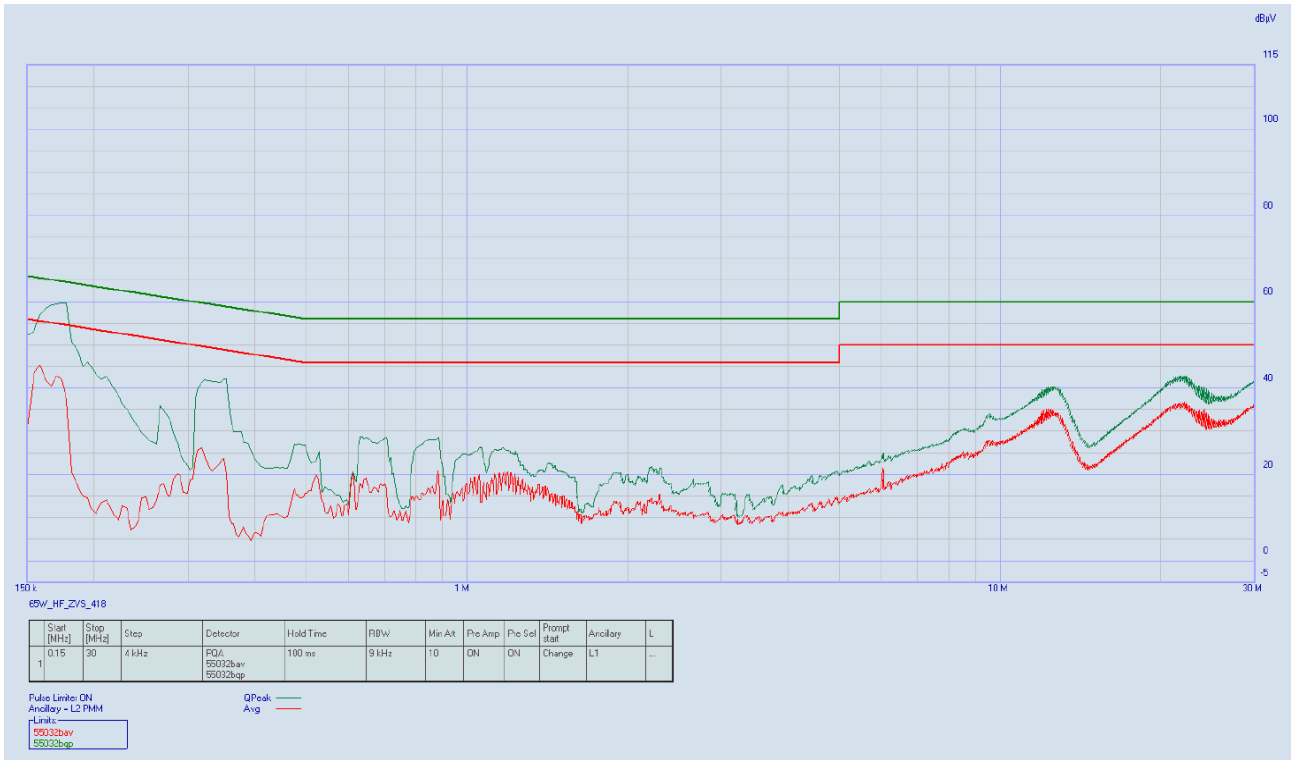
	Frequency [MHz]	Avg [dBµV]	Limit 55032bav [dBµV]	Delta [dB]	QPeak [dBµV]	Limit 55032bqp [dBµV]	Delta [dB]
1	21.39	44.52	50.00	-5.48	48.78	60.00	---
2	21.394	43.54	50.00	---	55.51	60.00	-4.49
3	21.398	43.50	50.00	---	54.58	60.00	-5.42
4	21.406	43.17	50.00	---	55.75	60.00	-4.25
5	21.41	42.49	50.00	---	55.56	60.00	-4.44
6	21.79	44.57	50.00	-5.43	49.60	60.00	---

QP: 4.44 dB PASS

Figure 63 CE at 230 V_{AC} 20V full load with trace L2

Power management test results

Conducted Emission L1 at 115 V_{AC} 60 Hz

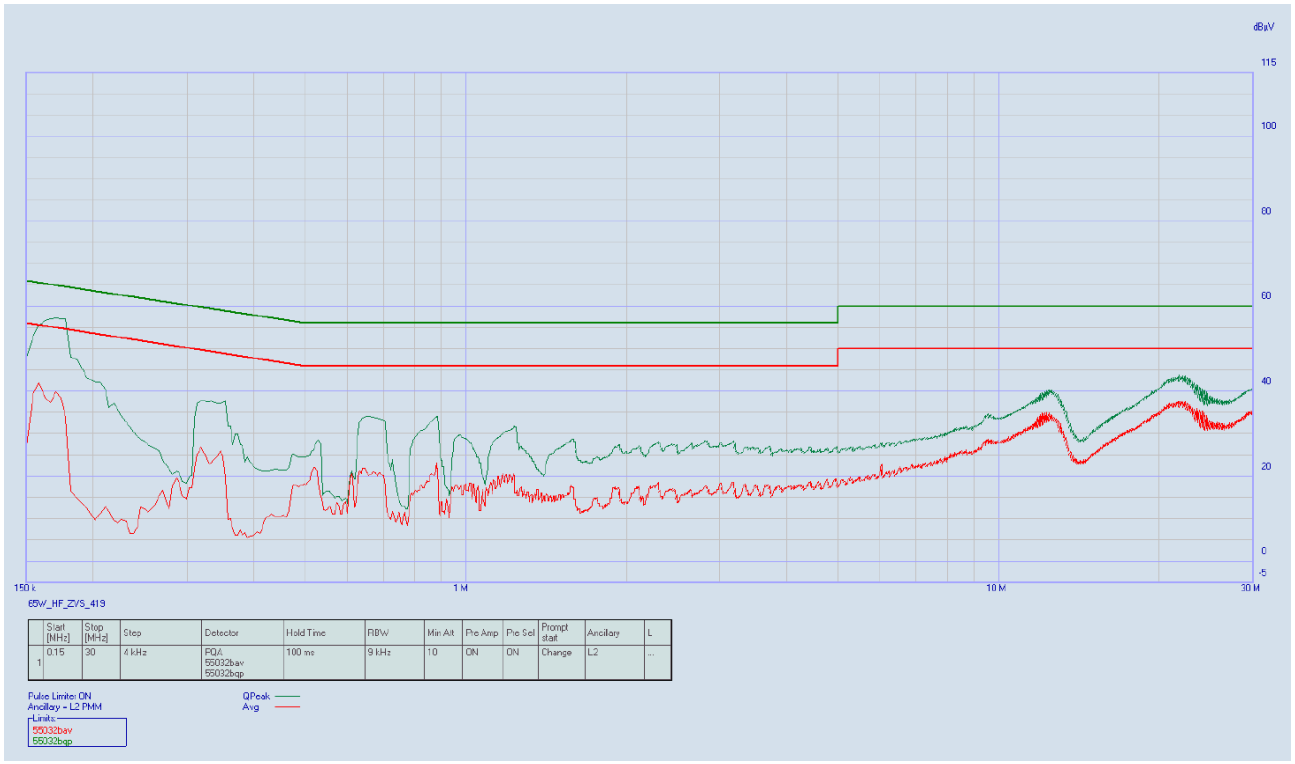


	Frequency [MHz]	Avg [dBµV]	Limit 55032bav [dBµV]	Delta [dB]	QPeak [dBµV]	Limit 55032bqp [dBµV]	Delta [dB]
1	0.158	45.38	55.57	---	57.03	65.57	-8.54
2	0.162	41.79	55.36	---	58.60	65.36	-6.76
3	0.166	40.59	55.16	---	59.30	65.16	-5.86
4	0.17	42.97	54.96	---	59.58	64.96	-5.38
5	0.174	41.85	54.77	---	59.66	64.77	-5.11
6	0.178	37.38	54.58	---	59.64	64.58	-4.94

QP: 4.94dB PASS

Figure 64 CE at 115 V_{AC} 20V full load with trace L1

Conducted Emission L2 at 115 V_{AC} 60 Hz



	Frequency [MHz]	Avg [dBµV]	Limit 55032bav [dBµV]	Delta [dB]	QPeak [dBµV]	Limit 55032bqp [dBµV]	Delta [dB]
1	0.162	38.57	55.36	---	56.71	65.36	-8.65
2	0.166	37.36	55.16	---	57.05	65.16	-8.11
3	0.17	39.80	54.96	---	57.16	64.96	-7.80
4	0.174	38.42	54.77	---	57.12	64.77	-7.65
5	0.178	33.81	54.58	---	57.12	64.58	-7.46

QP: 7.46dB PASS

Figure 65 CE at 115 V_{AC} 20 V full load with trace L2

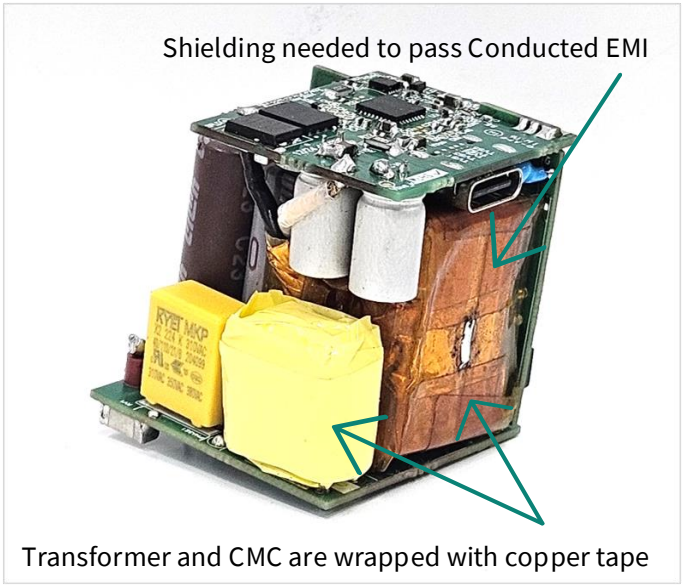


Figure 66 DUT Images with CE modifications

3.20.2 Surge

Requirements: IEC61000-4-5, ±1 kV DM and ±2 kV CM, Criteria B (auto-recovery)

Test Condition: V_{AC}: 230 V_{AC}, 50 Hz, V_O = 20 V, I_O = 3.25 A
Combination wave surge: ±1 kV DM at 0°, 90°, and 270° - 5 pulses each with 60 s interval between pulses.

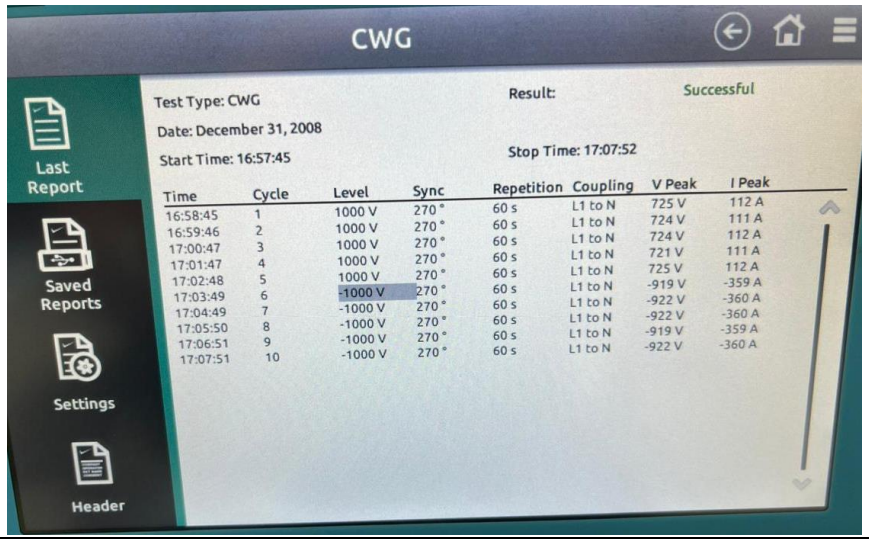


Figure 67 Surge test report for ±1 kV DM at 270°

3.20.3 ESD

Requirements: IEC61000-4-2 level 4; ±8 kV contact, ±16 kV air, Criteria A

Test Condition: V_{AC}: 230 V_{AC}, 50 Hz, V_O = 20 V, I_O = 3.25 A, 10 pulse each, vertical and horizontal plane with all orientations.

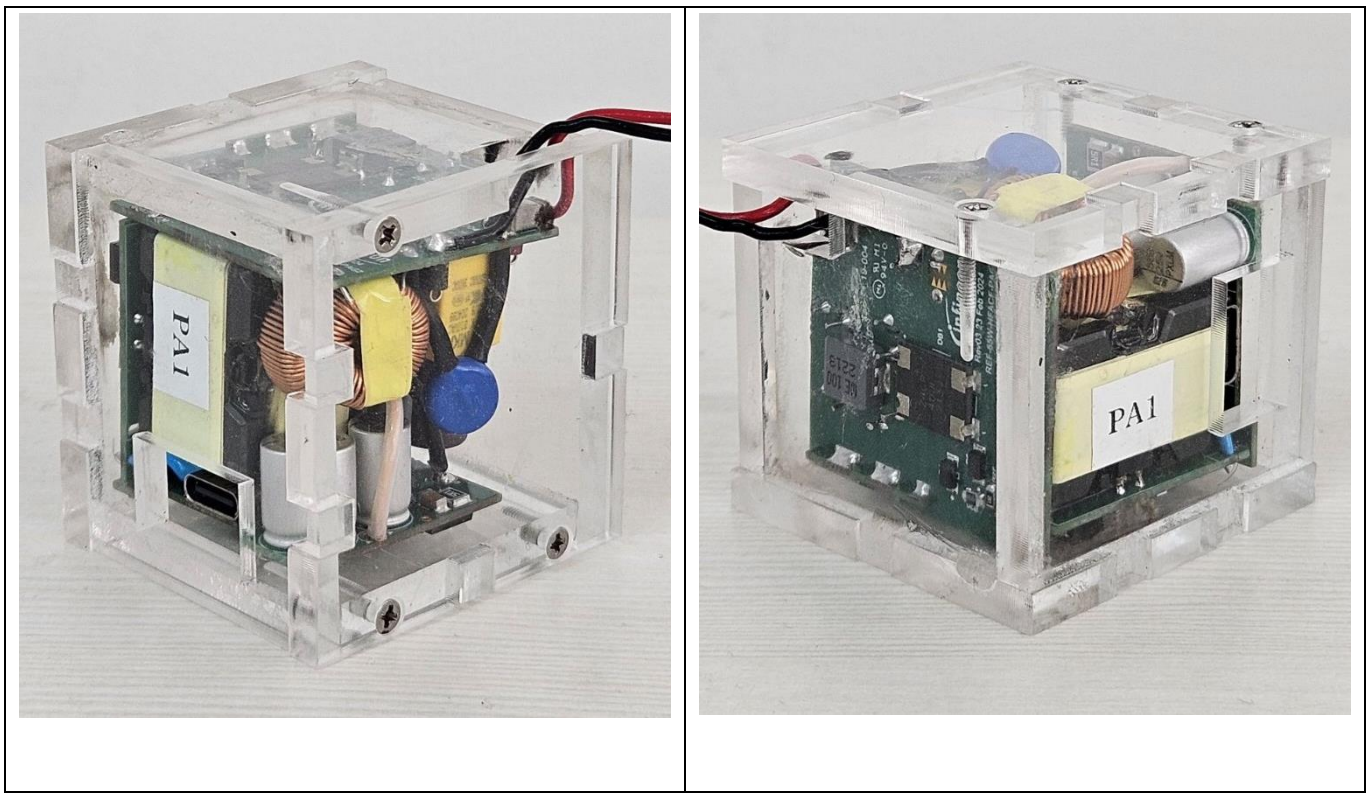
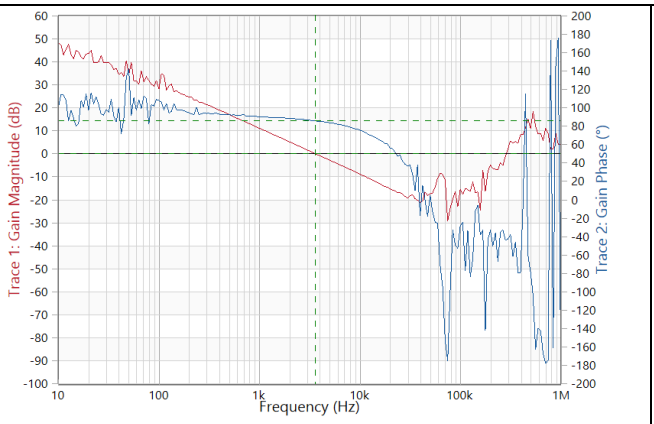
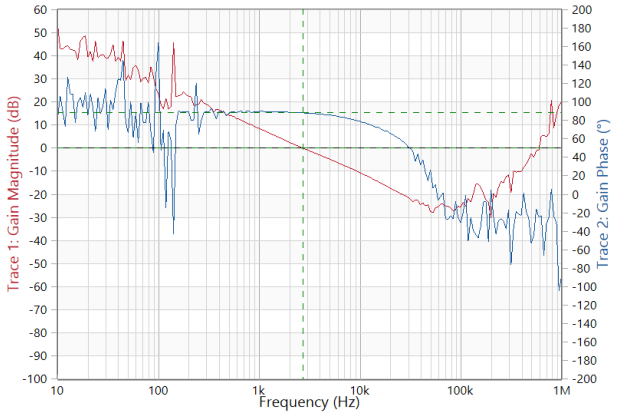


Figure 68 Device set-up for ESD test

3.21 Bode stability

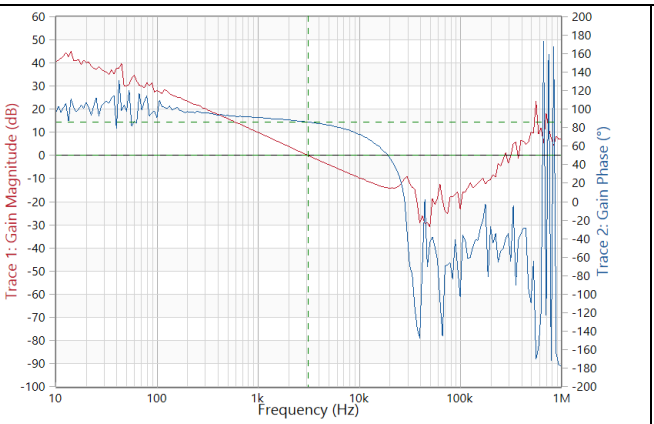


PDO – 5 V, 3 A

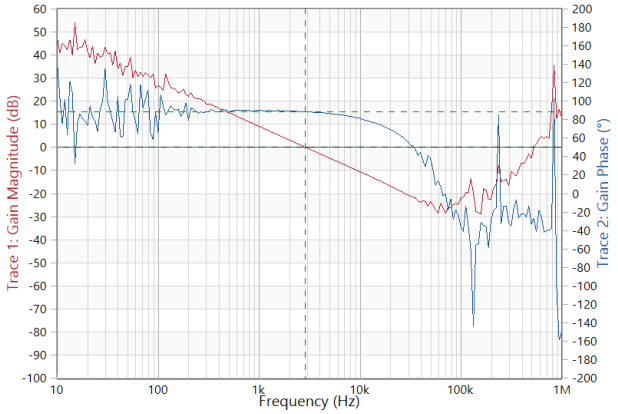


PDO – 20 V, 3.25 A

Figure 69 Loop stability at 115 V_{AC}, 60 Hz



PDO – 5 V, 3 A



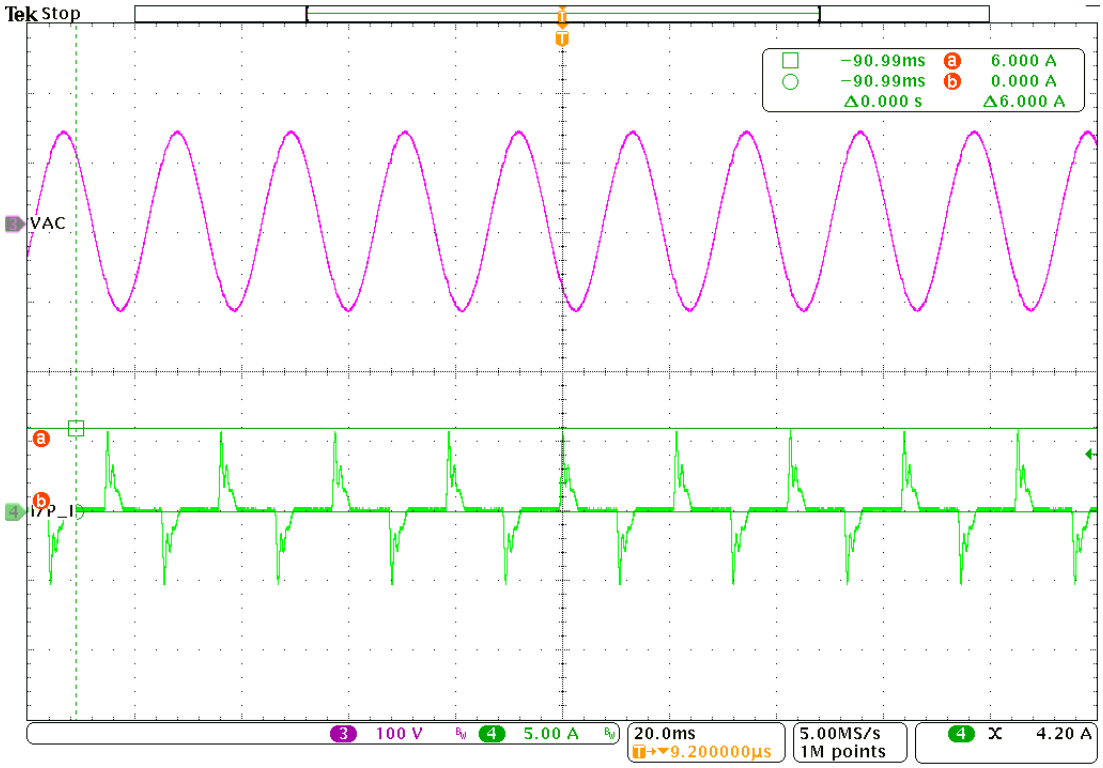
PDO – 20 V, 3.25 A

Figure 70 Loop stability at 230 V_{AC}, 50 Hz

Table 20 Loop stability data for all output conditions

V_{IN}	Vout	Load current	Cross over frequency (Hz)	Phase margin
115 V_{AC}	5 V	3 A	3.626 k	85.86
	9 V	3 A	3.31 k	87.01
	15 V	3 A	2.901 k	87.62
	20 V	3.25 A	2.702 k	88.37
	5 V	0.6 A	1.47 k	88.38
	9 V	0.6 A	1.188 k	88.54
	15 V	0.6 A	970.03 k	88.06
	20 V	0.65 A	912.75 k	88.04
230 V_{AC}	5 V	3 A	3.115 k	86.05
	9 V	3 A	2.901 k	88.1
	15 V	3 A	2.991 k	88.27
	20 V	3.25 A	2.872 k	88.48
	5 V	0.6 A	1.729 k	62.83
	9 V	0.6 A	1.729 k	70.54
	15 V	0.6 A	1.031 k	88.39
	20 V	0.65 A	931.46 k	88.05

3.22 Maximum input current in steady state

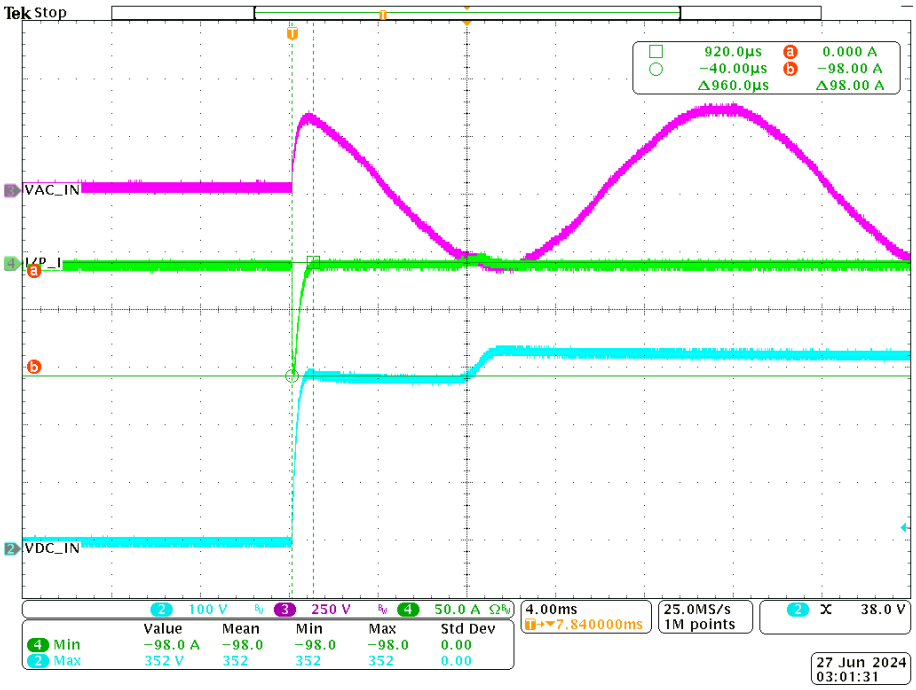


V_{OUT} = 20 V, I_{OUT} = 3.25 A

Input rms current (from power meter) = 1.28 A, Input peak current = 6 A

Figure 71 Input current at steady state, 90 V_{AC}, 47 Hz (CH3: V_{AC}, CH4: I_{AC})

3.23 Inrush current at cold start



V_{OUT} = 5 V, I_{OUT}=0 A

Input peak current = 98 A

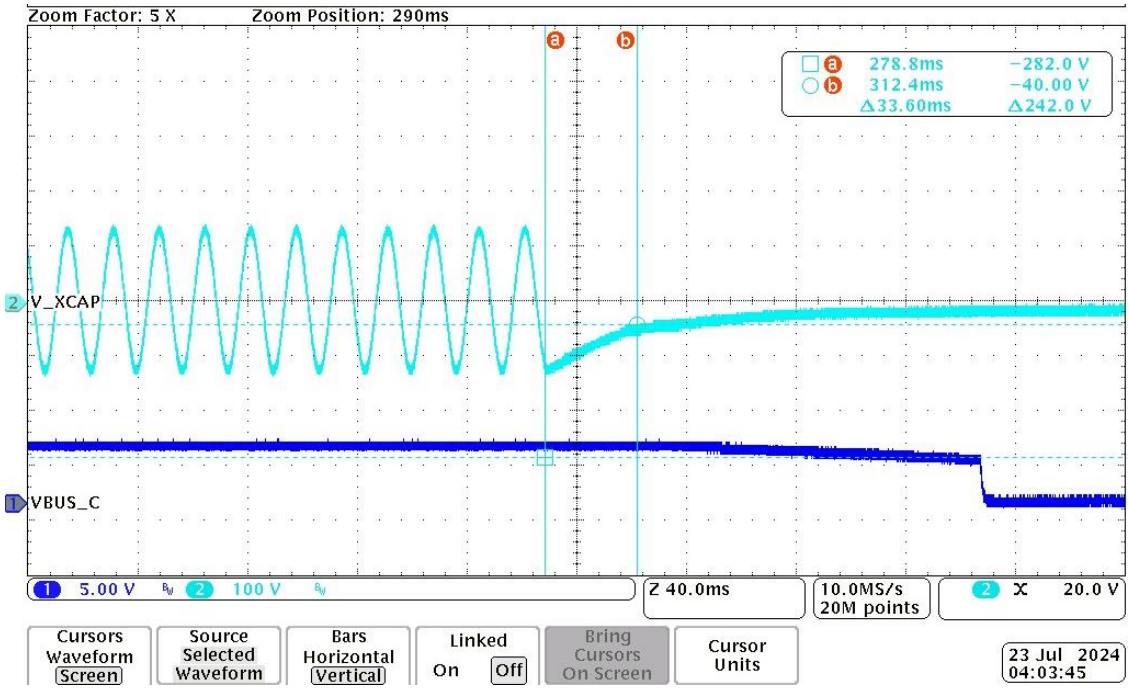
Figure 72 Inrush current at cold start 230 V_{AC}, 50 Hz (CH2: V_{DC_IN} CH3: V_{AC}, CH4: I_{AC})

3.24 Brown-out recovery

Table 21 Brown-out data

Test Condition	Result	
V_O = 5 V_{DC}, I_O = 0 A (No load)	UVLO falling	74.2 V_{AC}
	UVLO rising	75.8 V_{AC}
V_O = 20 V_{DC}, I_O = 3.25A (Full load)	UVLO falling	75.3 V_{AC}
	UVLO rising	76.5 V_{AC}

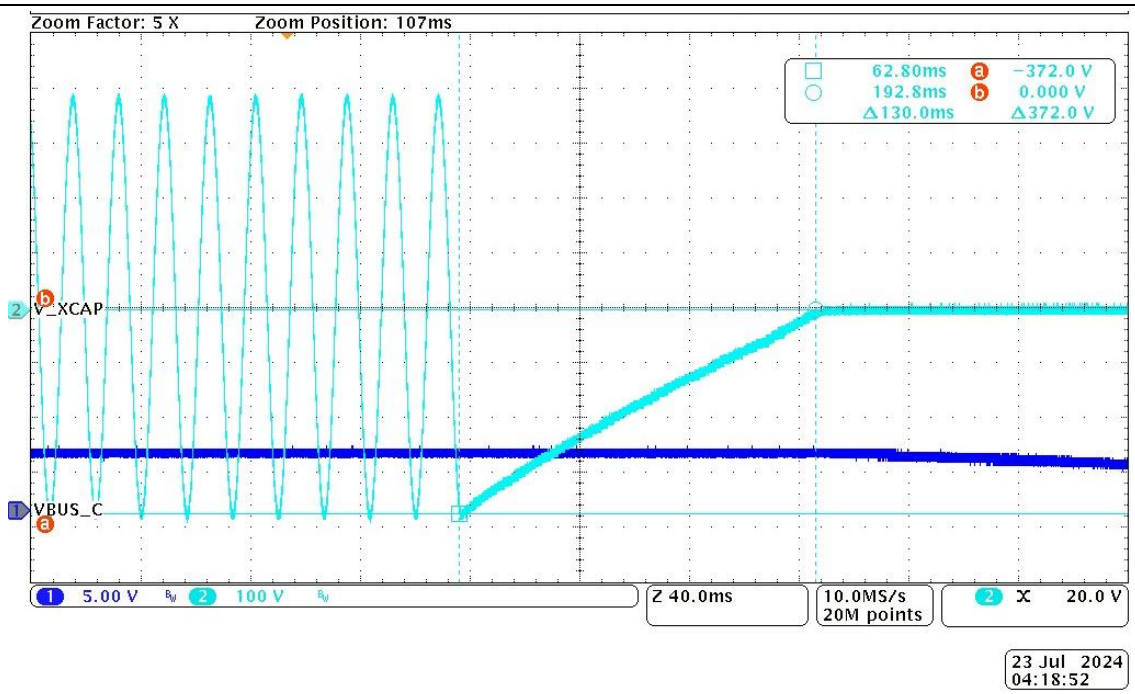
3.25 X-cap discharge



V_{OUT} = 5 V, No load

90 V_{AC}, X-cap discharge time = 33.6 ms

Figure 73 X-cap discharge at 90 V_{AC},47 Hz (CH1: V_{BUS_C}, CH2: V_{AC})

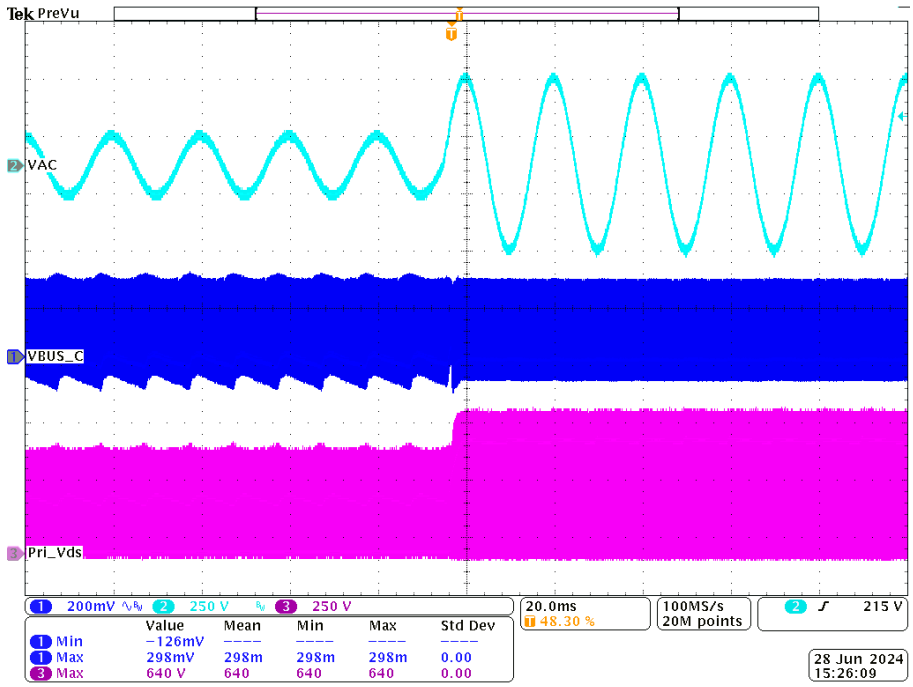


V_{OUT} = 20 V, No load

265 V_{AC}, X-cap discharge time = 130 ms

Figure 74 X-cap discharge at 265 V_{AC},63 Hz (CH1: V_{BUS_C}, CH2: V_{AC})

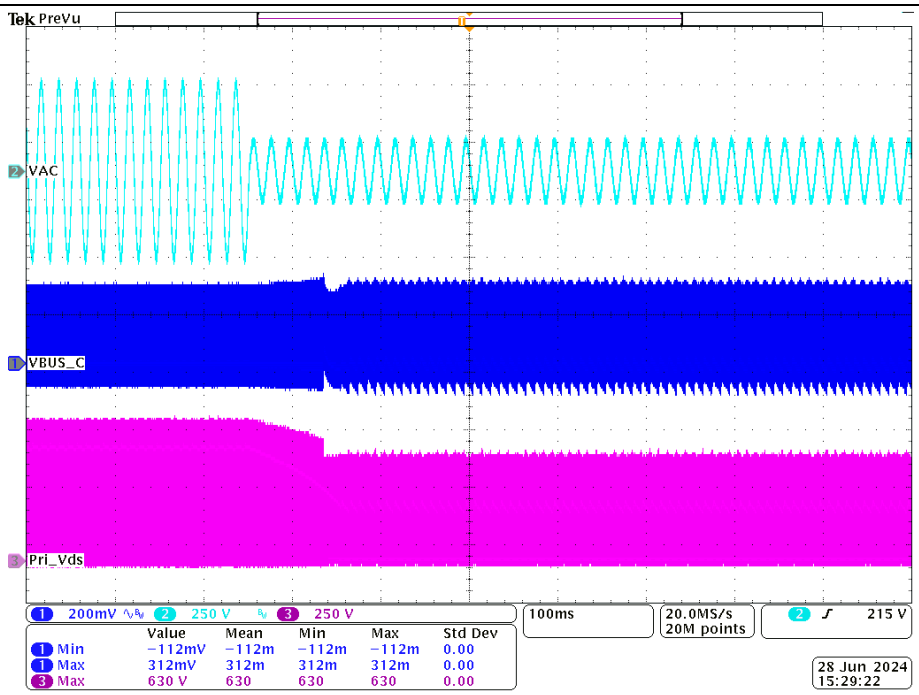
3.26 V_O steady state response with line transition



V_{OUT} = 20 V, I_{OUT} = 3.25 A

Delta V_O = 424 mV, Primary V_{DS} = 640 V

Figure 75 Line transition from 90 V_{AC}, 50 Hz to 265 V_{AC}, 50 Hz (CH1: V_{BUS_C}, CH2: V_{AC}, CH3: Pri_V_{DS})



V_{OUT} = 20 V, I_{OUT} = 3.25 A

Delta V_O = 424 mV, Primary V_{DS} = 630 V

Figure 76 Line transition from 265 V_{AC}, 50 Hz to 90 V_{AC}, 50 Hz (CH1: V_{BUS_C}, CH2: V_{AC}, CH3: Pri_V_{DS})

3.27 Hi-POT test

Test condition: Mode: ACW, Voltage: 3 kV, Timer: 2 s, Hi-SET: 1 mA, Lo-SET: 0 mA

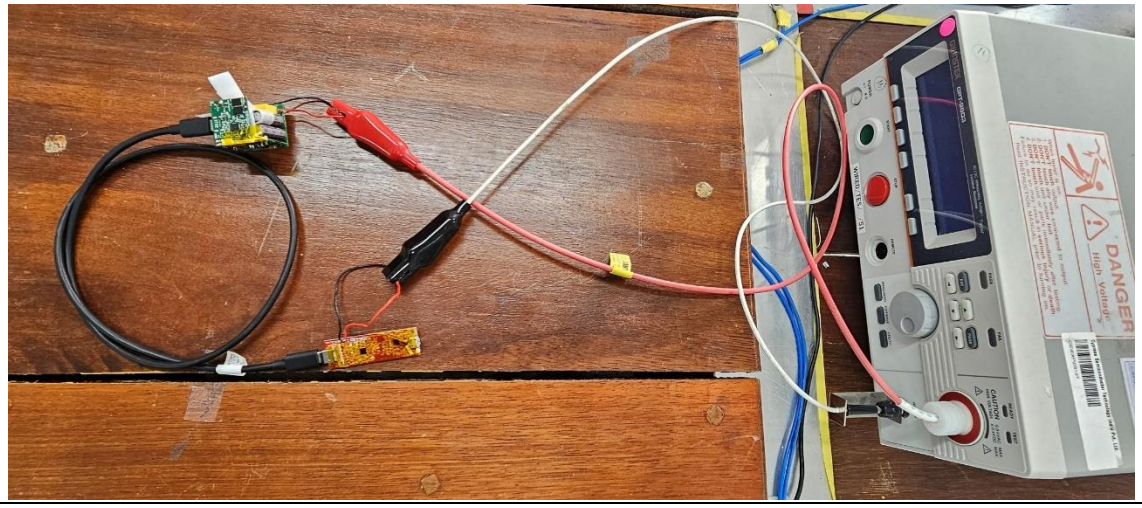


Figure 77 Hi-POT test setup

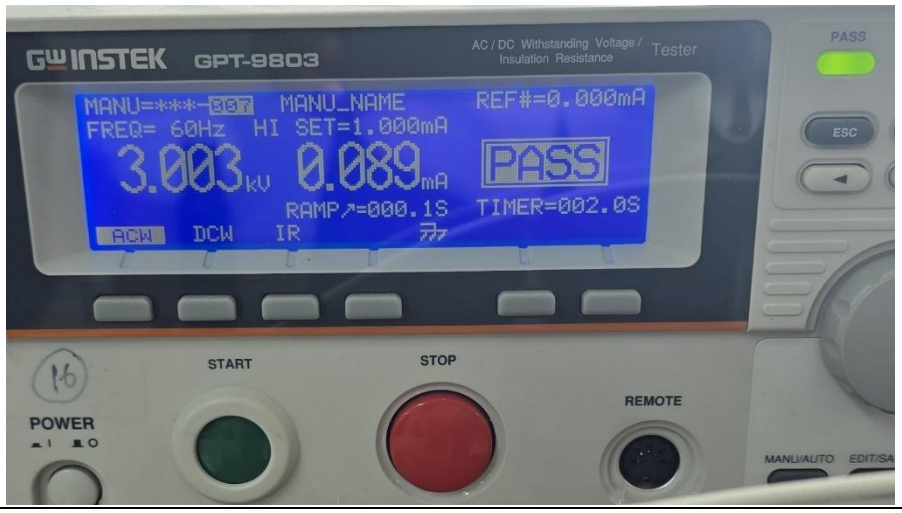


Figure 78 Hi-POT test result

4 USB PD source test results (using QuadraMAX)

4.1 Test setup

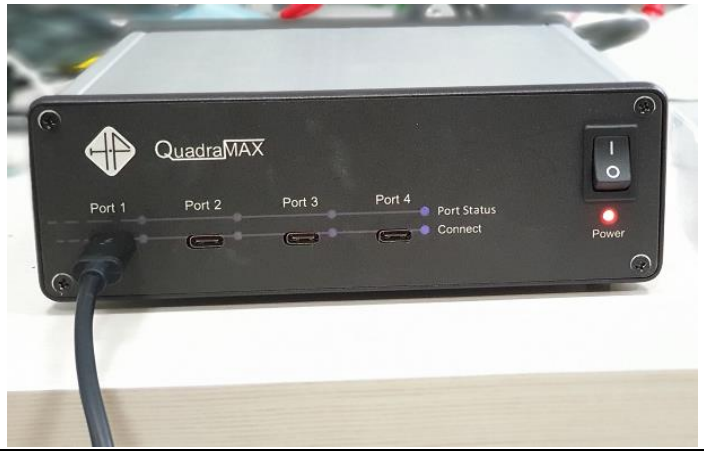


Figure 79 QuadraMAX tester

- QuadDraw Version: 0.9.8594
- QM#108 HW Rev: 1.4.4 FWST:0.0.1376 FWCCG1:0.10

4.2 Test results

Test input voltage conditions: 115 V_{AC}, 60 Hz and 230 V_{AC}, 50 Hz

Table 22 QuadraMAX test results

Test	Description	Result
TD SPT.1	Load test	PASS
TD SPT.2	Capabilities	PASS
TD SPT.3	Hard reset test	PASS
TD SPT.6	PPS voltage step test	PASS
TD SPT.7	PPS current limit test	PASS

5 Appendix

5.1 Schematic

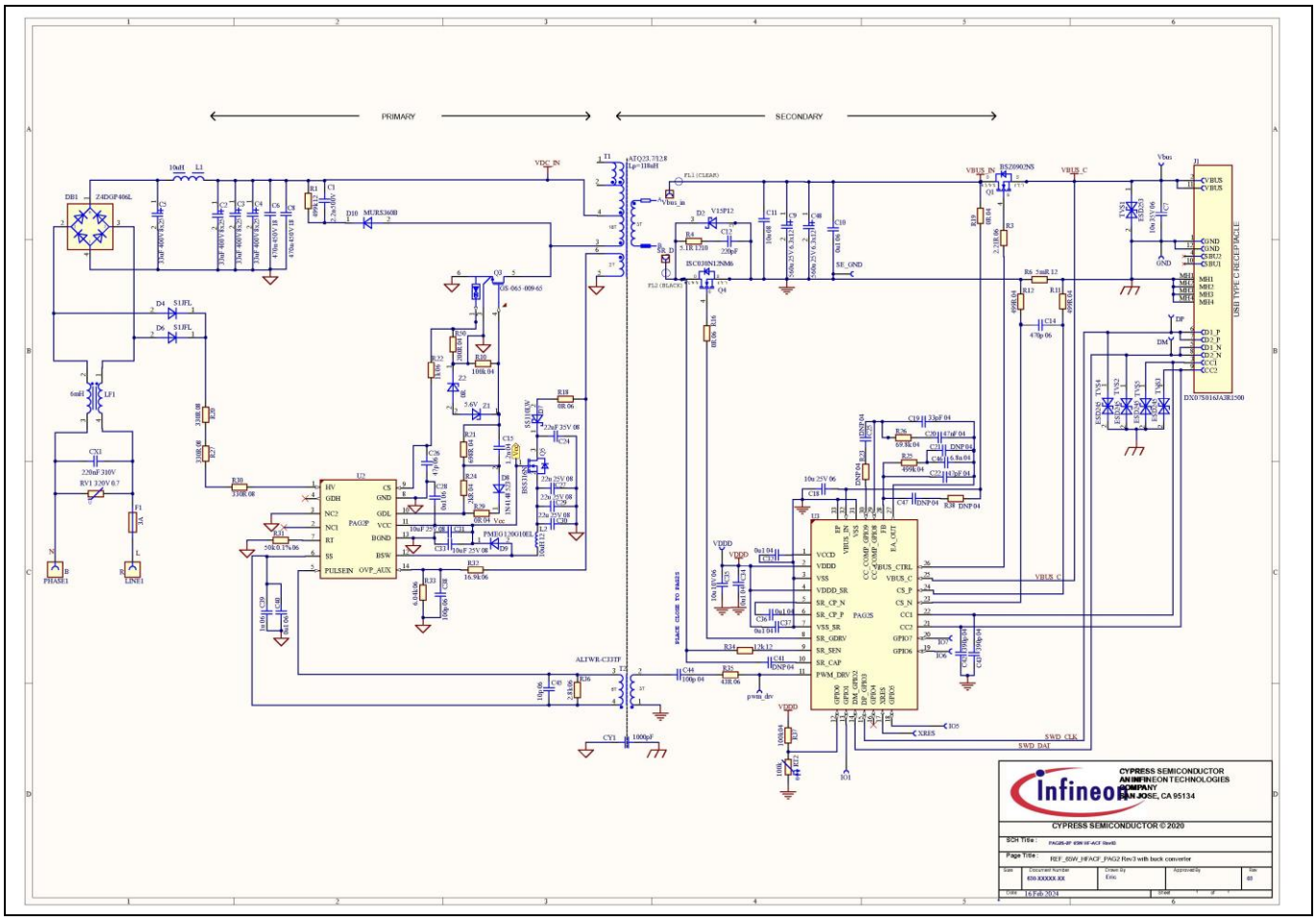


Figure 80 Schematic diagram of 65 W PAG2P_PAG2S_HF ZVS_Rev3_GaN system _SCH

5.2 Bill of materials (BOM)

Table 23 Bill of materials

Designator	Quantity	Comment	Value	Manufacturer order number	Manufacturer
C1	1	2200pF 500V	2200pF 500V	CC1206KKX7RBBB222	YAGEO
C2, C3, C4, C5	4	33uF 400V 8x25	33uF 400V 8x25	KCX 33u1F 400V 8X25	Rubycon
C6, C8	2	470n 450V 18	470n 450V 18	CGA8N4X7T2W474M230KA	TDK Corporation
C7	1	10u 35V 06	10u 35V 06	GRM188R6YA106MA73D	Murata
C9, C48	2	560u 25V 6.3x12	560u 25V 6.3x12	NPX 560uF 25V 6.3 x 12	Sh-ymin
C10	1	0u1 06	0u1 06	CGA3E2X8R1E104K080AA	TDK Corporation
C11	1	10u 08	10u 08	GRM21BR61H106KE43K	Murata
C12	1	220pF	220pF	1206B221K201CT	Walsin Technology
C14	1	470pF 06	470pF 06	GRM188R71H471KA01D	Murata
C15	1	1.2n 04	1.2n 04	GRM155R71H122JA01	Murata
C18	1	10u 25V 06	10u 25V 06	8.85012E+11	Würth Elektronik
C19	1	33pF 04	33pF 04	GRM1555C1E330GA01	Murata
C20	1	47nF 04	47nF 04	GRM155R61C473JA01	Murata
C22	1	4.7pF 04	4.7pF 04	GRM1555C1H4R7BA01D	Murata
C24	1	22uF 35V 08	22uF 35V 08	C2012X5R1V226M125AC	TDK
C26	1	47p 06	47p 06	GRM1885C1H470GA01	Murata
C27, C29, C30	3	22u 25V 08	22u 25V 08	GRM21BR61E226ME44	Murata
C28	1	0u1 06	0u1 06	06035C104JAT2A	AVX
C31, C33	2	10uF 25V 08	10uF 25V 08	GRM21BR61E106KA73	Murata
C32, C34	2	0u1 04	0u1 04	GRM152R61A104KE19	Murata
C35	1	10u 10V 06	10u 10V 06	ZRB18AD71A106KE01L	Murata
C36, C37	2	0u1 04	0u1 04	GCM155R71C104KA55	Murata
C38	1	100p 06	100p 06	06033A101JAT2A	AVX
C39	1	1u 06	1u 06	GRM185R61A105KE26	Murata
C40	1	0u1 06	0u1 06	C0603C104J8RAC	Kemet
C42, C43	2	390p 04	390p 04	GRM1555C1E391JA01	Murata
C44	1	100p 04	100p 04	GRM1555C1E101JA01	Murata

Appendix

Designator	Quantity	Comment	Value	Manufacturer order number	Manufacturer
C45	1	10p 06	10p 06	C0603C100K5GACAUTO	Kemet
C46	1	6.8n 04	6.8n 04	GRM155R71E682JA01	Murata
CX1	1	220nF 310V	220nF 310V	PX224K2C0702T	KYET
CY1	1	1000pF	1000pF	DE1E3RA102MN4AN01F	Murata
D2	1	V15P12	V15P12	V15P12-M3/H	Vishay
D8	1	1N4148 523	1N4148 523	1N4148WT-7	Diodes Incorporated
D4, D6	2	S1JFL	S1JFL	S1JFL	ON Semiconductor
D10	1	MURS360B	MURS360B	MURS360BT3G	ON Semiconductor
D7	1	SS110LW	SS110LW	SS110LW	Taiwan Semiconductor
D9	1	PMEG120G10EL	PMEG120G10EL	PMEG120G10ELRX	Nexperia
DB1	1	Z4DGP406L	Z4DGP406L	Z4DGP406L-HF	Comchip Technology
DM, DP, GND, IO1, IO5, IO6, IO7, pwm_drv, SE_GND, Vbus, VDDD, XRES	12	Test pad	Test pad	-	-
F1	1	3A	3A	TR1-2410TD3-R	Bussmann
J1	1	DX07S016JA3R1500	DX07S016JA3R1500	DX07S016JA3R1500	JAE
L1	1	10uH	10uH	74437346100	Würth Elektronik
L2	1	10uH 12	10uH 12	LSQCA322525T100KR	Taiyo Yuden
LF1	1	6mH	6mH	B64290L0044X038	EPCOS
LINE1	1	R	R	5000	Keystone Electronics Corp.
PHASE1	1	B	B	5001	Keystone Electronics Corp.
Q1	1	BSZ0902NS	BSZ0902NS	BSZ0902NS	Infineon Technologies
Q3	1	GS-065-009-65	GS-065-009-65	GS-065-009-65	Infineon Technologies

Appendix

Designator	Quantity	Comment	Value	Manufacturer order number	Manufacturer
Q4	1	ISC030N12NM6	ISC030N12NM6	ISC030N12NM6	Infineon Technologies
Q5	1	BSS316N	BSS316N	BSS316N H6327	Infineon Technologies
R1	1	499k 13	499k 13	ERJ-P08F4993V	Panasonic
R10	1	100k 04	100k 04	RC0402FR-07100KL	Yageo
R3	1	2.21R 06	2.21R 06	CRCW06032R21FK	Vishay
R4	1	5.1R 1210	5.1R 1210	ERJ-14YJ5R1U	Panasonic
R6	1	5mR 12	5mR 12	CSRF1206FT5L00	Stackpole Electronics
R11, R12	2	499R 04	499R 04	CRCW0402499RFK	Vishay
R24	1	2k 04	2k 04	CRCW04022K00FKEDC	Vishay
R16, R18	2	0R 06	0R 06	CRCW06030000Z0EA	Vishay
R29	1	0R 04	0R 04	RC0402JR-070RL	Yageo
R19	1	0R 04	0R 04	RC0402FR-070RL	Yageo
R20, R27, R30	3	330R 08	330R 08	CRCW0805330RFKEAHP	Vishay
R21	1	698R 04	698R 04	CRCW0402698RFKEDC	Vishay
R22	1	1k 06	1k 06	AC0603JR-071KL	Yageo
R25	1	499k 04	499k 04	CRCW0402499KFK	Vishay
R26	1	69.8k 04	69.8k 04	CRCW040269K8FK	Vishay
R31	1	50k 0.1% 06	50k 0.1% 06	RT0603BRD0750KL	Yageo
R32	1	16.9k 06	16.9k 06	CRCW060316K9FK	Vishay
R33	1	6.04k 06	6.04k 06	CRCW06036K04FK	Vishay
R34	1	12k 12	12k 12	CRCW120612K0FK	Vishay
R35	1	43R 06	43R 06	CRCW060343R0FK	Vishay
R36	1	2.8k 06	2.8k 06	MCR03EZPFX2801	ROHM Semiconductors
R37	1	100k 04	100k 04	CRCW0402100KFK	Vishay
R50	1	200R 04	200R 04	CRCW0402200RFK	Vishay
RT2	1	100k	100k	NCU18WF104J60RB	Murata
RV1	1	320V 0.7	320V 0.7	B72207S2321K101	Epcos
SR_D, Vbus_in	2	Test pad	Test pad	-	-
T1	1	ATQ23.7/12.8	ATQ23.7/12.8	ATQ23.7/12.8	Better Magnetic
T2	1	ALTWR-C33TF	ALTWR-C33TF	ALTWR-C33TF	Sunlord
TVS1	1	ESD253	ESD253	ESD253-B1-W0201	Infineon Technologies

Appendix

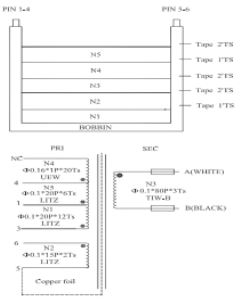
Designator	Quantity	Comment	Value	Manufacturer order number	Manufacturer
TVS2, TVS3, TVS4, TVS5	4	ESD245	ESD245	ESD245-B1-W0201	Infineon Technologies
U2	1	PAG2P	PAG2P	CYPAP212A1-14SXI	Infineon Technologies
U3	1	PAG2S	PAG2S	CYPAS212A1-32LQXQ	Infineon Technologies
Z1	1	5.6V	5.6V	DZ9F5V6S92	Diodes Incorporated
Z2	1	0R 04	0R 04	RC0402FR-070RL	Yageo

5.3 Transformer specification (T1)

PROPRIETARY

Outline Dimension and Winding Configuration

1. Schematic:

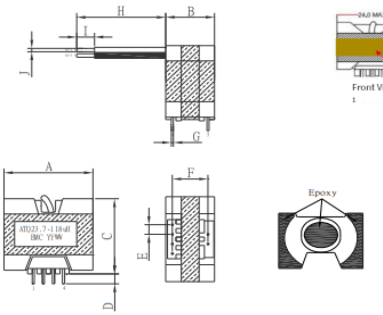


Note: 1. ● Winding start. ▭ Teflon tube

3.Electrical Characteristic

1. Inductance test : @100KHz/1.0V
   PIN(3-4)=118uH±5%
2. Leakage Inductance test : @100KHz/1.0V
   PIN(3-4)=5.0uH MAX Short others pin
3. DC Resistance @25℃
   PIN(3-4)=120mΩ MAX
   PIN(6-5)=20mΩ MAX
   PIN(WHT-BLK)=8mΩ MAX
4. Turns test '@20KHz/1.0V
   NP:PIN(3-4)=18T'S
   NS:PIN(6-5)=2T'S
   NS:PIN(WHT-BLK)=3T'S
4. Dielectric Strength
   PRI to SEC AC 3750V 50Hz/60Hz 5mA for 3 seconds
   PIN1.3.4.WHT,BLK to CORE AC 1000V 50Hz/60Hz 5mA for 3 seconds

2. Appearance size chart:



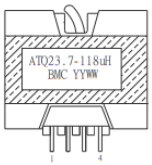
Sym.	Nom(mm)	±Tol.
A	26.5	MAX
B	14.5	MAX
C	22.5	MAX
D	3.5	0.5
E	2.9	0.5
F	10.0	0.5
G	0.6	0.1
H	25.0	2.0
I	5.0	2.0
I	3.0	MAX

Note: 1.Gap core connection dough epoxy resin （研磨铁芯结合面中柱点胶）（如上图）
2..Core is secured with tape 2T'S.（包2圈铁芯固定胶布）
3.Note : Add cross copper shields to the cores and ground to pin 5. Horizontal copper shield is 8mm width and vertical copper shield is 2mm.

Description			Issued Date	Page Nr.
			09/13/2023	2-1
Cust.Code-Part Nr.	Rev.	Engineering	Checked By	Approved By
ATQ23.7-118uH	0.0	BMC Engineering LiZhiEin	BMC Engineering HongChangLi	BMC Engineering ZiaoPingRong
Better Magnetics Nr.	BMC Rev.			
EF-239002	A			

Appendix

PROPRIETARY
Material List



All materials listed are in compliance with RoHS requirements

No.	Name	Description	Rating	Approval	Maker
1	Core	Ferrite core ATQ23.7/12.8/17.8 NH97 or equivalent			LIANFENG
2	Bobbin	Phenolic PM-9630 UL 94V-0	150℃	E41429	SUMITOMO
3	Wire	Polyurethane enamelled copper Wire UEW MW75-C Ø0.1*20P,Ø0.1*15P Ø0.16	130℃ 130℃	E339217 E201757	WEIHAN PACIFIC
		Triple insulated wire TIW-B Ø0.1X80P or equivalent	130℃	E357240	KAIZHONGHEDONG
4	Tape	Polyester tape #1350F-1 or #CT280	130℃ 130℃	E17385 E165111	3M YA HUA
5	Tube	CB-HFT ND-LL	125℃ 200℃	E180908 E350651	CHANGYUAN NANDIAN
6	Copper foil	0.05(T)*8mm 0.05(T)*3mm			HAIYU DETAI
7	Epoxy	2050 2041			CHENGGE CHENGGE
8	Varnish	BC-359 WP-2952F-2G(Y)	180℃ 130℃	E317427 E72979	DOLPH HITACHI

Description			Issued Date	Page Nr.
Note: denotes the material used for the sample			09/13/2023	2-2
Cust.Code-Part Nr.	Rev.	Engineering	Checked By	Approved By
ATQ23.7-118uH	0.0			
Better Magnetics Nr.	BMC Rev.			
EF-239002	A			

Figure 81 ATQ23.7-118uH (NH97)

5.4 Inductor specification (L1)

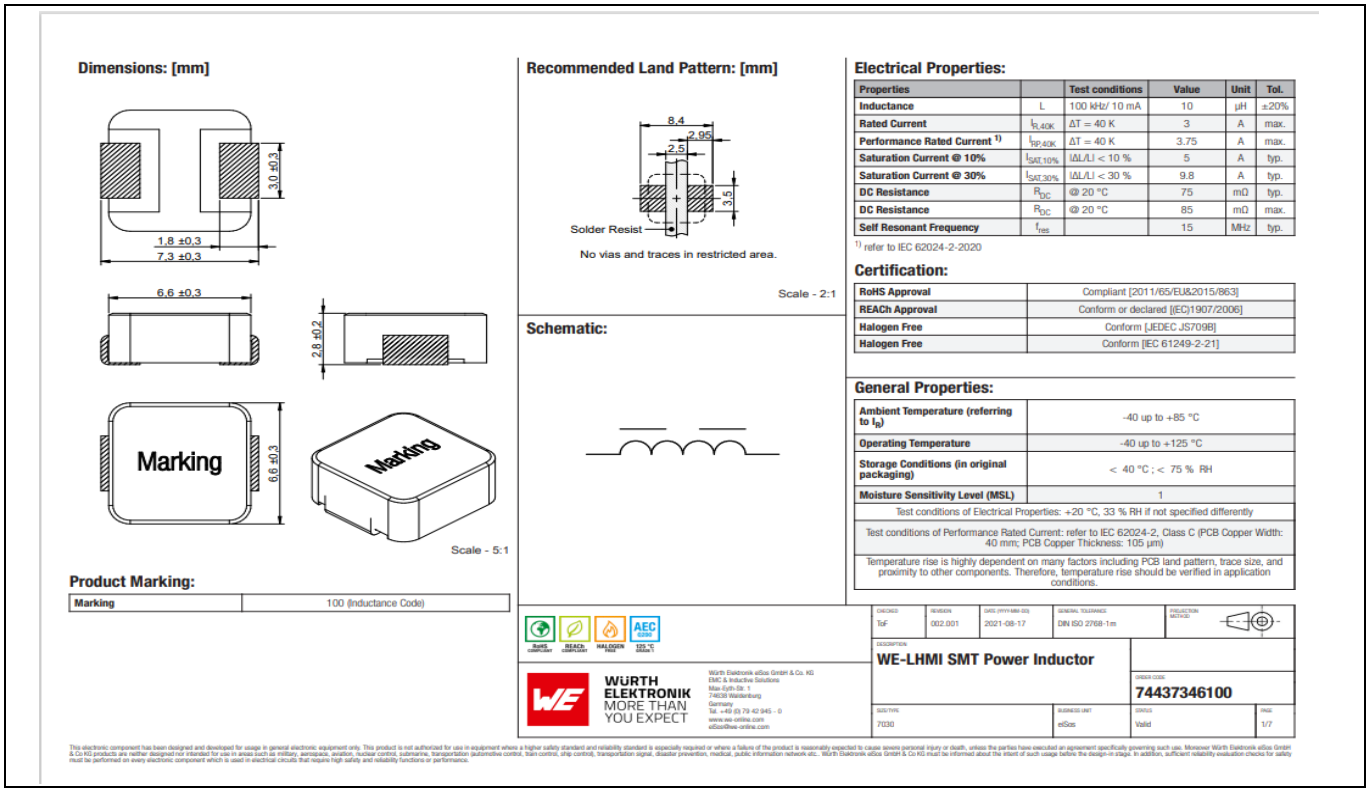


Figure 82 FIXED IND 10UH 3A 85 MOHM SMD Würth Elektronik

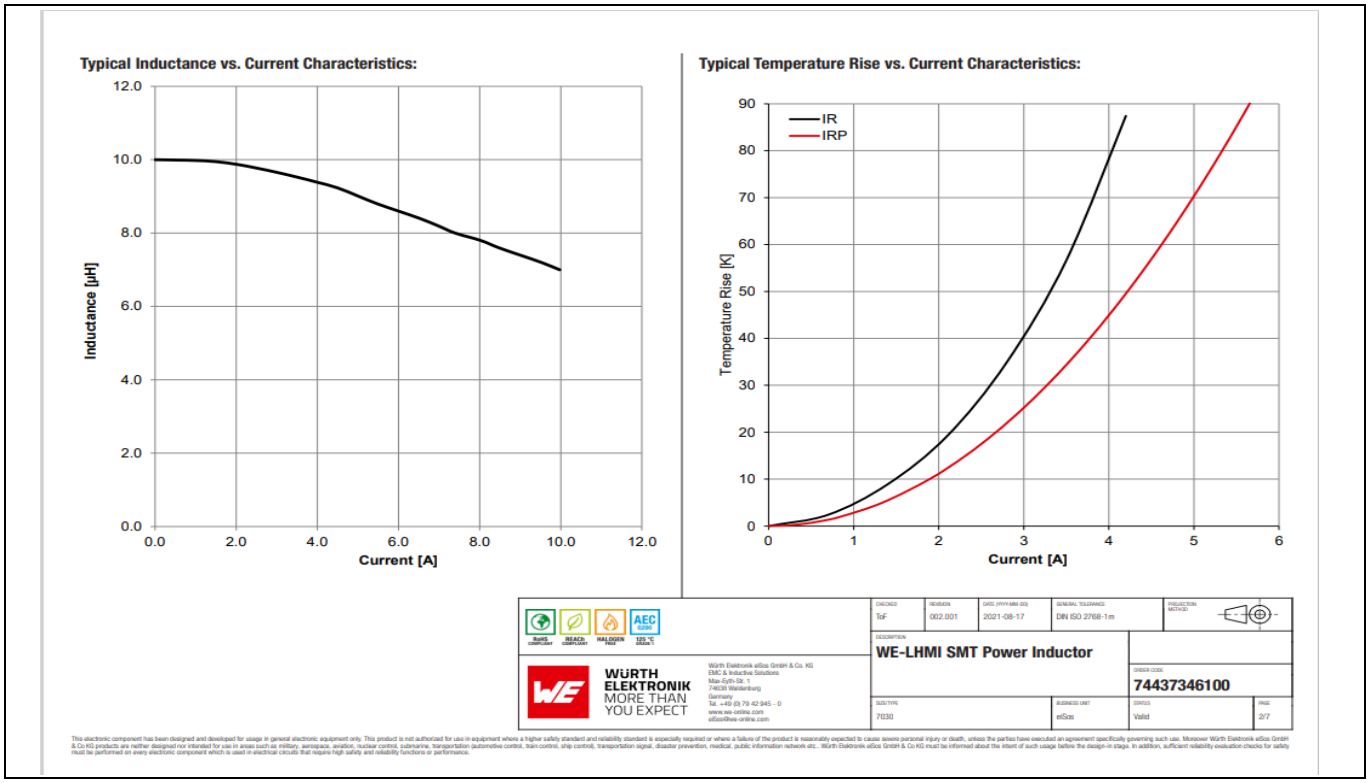


Figure 83 L1 FIXED IND 10UH 3A 85 MOHM SMD Würth Elektronik inductor specifications

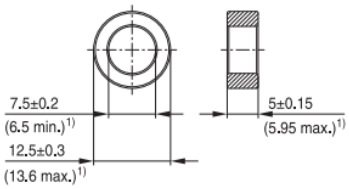
5.5 Common mode choke specification (LF2)

TDK

R 12.5 × 7.50 × 5.00 **B64290L0044**

■ Epoxy coating

R 12.5 × 7.50 × 5.00 (mm)
R 0.492 × 0.295 × 0.197 (inch)



1) With coating FUS0230-T-E

Dimensions

d_a (mm)	d_i (mm)	Height (mm)	d_a (inch)	d_i (inch)	Height (inch)	
12.5 ±0.3	7.5 ±0.2	5.00 ±0.15	0.492 ±0.012	0.295 ±0.008	0.197 ±0.005	uncoated 1)
13.6 max.	6.5 min.	5.95 max.	0.535 max.	0.256 min.	0.234 max.	coated

Characteristics and ordering codes

Material	A_L value nH	μ_i (approx.)	Ordering code	Magnetic characteristics				Approx. weight g
				$\Sigma l/A$ mm^{-1}	l_e mm	A_e mm^2	V_e mm^3	
N49	660 ±25%	1300	B64290L0044X049	2.46	30.09	12.23	368	1.8
N87	1120 ±25%	2200	B64290L0044X087					
N30	2200 ±25%	4300	B64290L0044X830					
T65	2400 ±30%	4700	B64290L0044X065					
T35	3060 ±25%	6000	B64290L0044X035					
T37	3320 ±25%	6500	B64290L0044X037					
T38	5110 ±30%	10000	B64290L0044X038					

Figure 84 Common mode chock specification

Remarks: Material: T38, Turns:30, L=4.6 mH, R_{dc}=66 mohm

5.6 Pulse transformer specification (T2)

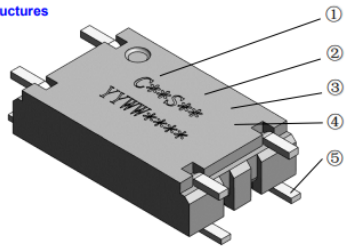
Sunlord www.sunlordinc.com

Proposal Of Pulse Transformer For Automobiles(ALTWR-C33TF)

Issued By	Checked By	Prepared By
Xiangping Qu	Xiangping Qu	Liangming Bin
2023/1/16	2023/1/16	2023/1/16

Note: This is a preliminary proposal for communication.The product reliability is being test,and the final product P/N, Structure, Shape and Dimensions, Electrical Characteristics may be changed. You are requested to confirm and approve our spec.

1.Structures

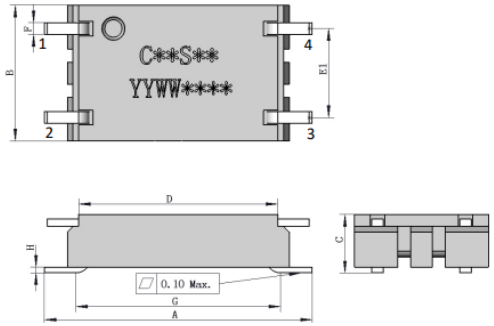


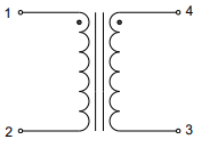
No.	Part Name	Material
①	Case	Plastics
②	Glue	Silicon Glue
③	Core	Ferrite soft magnetism
④	Wire	Polyurethane system enameled copper wire
⑤	Terminal	Cu+Ni+Sn plating

2.Shape and dimensions (mm)

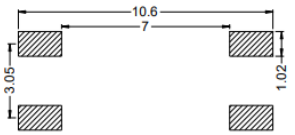
Unit:mm

Items	A	B	C	D Ref.	E1	F	G Ref.	H Ref.
Sunlord Design	9.3±0.30	4.90 Max.	2.00+0.20/ -0.10	6.9±0.50	3.05±0.13	0.50±0.13	7.10	0.25





Topological diagram

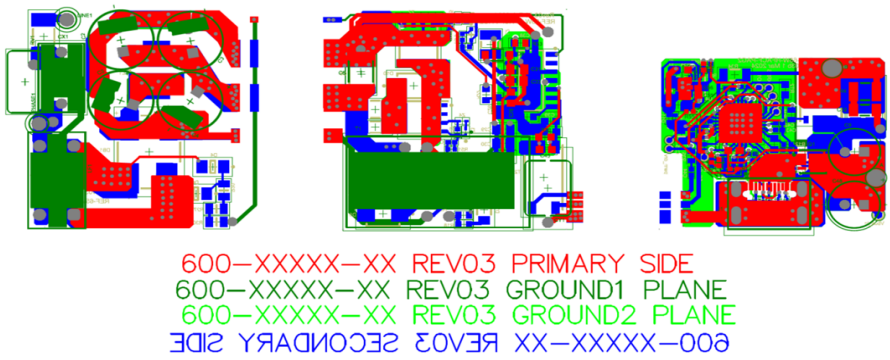


Recommend pad patterm (mm)

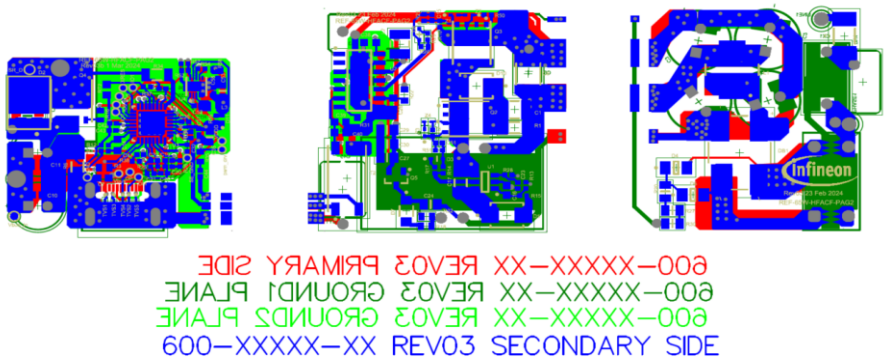
Shenzhen Sunlord Electronics Co.,Ltd. Page1/2

Figure 85 Pulse transformer specification

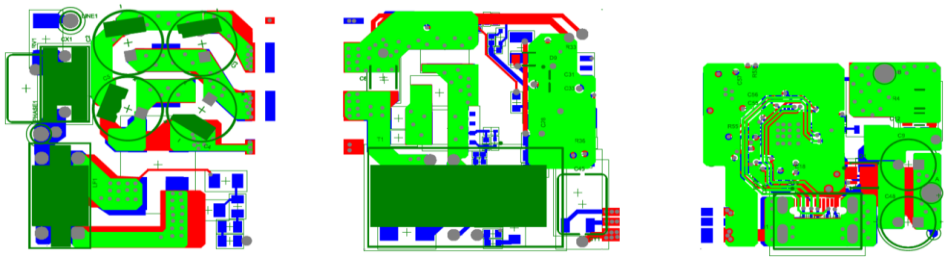
5.7 PCB layout



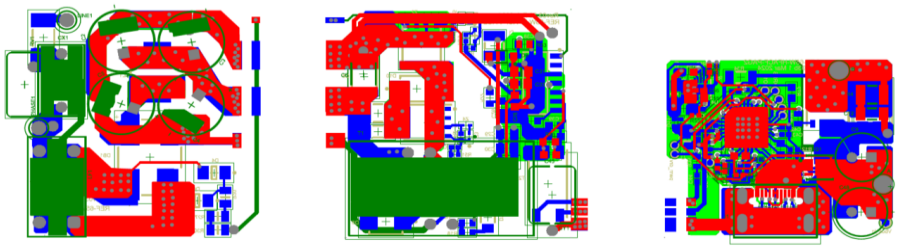
TOP SIDE COPPER- LAYER 1



BOTTOM SOLDER COPPER – LAYER 4



INNER LAYER – LAYER 2



INNER LAYER – LAYER 3

Figure 87 PCB layout

5.8 EZ-PD™ Configuration Utility

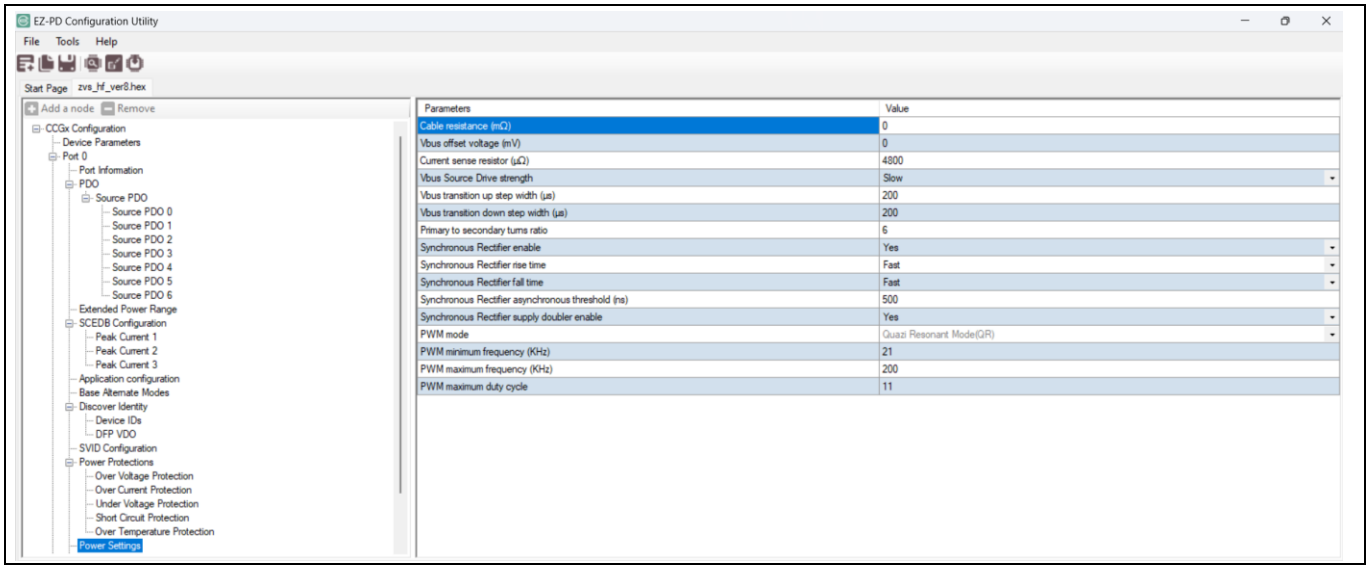


Figure 88 EZ-PD™ Configuration Utility

The Infineon's EZ-PD™ PAG2S controller is a highly configurable and programmable solution. The chip can be configured using parameters stored in the internal flash memory. These parameters are to be chosen and programmed by Infineon customers according to their use cases and requirements.

The Graphical User Interface (GUI) of EZ-PD™ Configuration Utility allows users to intuitively select and configure the parameters for their application.

Here is the default configured values with respect to Power Settings and Power Protections.

Table 24 Default configuration values

Parameters	Values
Power Settings	
Cable resistance (mΩ)	0
Vbus offset voltage (mV)	0
Current sense resistor (µΩ)	4800
Vbus source drive strength	Slow
Vbus transition up step width (µs)	200
Vbus transition down step width (µs)	200
Primary to secondary turns ratio	6
Synchronous rectifier enable	Yes
Synchronous rectifier rise time	Fast
Synchronous rectifier fall time	Fast
Synchronous rectifier async threshold (ns)	500
Synchronous rectifier doubler enable	Yes
PWM mode	Quasi Resonant Mode (QR)
PWM minimum frequency (kHz)	21
PWM maximum frequency (kHz)	200

Appendix

Parameters	Values
PWM maximum duty cycle at minimum frequency (%)	11
Power protections	
Overvoltage protection	
Enable	Yes
OVP threshold (%)	20
Debounce period (µs)	10
Retry count	2
Overcurrent protection	
Enable	Yes
OCP threshold (%)	20
Debounce period (ms)	10
Retry count	2
Undervoltage protection	
Enable	Yes
UVP threshold (%)	70
Debounce period (µs)	10
Retry count	2
Short-circuit protection	
Enable	Yes
SCP threshold (%)	40
Debounce period (µs)	2
Retry count	2
Over temperature protection	
Enable	Yes
Thermistor type 1	NTC
Cut-off value 1	255
Restart value 1	909
Debounce period(ms)	10
Enable Thermistor 2	Yes
Thermistor type 2	NTC
Cut-off value 2	255
Restart value 2	909

Acronyms

Table 25 Acronyms

Abbreviation	Definition
CC-CV	Constant current - constant voltage
CE	Conducted emission
CH'x'	Oscilloscope channel numbers
CR Mode	Constant resistance mode in electronic load
DCM	Discontinuous current mode
DP/DM	USB data positive/data negative lines
DUT/EUT	Device under test/equipment under test
FET	MOSFET (Metal Oxide Semiconductor Field Effect Transistor)
GUI	Graphical User Interface
HF	High frequency
Io/I_{OUT}	Output current of the DUT
NGDO	NFET gate driver output
OCP	Overcurrent protection
OVP	Overvoltage protection
P-P	Peak-to-peak
PAT	Power adapter tester
PDO	Power Delivery output
PPS	Programmable power supply
SCP	Short-circuit protection
USB PD	Universal Serial Bus Power Delivery
V_{BUS_C}/V_{OUT}	Output voltage of the DUT
V_{AC}/V_{IN_AC}	Input DC voltage to the DUT
ZVS	Zero voltage switching

References

[1] USB Implementers Forum, Inc.: *Document library;* Available online

[2] USB Implementers Forum, Inc.: *USB Type-C and connector specification (Release 2.2)*; Available online

[3] Infineon Technologies AG: *EZ-PD™ Configuration Utility*; Available online

[4] Infineon Technologies AG: *EZ-PD™ PAG2S-QZ integrated USB PD and secondary-side QR-ZVS CONTROLLER* (Document Number: 002-37216 Rev. *C), 2023-12-21; Available online

[5] Infineon Technologies AG: *EZ-PD™ PAG2P primary-side start-up controller* (Document Number: 002-34772 Rev. *F), 2022-06-13; Available online

Revision history

Document revision	Date	Description of changes
**	2024-10-18	Initial release
*A	2024-10-28	Updated title

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-10-28
Published by

Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email:
erratum@infineon.com

Document reference
002-40639 Rev. *A

Important notice
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”).

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.