Title - ZU111 Validation Plan/Procedure/Analysis

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Introduction

This document is used to record the power supply programming, bringup, and validation for Xilinx ZU111 platform. This document applies to Rev A hardware only.

Documents

The following documents are used for this validation plan.

Table 1 – Document and File Description

Originator	Title	Description
Xilinx	HW-Z1-ZCU111_11272017_PM	Schematic
Xilinx	ZCU111_REVA_Patches	Rev A PCB Rework
Xilinx	70_ZCU111.brd	Layout
Infineon	IRPS5401MXI04TRP_MTPplus5_0.85V_1.8V_0.85V_800k_Rev2_2.txt	U53 Configuration
Infineon	IRPS5401MXI04TRP_MTPplus6_3.3V_2.5V_1.2V__0.85V_800k_Rev2_2.txt	U55 Configuration
Infineon	IRPS5401MXI04TRP_MTPplus7_1.2V_2.5V_1.8V_1.8V_800k_Rev2_2.txt	U57 Configuration
Xilinx	ZCU111_REVA_Powerup	Power Up Instructions

Test Equipment

The following is the test equipment used for validation purposes.

Table 2 – Test Equipment

Item	Manufacturer	Function	Model/Description
1	LTE	Power Supply	
2	Fluke	DMM	179
3	Agilent	DMM	34401A
4	Tek	Oscilloscope	TDS5104B
5	Tek	Differential Probe	P6247
6	Tek	Passive Probe	P6139A
7	N/A	Coax Probe	
8	Infineon	Comms	USB005
9	Infineon	GUI	Power Center
10	Chroma	Electronic Load	

DC/DC Converter Overview

The below reference designators are the voltage regulators designed onto the ZU111 hardware and tested as part of the validation plan/procedure. The voltage rails associated with each are listed. Note there are multiple ref des associated with a few voltage rails due to the use of power stages.

Table 3 - Ref Des Description

Ref Des	Manufacturer	Schematic Page	Voltage Rail
U53	Infineon	47	VCCINT_IO_BRAM_PS_SDFEC
			VCC1V8
			VCCINT_AMS
U54	Infineon	48	*VCCINT_IO_BRAM_PS_SDFEC (power stage)
U55	Infineon	49	UTIL_3V3
			UTIL_2V5
			MGT1V2
			MGTRAVCC
U56	Infineon	50	*UTIL_3V3 (power stage)
U57	Infineon	51	VCC1V2
			DAC_AVTT
			VADJ_FMC
			MGT1V8
U58		52	* VCC1V2 (power stage)
U68	Infineon	54	VCCINT
U70	Infineon	55	MGTAVCC
U72	Infineon	56	DAC_AVCCAUX
U74	Infineon	57	ADC_AVCCAUX
U75	Infineon	58	UTIL_1V13
U76	Infineon	59	UTIL_5V0
U101	Intersil	60	ADC_AVCC
U78	Intersil	60	DAC_AVCC
U81	Infineon	61	PL_DDR_VTT
U82	Infineon	61	PS_DDR_VTT
U62	Infineon	71	UTIL_3V5
U100	Intersil	71	AMS_CLK_VCC3V3

Programming

The programming procedure assumes a board populated with an IRPS5401, U53, U55, and U57, has parts pre-programmed. All others have no pre-programmed configuration in the NVM where applicable.

Please confirm all REVA_PATCHES are complete.

DCDC Converter Validation Results

The following sections document the DCDC converters with respect to the following test conditions and measurements.

1. DC Voltage
    a. All DC measurements are recorded by use of a true RMS DMM to ensure accuracy and validation with the GUI reported results.
2. DC Ripple (Steady-State)
    a. DC ripple is measured with a differential active probe or an analog coax probe (ac coupled) where precision noise floor measurements are required. Note o-scope offsets are in effect and absolute DC reference point must be measured by the DMM and are recorded as the DC voltage. Noise floor for active differential probes typically limit to 10mVpp. Noise floor for coax probes typically limit to just under 5mVpp.
3. ac transient response (Large Signal Analysis)
    a. All ac transient measurements are measured with respect to the valley/valley or peak/peak for loading and releasing events respectively. Note 0-scope offsets are in effect and absolute DC reference point must be measured by the DMM and are recorded as the DC voltage.
4. Current Sense Accuracy
    a. Where telemetry is available, the calibrated E-load is used to verify the telemetry reporting accuracy.
5. Protection (OCP)
    a. Where the programmability occurs, magnetic ratings on Isat allow, and test access allows, OCP protections are checked for accurate triggering. In some instances, the OCP rating may be artificially adjusted to check the operation of OCP but may not be the final programmed rating due to other HW limitations.
6. Sequence Timing

Acceptance test parameters are as follows:

1. DC Ripple (updated per inputs 1/26/18)
    a. ADC_AVCC [STE required]
        i. 0.25mV,pp (0.12mV,pp original spec)
    b. DAC_AVCC [STE required]
        i. 0.40mV,pp (0.2mV,pp original spec)
    c. ADC_AVCCAUX
        i. 11.03mV,pp (5.51mV,pp original spec)
    d. DAC_AVCCAUX [STE required]
        i. 2.00mV,pp (1.0mV,pp original spec)
    e. DAC_AVTT
        i. 8.94mV,pp (4.47mV,pp original spec)
    f. VCCINT_AMS
        i. 20mV,pp (10mV,pp original spec)
    g. MGTAVCC, MGTRAVCC, MGT1V2, MGT1V8

        i. 12mV,pp ~~10mV,pp~~
    h. VCCINT_IO_BRAM_PS_SDFEC (VCCPSINT)
        i. 2%, 17mV,pp
    i. VCC1V8
        i. 2%, 36mV,pp
    j. Others
        i. Combined within overall specification
2. Vac Transient
    a. ADC_AVCC (23.13mV), DAC_AVCC (23.13mV), DAC_AVCCAUX
        i. 2.5% @ 25% step, 1A/us
    b. VCCINT_AMS (21.25mV), VCCINT (21.25mV)
        i. 2.5% @ 25% step (6A given in last email for AMS), 2A/us
    c. UTIL3V5 (87.5mV), AMS_CLK_VCC3V3 (82.5mV)
        i. ±2.5% @ 50% step, 1A/us
    d. DAC_AVTT (62.5mV), ADC_AVCCAUX (45mV), VCC1V8 (45mV), UTIL1V13 (28.25mV), MGT1V8 (45mV)
        i. ±2.5% @ 100% step, 1A/us
    e. MGTRAVCC (21.25mV)
        i. ±2.5% @ 50% step, 1A/us
    f. MGT1V2 (30mV)
        i. ±2.5% @ 2.5A step, 1A/us
    g. VCC1V2 (30mV)
        i. ±2.5% @ 3.0A step, 1A/us
    h. MGTAVCC (22.5mV)
        i. ±2.5% @ 1.5A step, 1A/us
    i. FMC_VADJ (45mV)
        i. ±2.5% @ 0.7A step (test to 2A), 1A/us
            1. Connector requires 4A load ability on VADJ_FMC_BUS (before shunt)
    j. VCCINT_IO_BRAM_PS_SDFEC (VCCPSINT)
        i. ±2.5% (21.25mV) @ 8A step (2A to 10A), 2.5A/us
    k. UTIL1V13 (56.5mV)
        i. ±5.0% @ 100% step (step size unknown), 1A/us
    l. UTIL3V3 (165mV), UTIL2V5 (125mV)
        i. ±5% @ 50% step, 1A/us
    m. UTIL5V0 (250mV)
        i. ±5% @ 900mA step (1.8A to 2.7A), 1A/us
    n. PL_DDR4_VTT (30mV), PS_DDR4_VTT (30mV)
        i. ±5% @ 40% step, 1A/us
3. OCP
    a. Where circuit allows, ensure OCP meets design
    b. Else, ensure ample margin to prevent for false OCP
4. Sequencing

a. POR (power on reset) guidelines met

Design Change Recommendations

Any design change recommendations are embedded within the subsections to follow and are denoted in **RED**.

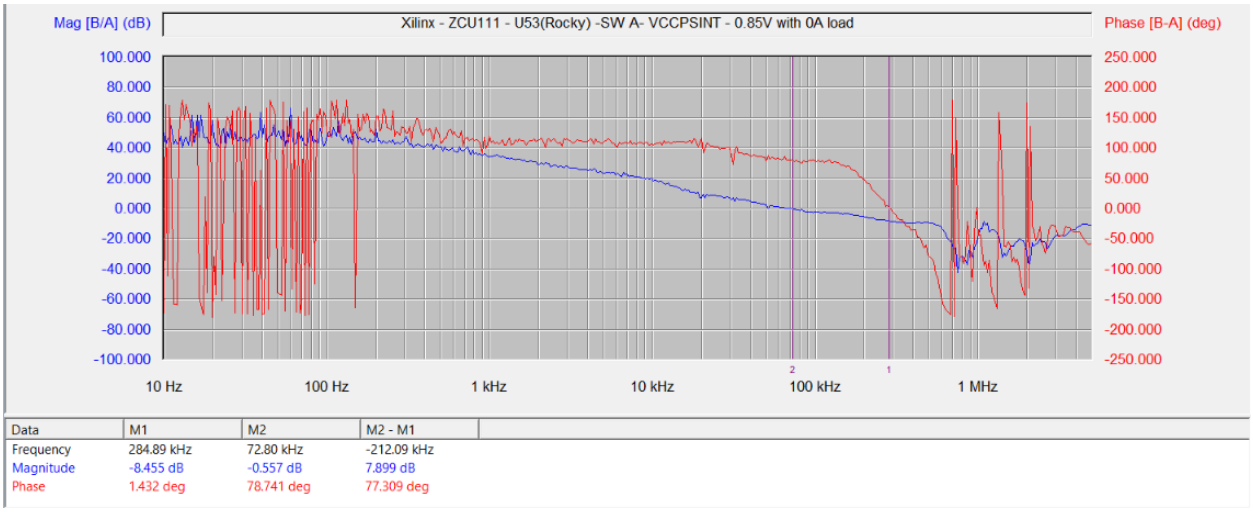
VCCINT_IO_BRAM_PS_SDFEC

Vin, 12V
Vout, 0.85V
Iout(pk), 15A
Istep, 8A (2A to 10A)
Iramp, 2.5A/us

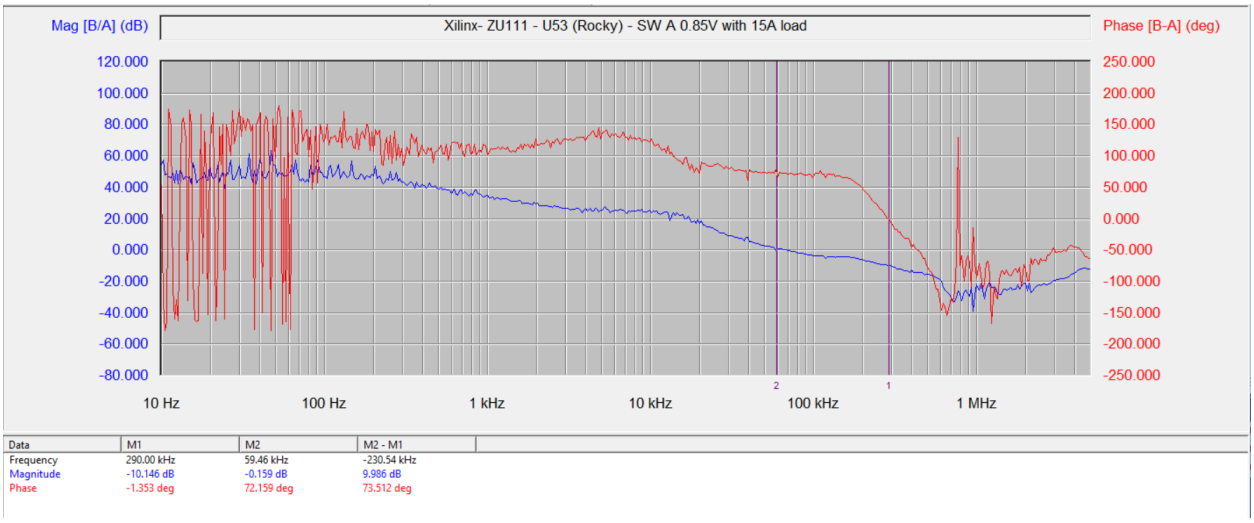
Vout Measurement Location, J46, C946
Load Test Location, J46
SW Node Measurement Location, L22

Jitter = 47ns (10A load)

Bode Analysis



At 0A load, Crossover Frequency is 72kHz with Phase Margin = 78deg and Gain Margin ~ -10dB



With 15A load, the crossover frequency is 59.5kHz with Phase Margin = 72 deg and Gain Margin = -10dB

Config: IRPS5401MXI04TRP_MTPplus5_0.85V_1.8V_0.85V_800k_Rev2_2.txt

Table 4 – VCCINT_IO_BRAM_PS_SDFEC Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.846V	Pass	0A 15A	DMM
DC Ripple	15.6mV 14.4mV	Pass	0A 15A	active probe across SP-Cap. Lower ripple at BGA pads.
Isense	0.38A 5.50A 10.38A 15.00A	Pass	0A 5A 10A 15A	Telemetry/E-load
Vac(droop)	5.4mV	Pass	2A to 10A	
Vac(overshoot)	9.4mV	Pass	10A to 2A	

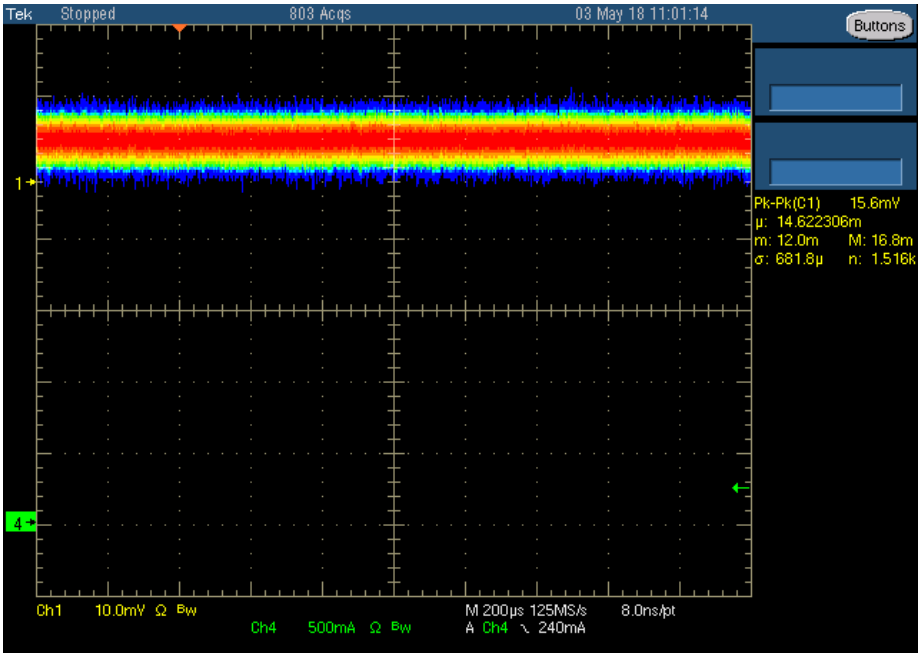


Figure 1 - VCCINT_IO_BRAM_PS_SDFEC DC Ripple, 0A

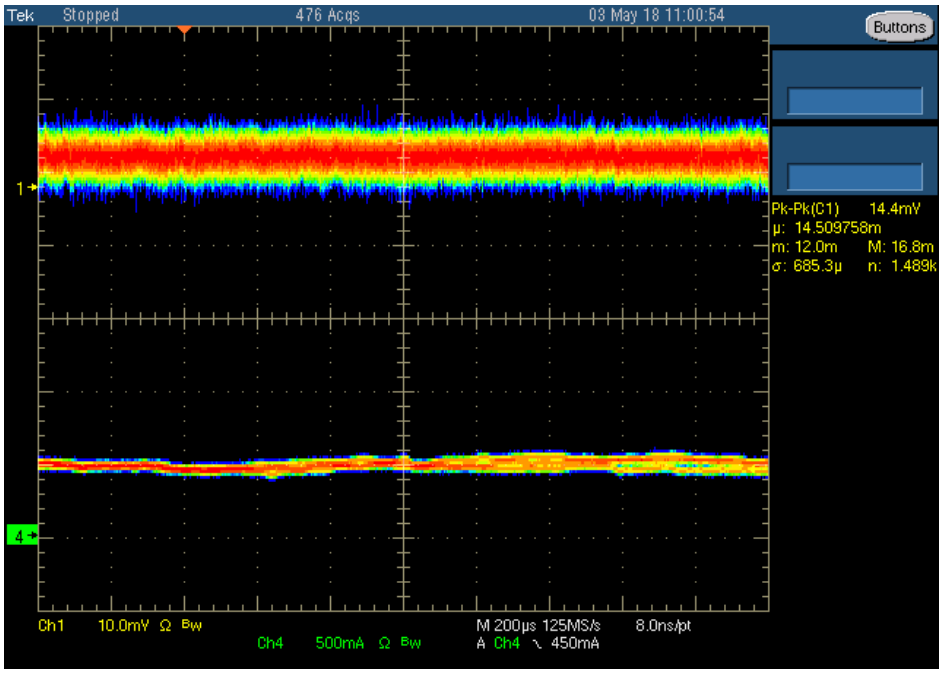


Figure - VCCINT_IO_BRAM_PS_SDFEC DC Ripple, 15A

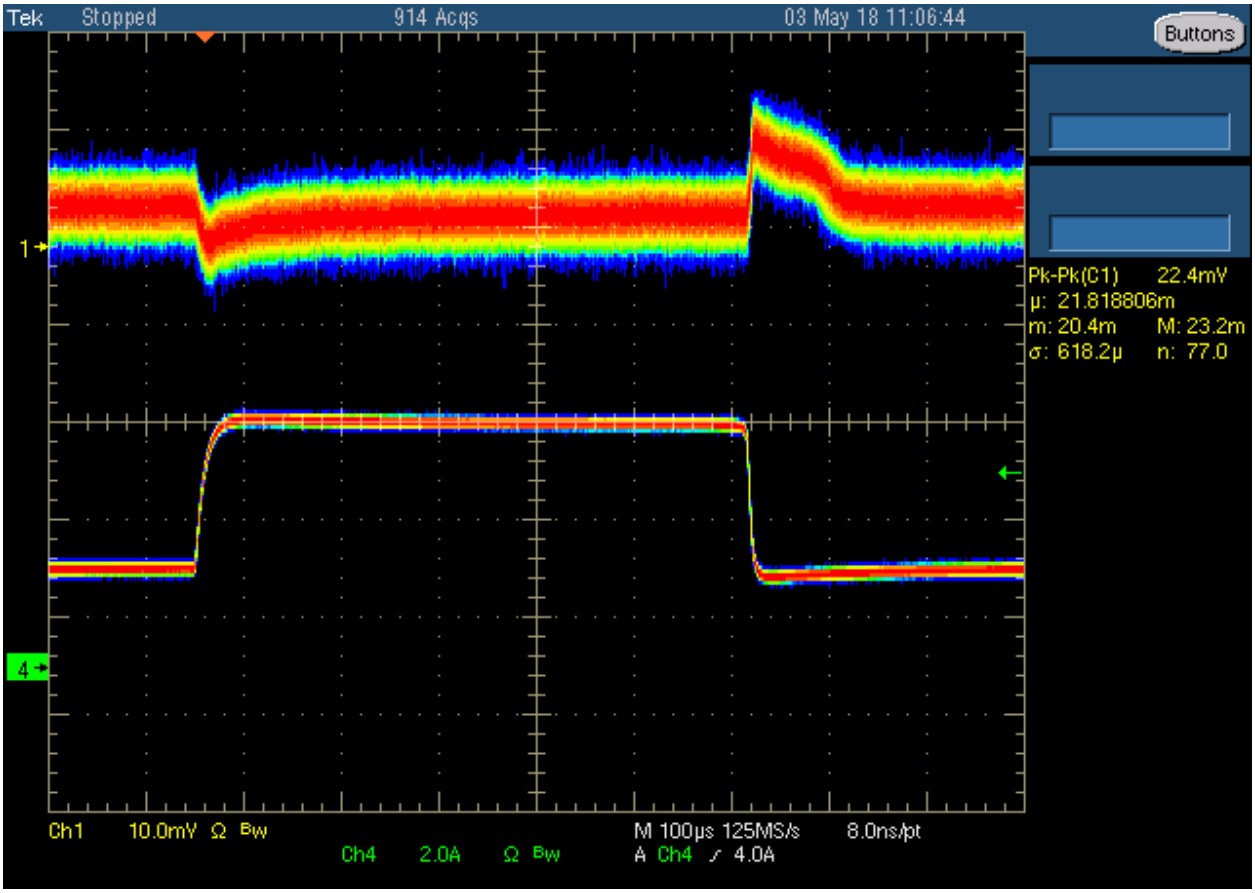


Figure 2 - VCCINT_IO_BRAM_PS_SDFEC Transient Load : 2-10A

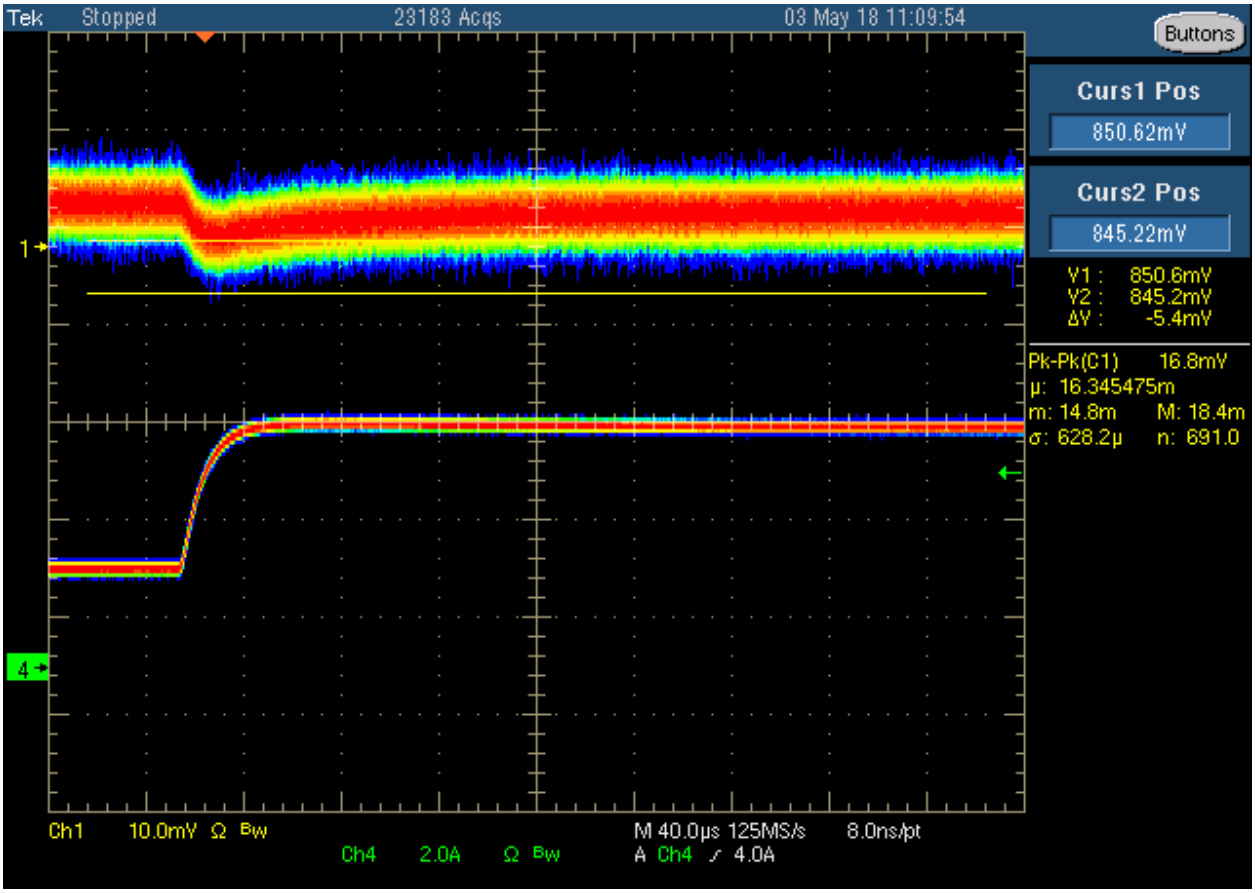


Figure – During 2-10A load step, the Vout excursion is around 5.4mV

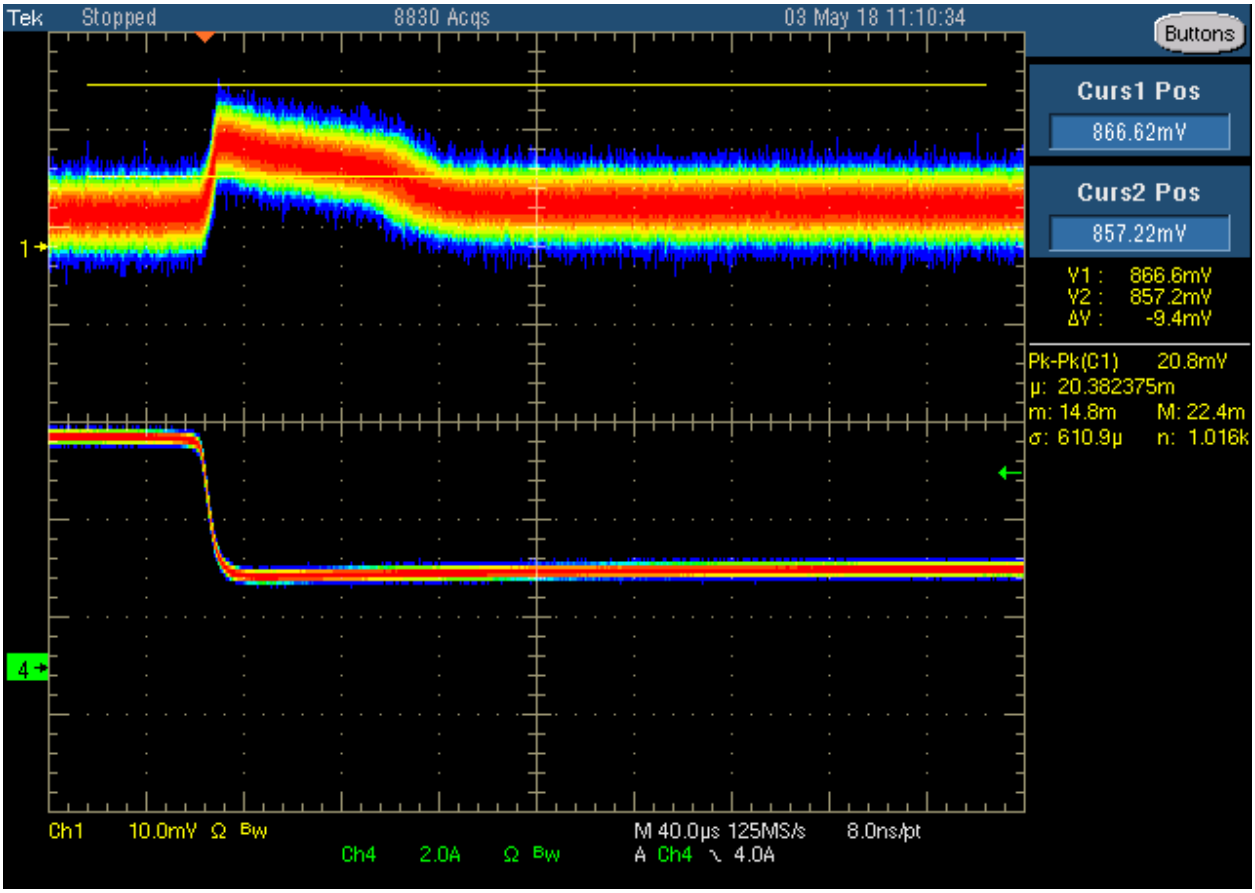


Figure 3 - VCCINT_IO_BRAM_PS_SDFEC during the 10A – 2A load release, Vout overshoot is around 9.4mV

VCC1V8

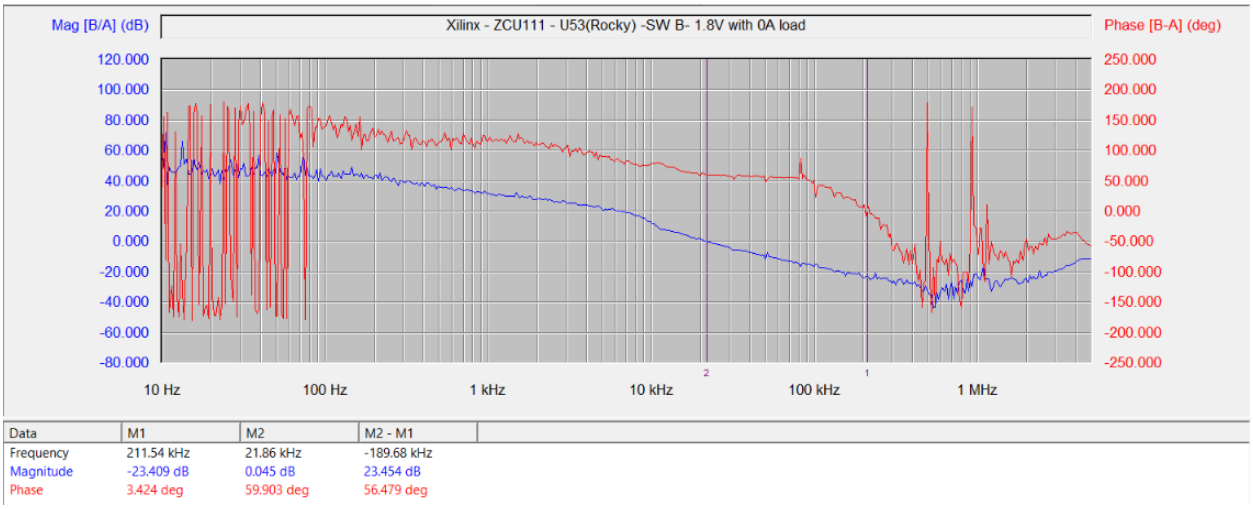
Vin, 12V
Vout, 1.8V
Iout(pk), 2A
Istep, 2A
Iramp, 1A/us

Vout Measurement Location, J61, L38, C110
Load Test Location, J61
SW Node Measurement Location, L19

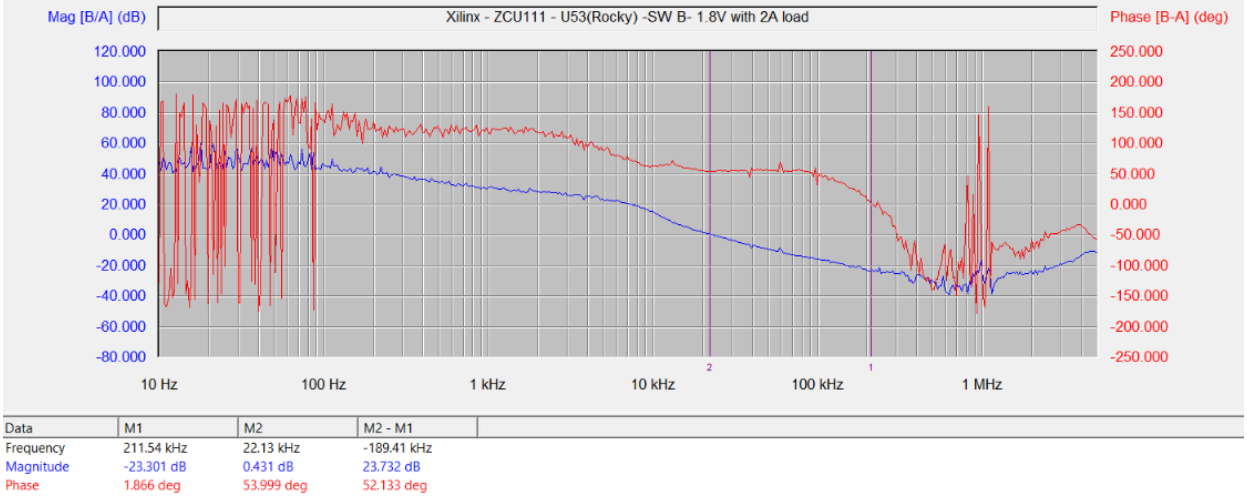
Jitter = 28.8ns (2A load)

Config: IRPS5401MXI04TRP_MTPplus5_0.85V_1.8V_0.85V_800k_Rev2_2.txt

Bode Analysis



At 0 A Load, crossover frequency is 21.86kHz with Phase Margin at 60deg and Gain Margin of -23dB



At 2A load, crossover frequency of 22.13kHz with Phase Margin of 54 deg and Gain Margin of -23dB

Table 5 – VCC1V8 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.8V	Pass	0A 2A	DMM
DC Ripple	13.0mV 13.2mV	Pass	0A 2A	Active probe
Isense	0.38A 2.34A	Pass	0A 2A	Telemetry/E-load
Vac(droop)	36.0mV	Pass	0A to 2A	
Vac(overshoot)	32.8mV	Pass	2A to 0A	

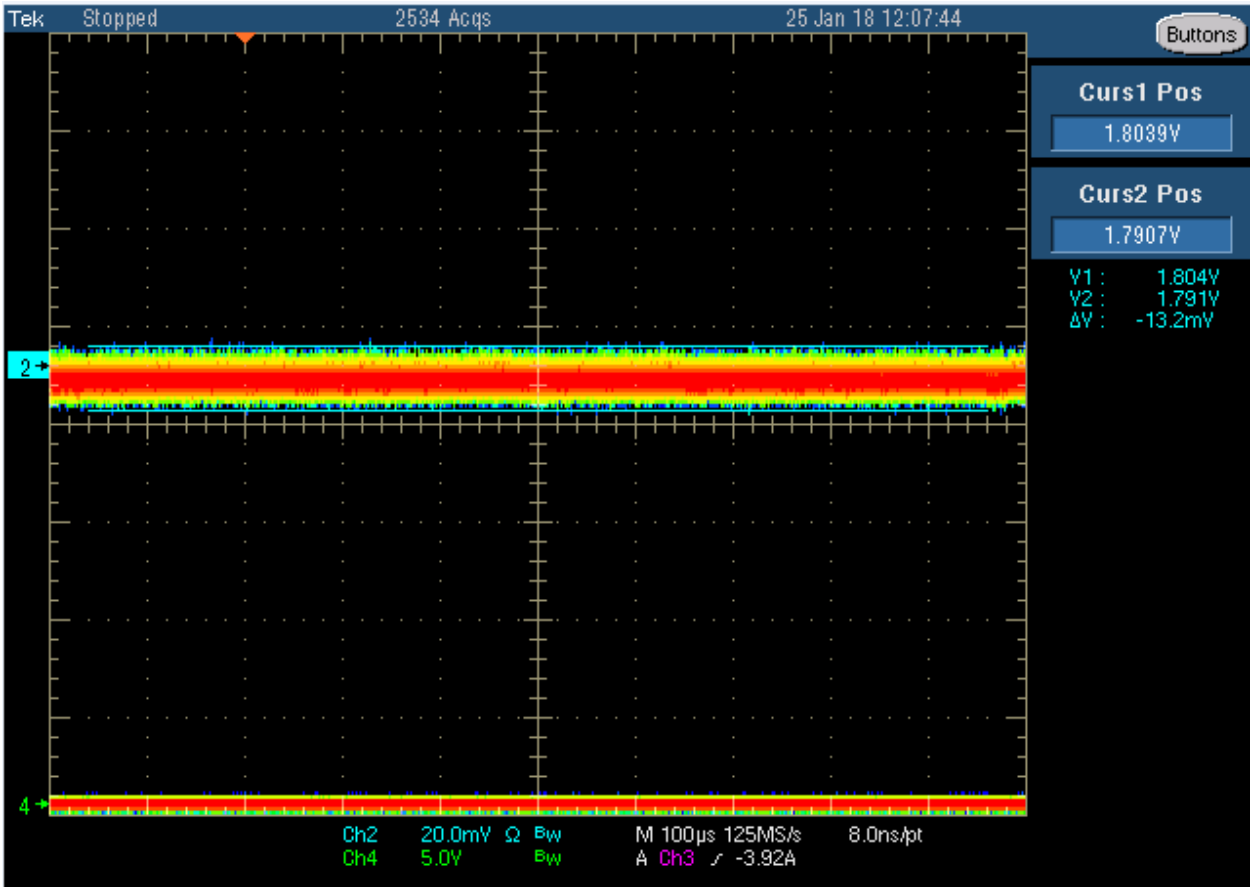


Figure 4 - VCC1V8 DC Ripple, 2A

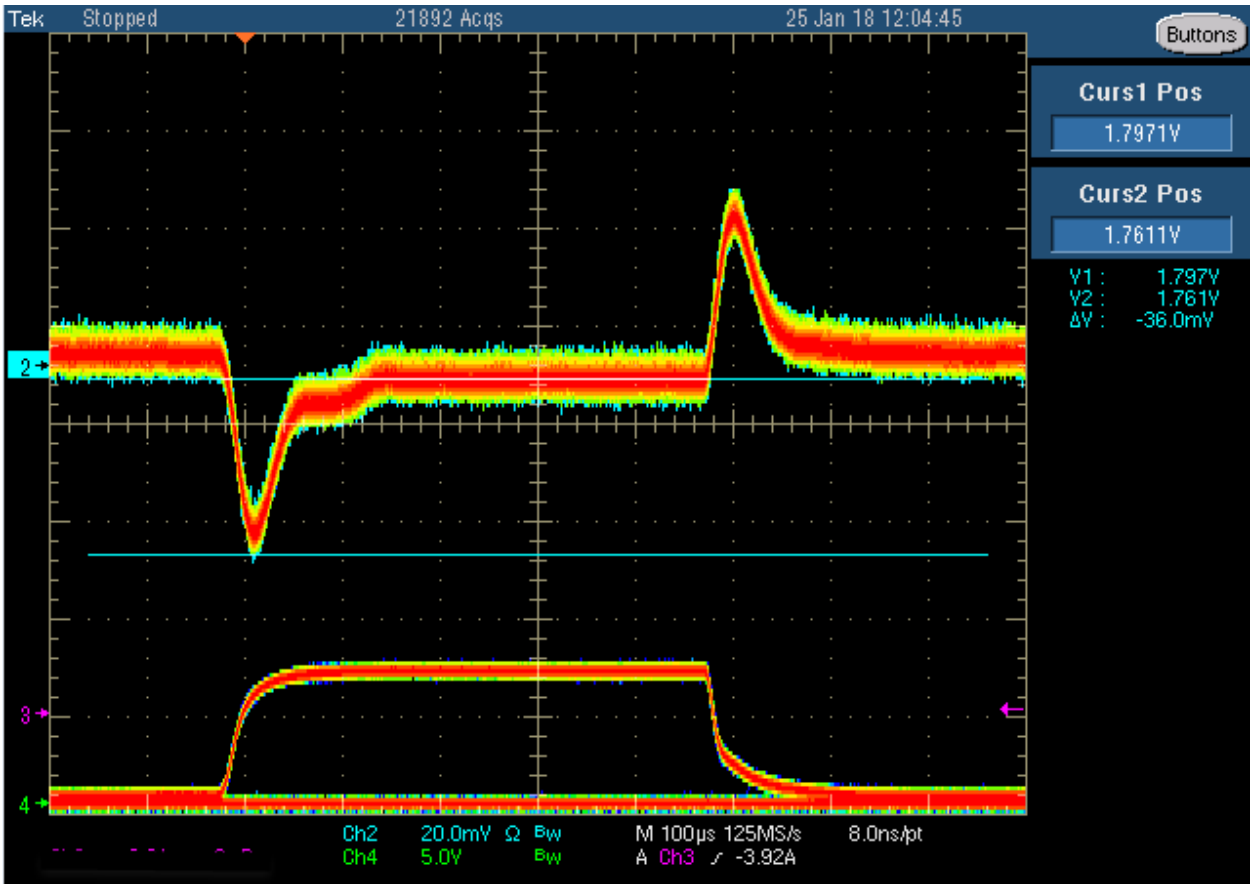


Figure 5 - VCC1V8 ac ripple load

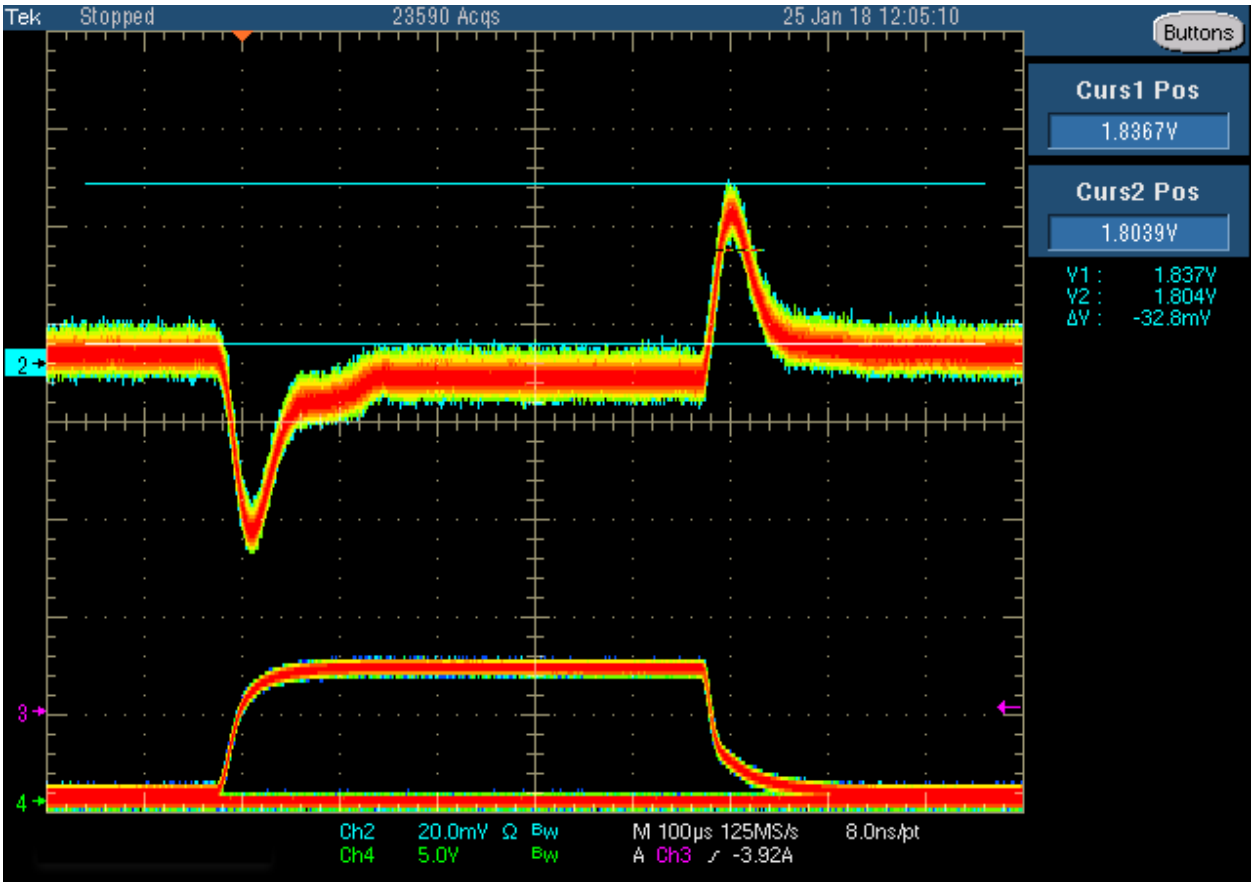


Figure 6 - VCC1V8 ac ripple release

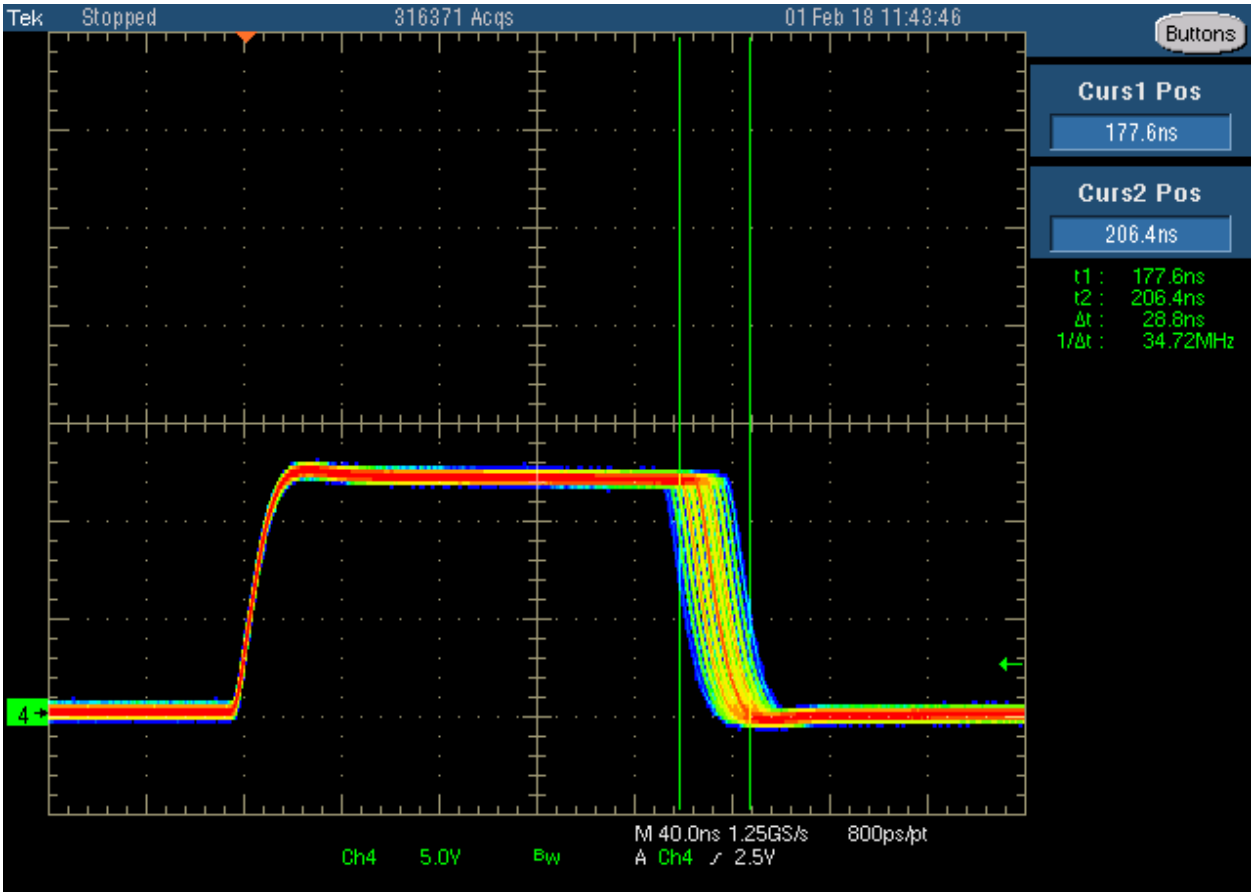
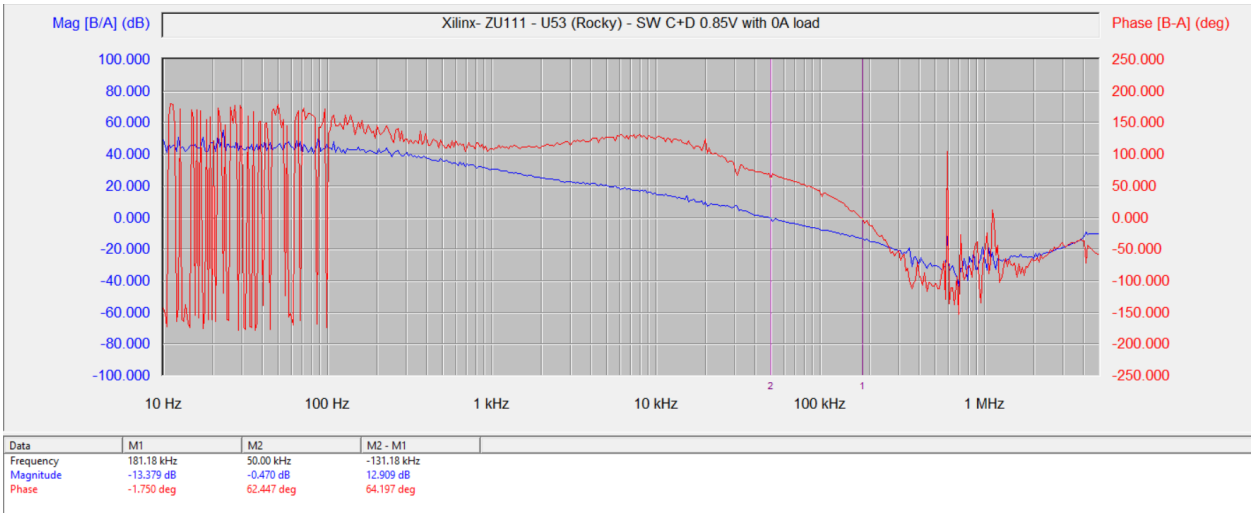


Figure 7 - VCC1V8 Jitter, 2A

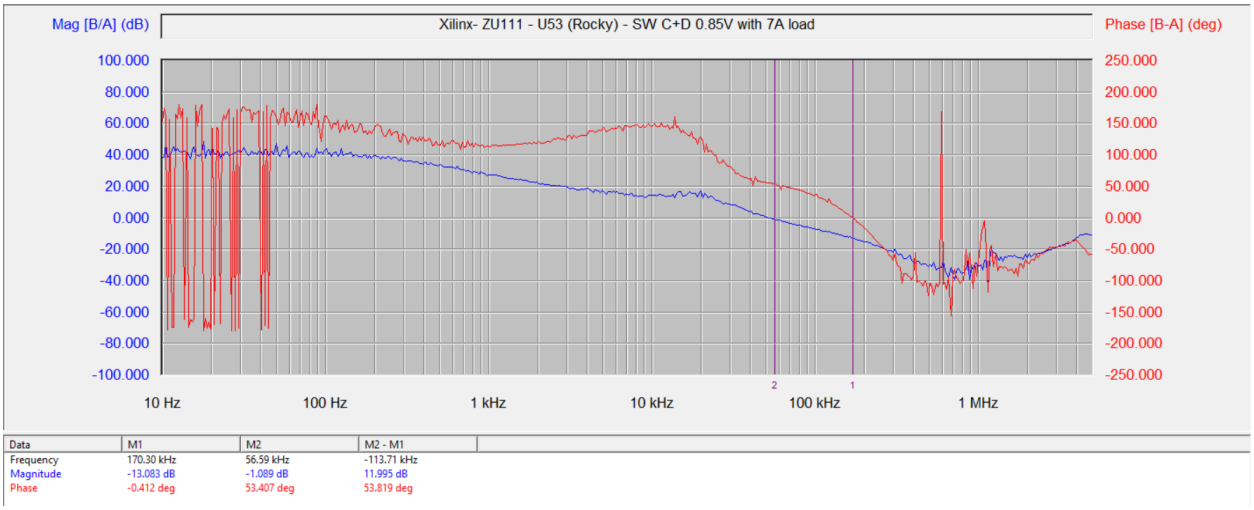
VCCINT_AMS

Vin, 12V
Vout, 0.85V
Iout(pk), 7A
Istep, 1.75A
Iramp, 2A/uS
Vout Measurement Location, C789, C119
Load Test Location, J62
SW Node Measurement Location, L20, L21
Jitter = 18.4ns (no load)
Config: IRPS5401MXI04TRP_MTPplus5_0.85V_1.8V_0.85V_800k_Rev2_2.txt

Bode Plot



With 0A load, the crossover frequency is around 50kHz where Phase Margin is 62.4 deg and Gain Margin is around -14dB



With 7A Load, the crossover frequency is around 56.6kHz with Phase Margin around 53.5 deg and Gain Margin is around -13dB

Table 6 – VCCINT_AMS Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.848V	Pass	0A 7A	DMM
DC Ripple	8.0mV 8.0mV	Pass	0A 7A	Coax
Isense	0A 3.33A 6.75A	Pass	0.0A 3.5A 7.0A	Telemetry/E-load
Vac(droop)	18.0mV	Pass	5.25A to 7.0A	
Vac(overshoot)	21.2mV	Pass	7.0A to 5.25A	

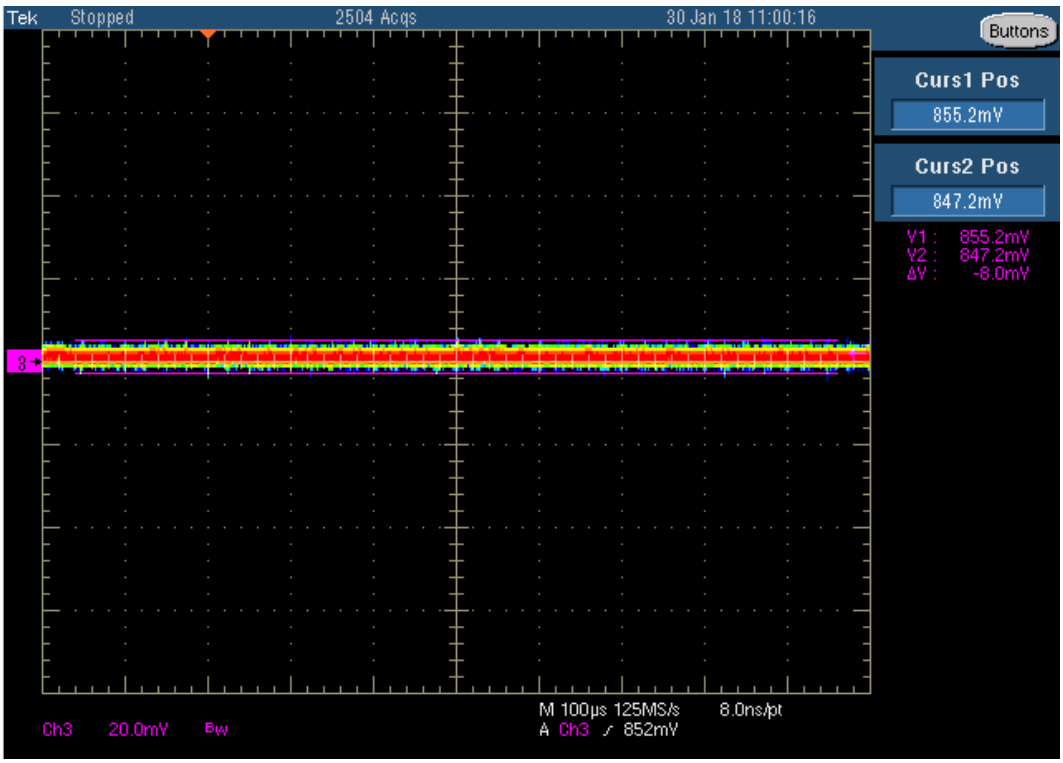


Figure 8 - VCCINT_AMS DC Ripple, 7A

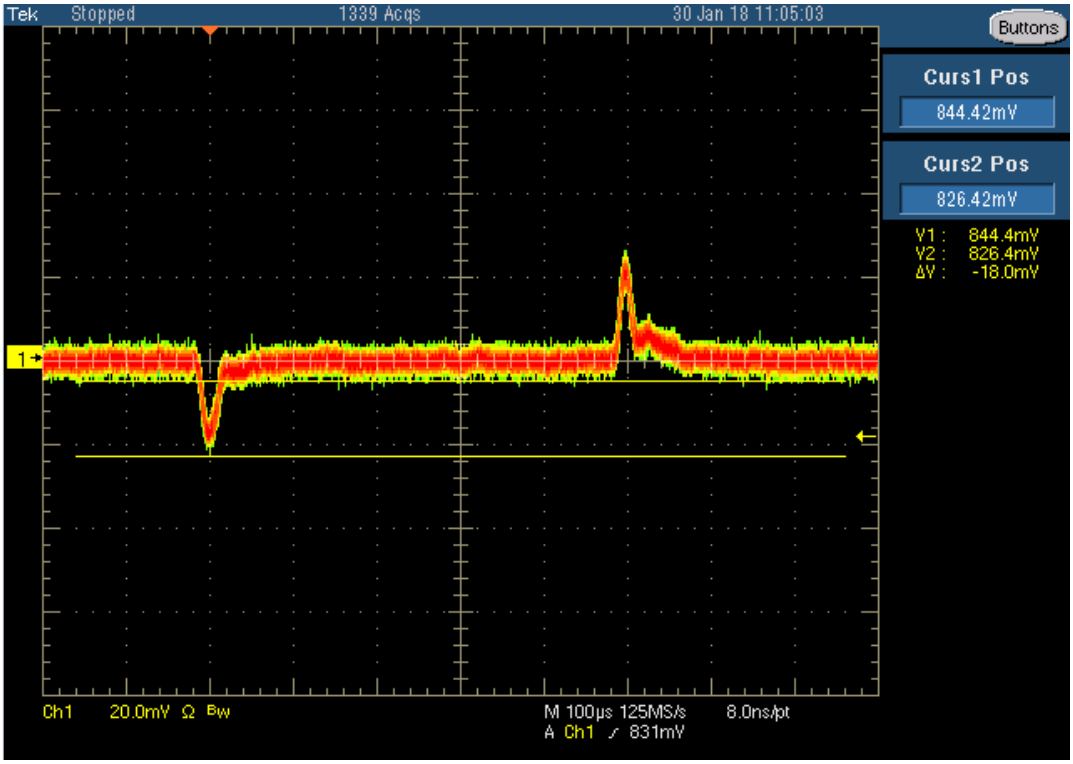


Figure 9 - VCCINT_AMS ac ripple load

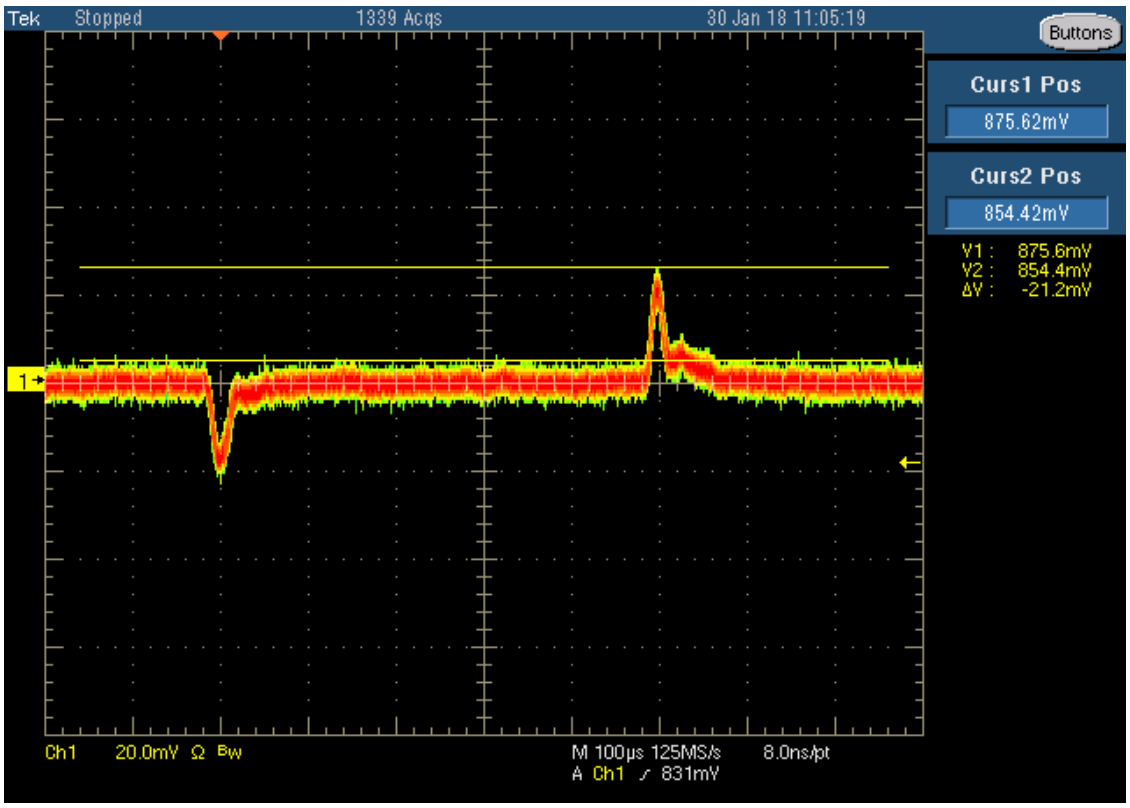


Figure 10 - VCCINT_AMS ac ripple release

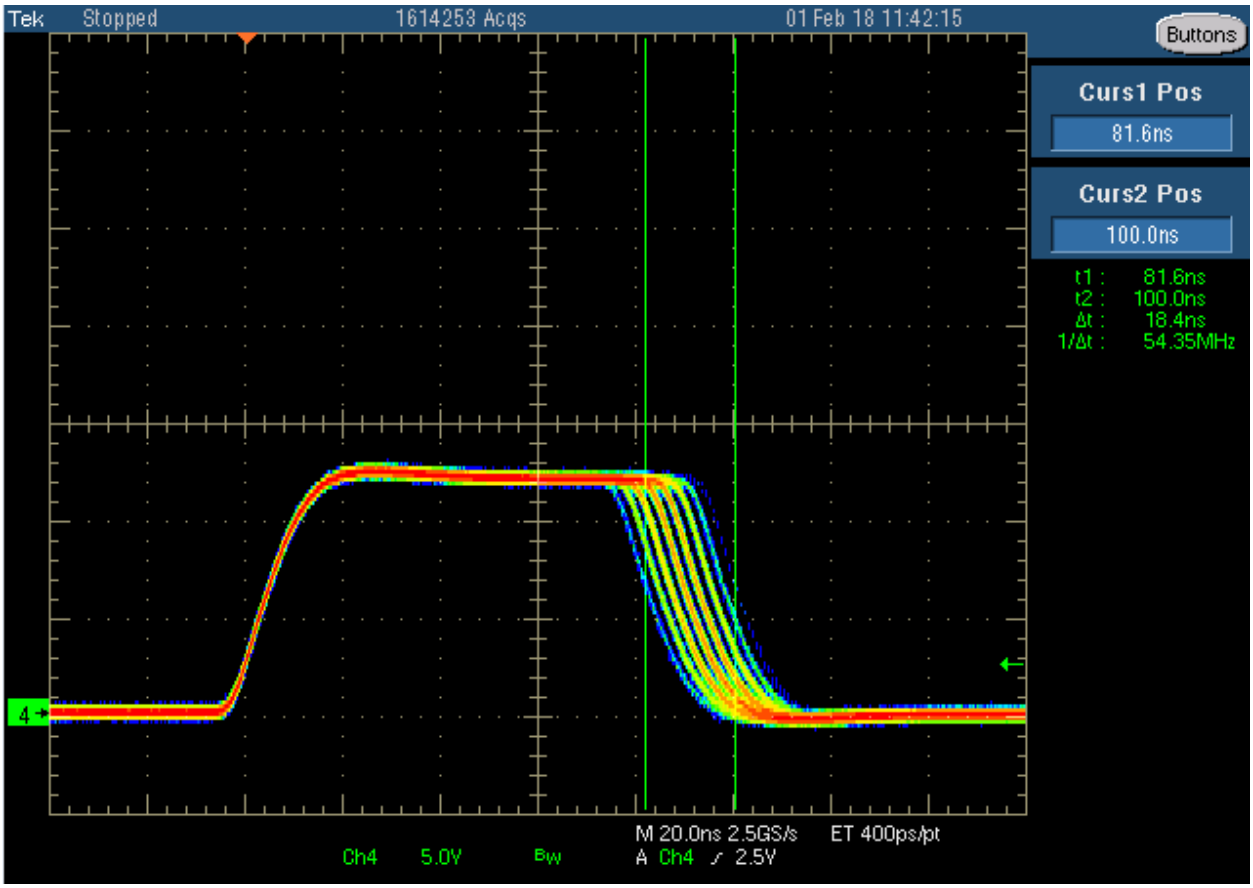


Figure 11 – VCCINT_AMS Jitter, 7A

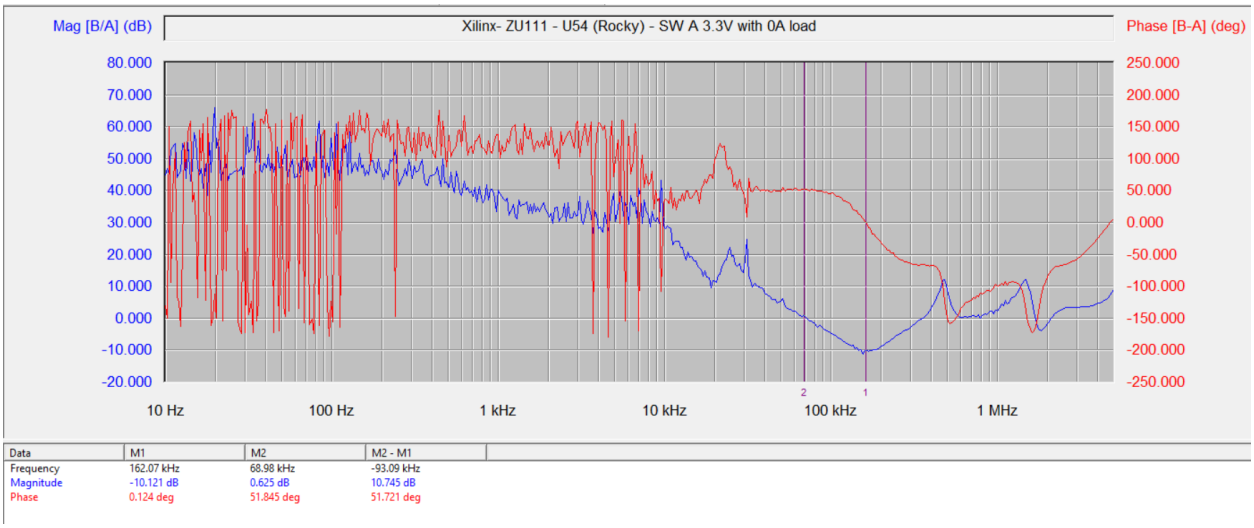
UTIL_3V3

Vin, 12V
Vout, 3.3V
Iout(pk), 15A (new from email)
Istep, 5A
Iramp, 1A/us

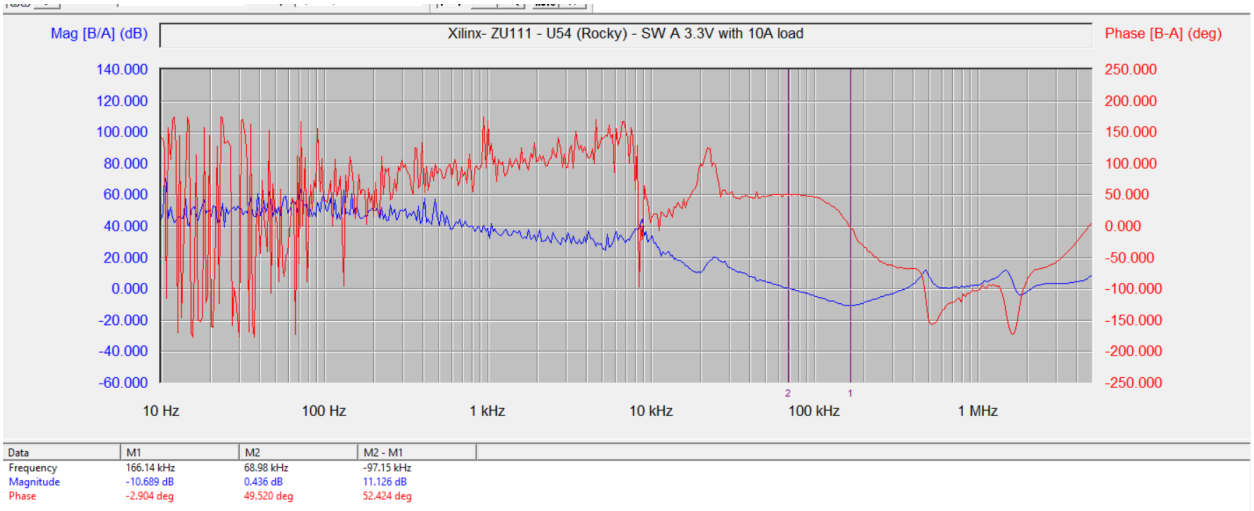
Vout Measurement Location, J69, U40, C183, J20
Load Test Location, J69
SW Node Measurement Location, L26

Jitter = 68ns (10A load)

Bode Analysis



With 0A Load the crossover frequency is around 69kHz with 52 deg of Phase Margin and Gain Margin of -10dB



With 10A Load, the crossover frequency is around 70kHz with 50 deg of Phase Margin and Gain Margin of -11dB

Config: IRPS5401MXI04TRP_MTPplus6_3.3V_2.5V_1.2V__0.85V_800k_Rev2_2.txt

Table 7 – UTIL_3V3 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	3.313V	Pass	0A 10A	DMM
DC Ripple	10.4mV 12.4mV 12.4mV	Pass	0A 10A 15A	Active probe
Isense	0.63A 5.25A 9.88A 14.88A	Pass	0A 5A 10A 15A	Telemetry/E-load
Vac(droop)	29.6mV 31.2mV	Pass	5A to 10A 10A to 15A	
Vac(overshoot)	25.2mV 30.0mV	Pass	10A to 5A 15A to 10A	

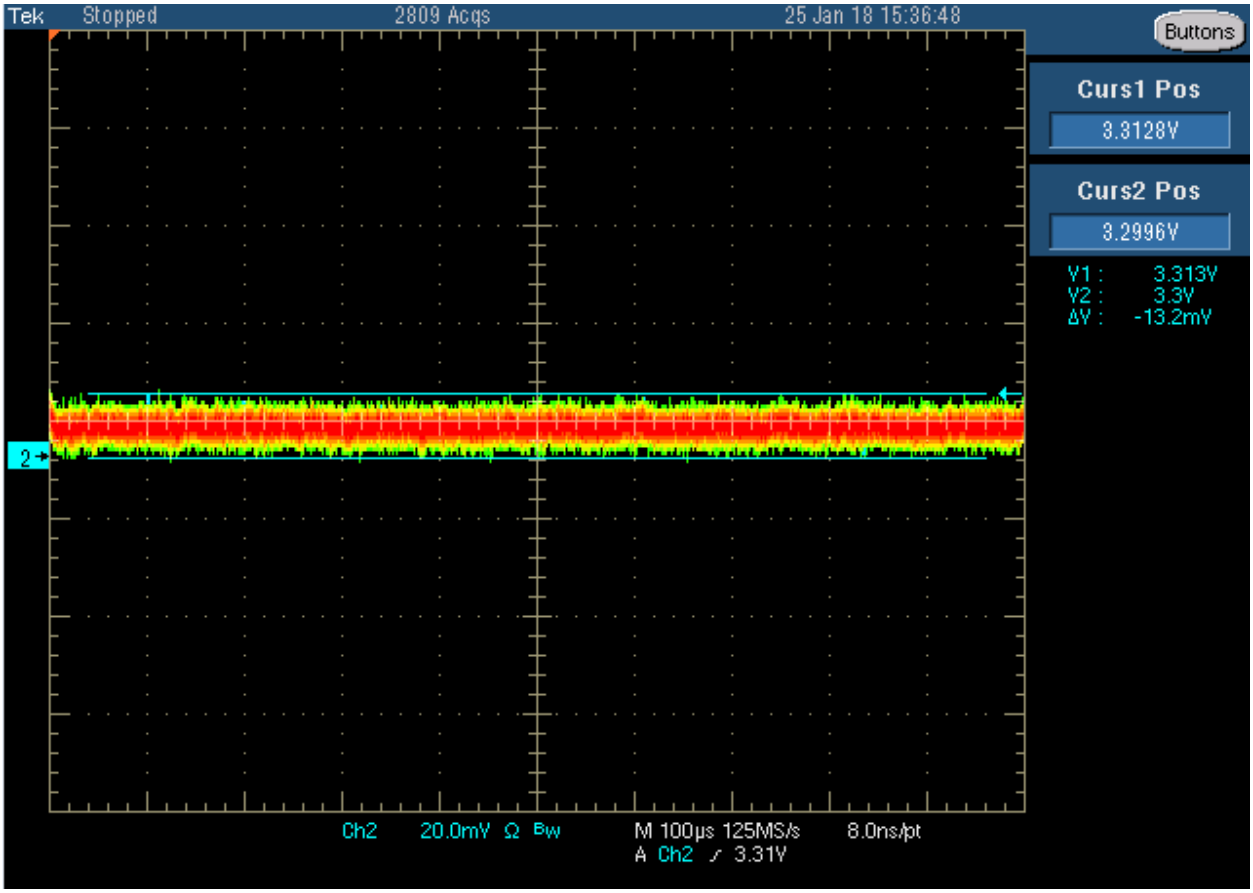


Figure 12 - UTIL_3V3 DC Ripple, 10A

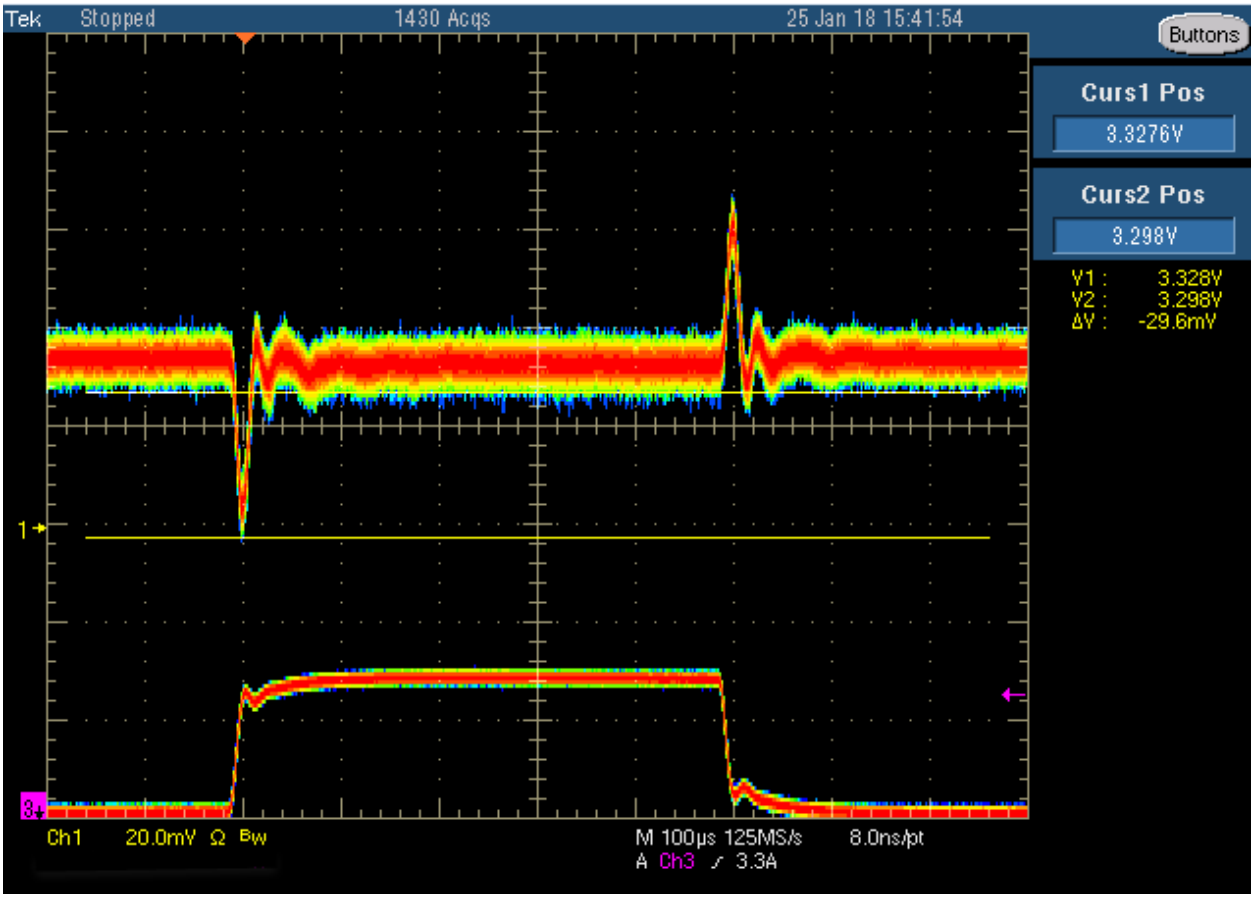


Figure 13 - UTIL_3V3 ac ripple load

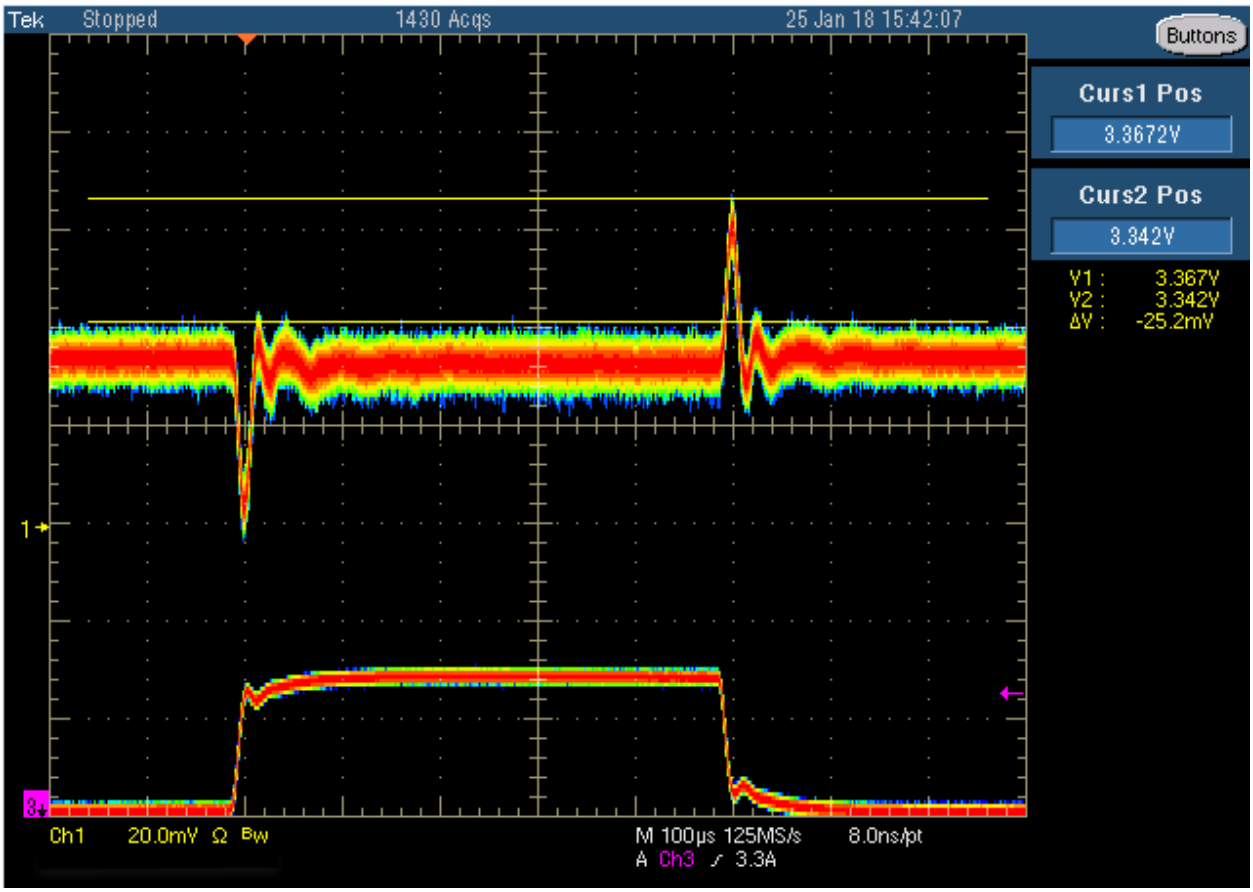


Figure 14 - UTIL_3V3 ac ripple unload

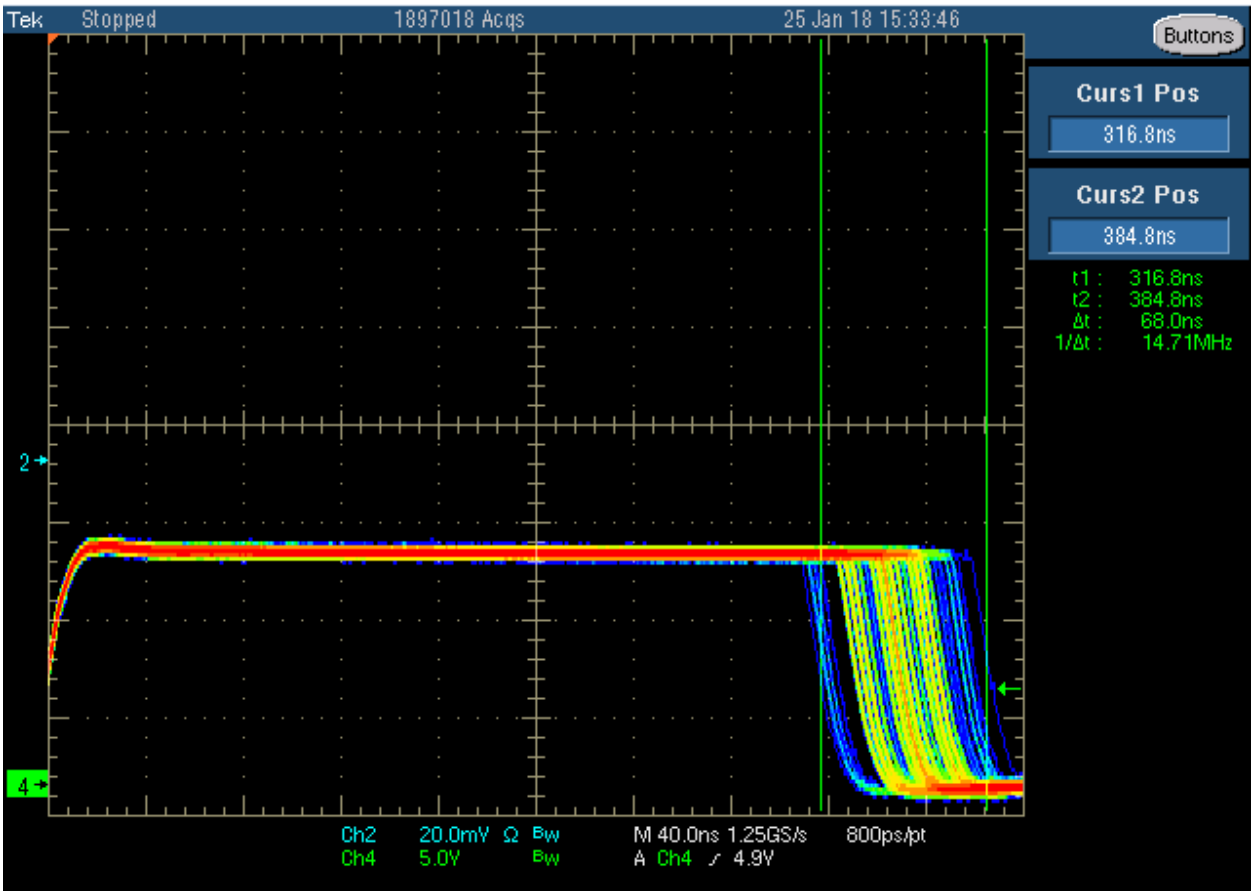


Figure 15 - UTIL_3V3 Jitter, 10A

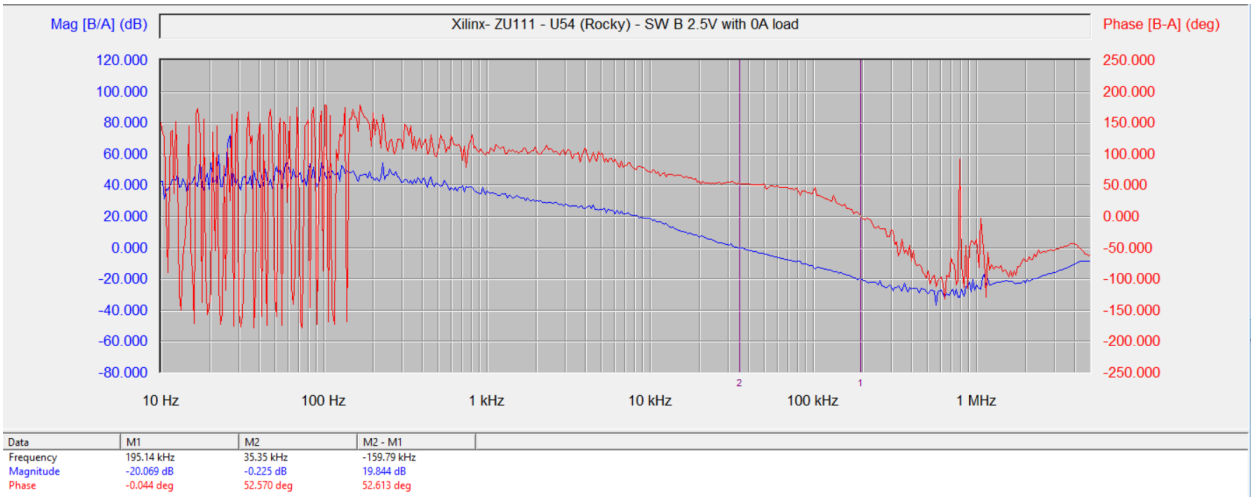
UTIL_2V5

Vin, 12V
Vout, 2.5V
Iout(pk), 2A
Istep, 1A
Iramp, 1A/us

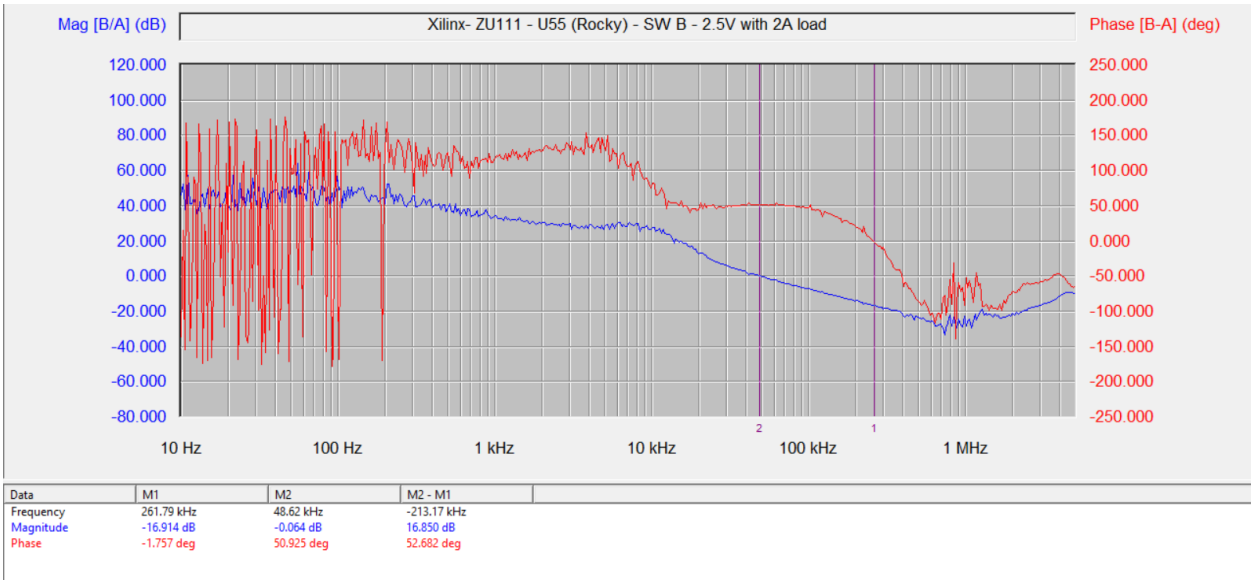
Vout Measurement Location, J66, L74
Load Test Location, J66
SW Node Measurement Location, L23

Jitter = 65ns (1A load)

Bode Analysis



With 0A load, the crossover frequency is around 35.3kHz and 52 deg of Phase Margin and Gain Margin of -20dB



With 2A load, the crossover frequency was around 48.62kHz with 51 deg of Phase Margin and Gain Margin of -17dB.

Config: IRPS5401MXI04TRP_MTPplus6_3.3V_2.5V_1.2V__0.85V_800k_Rev2_2.txt

Table 8 – UTIL_2V5 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	2.500V	Pass	0A 2A	DMM
DC Ripple	26.8mV 26.8mV	Pass	0A 2A	Active probe
Isense	0.03A 2.00A	Pass	0A 2A	Telemetry/E-load
Vac(droop)	22.8mV	Pass	1A to 2A	At Ethernet At LDO input
Vac(overshoot)	26.8mV	Pass	2A to 1A	At Ethernet At LDO input

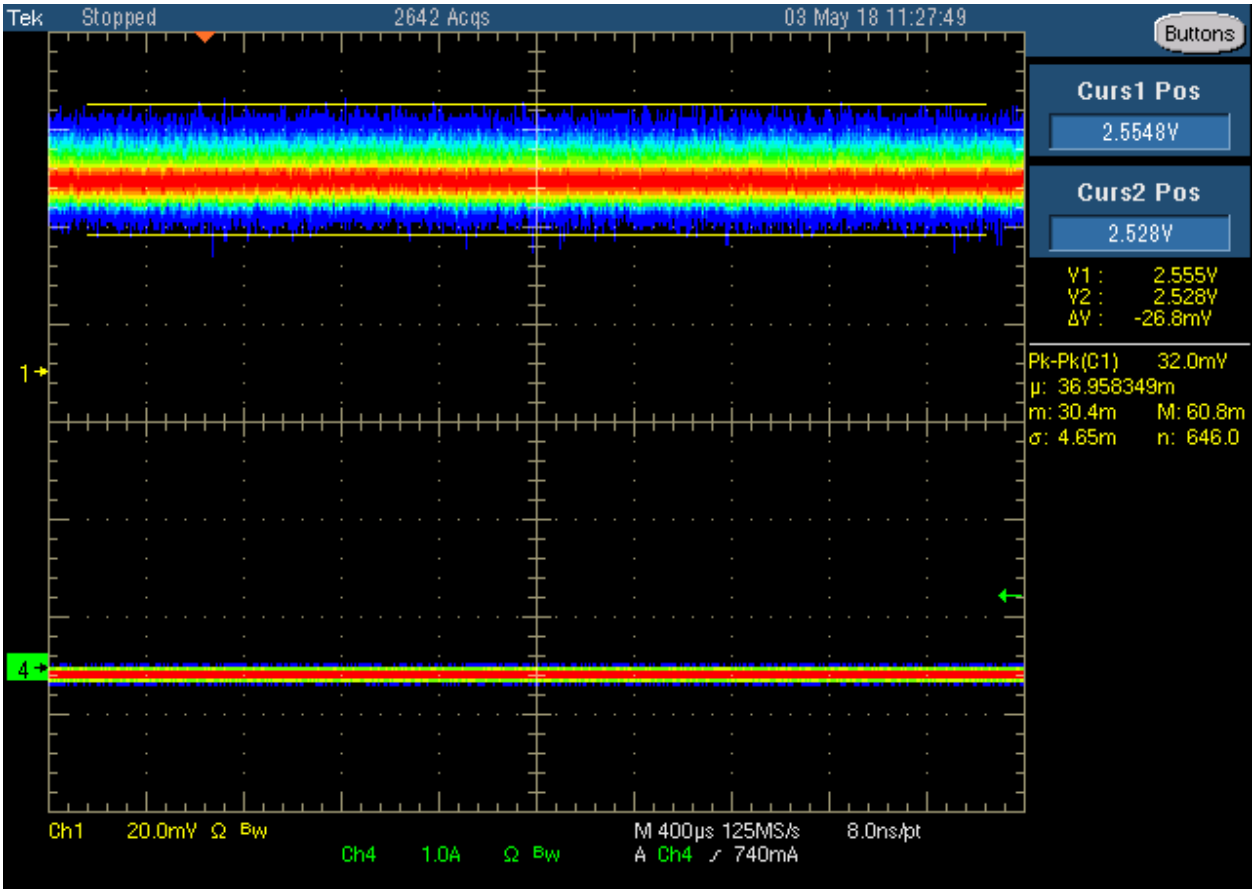


Figure 16 - UTIL_2V5 DC Ripple, 0A

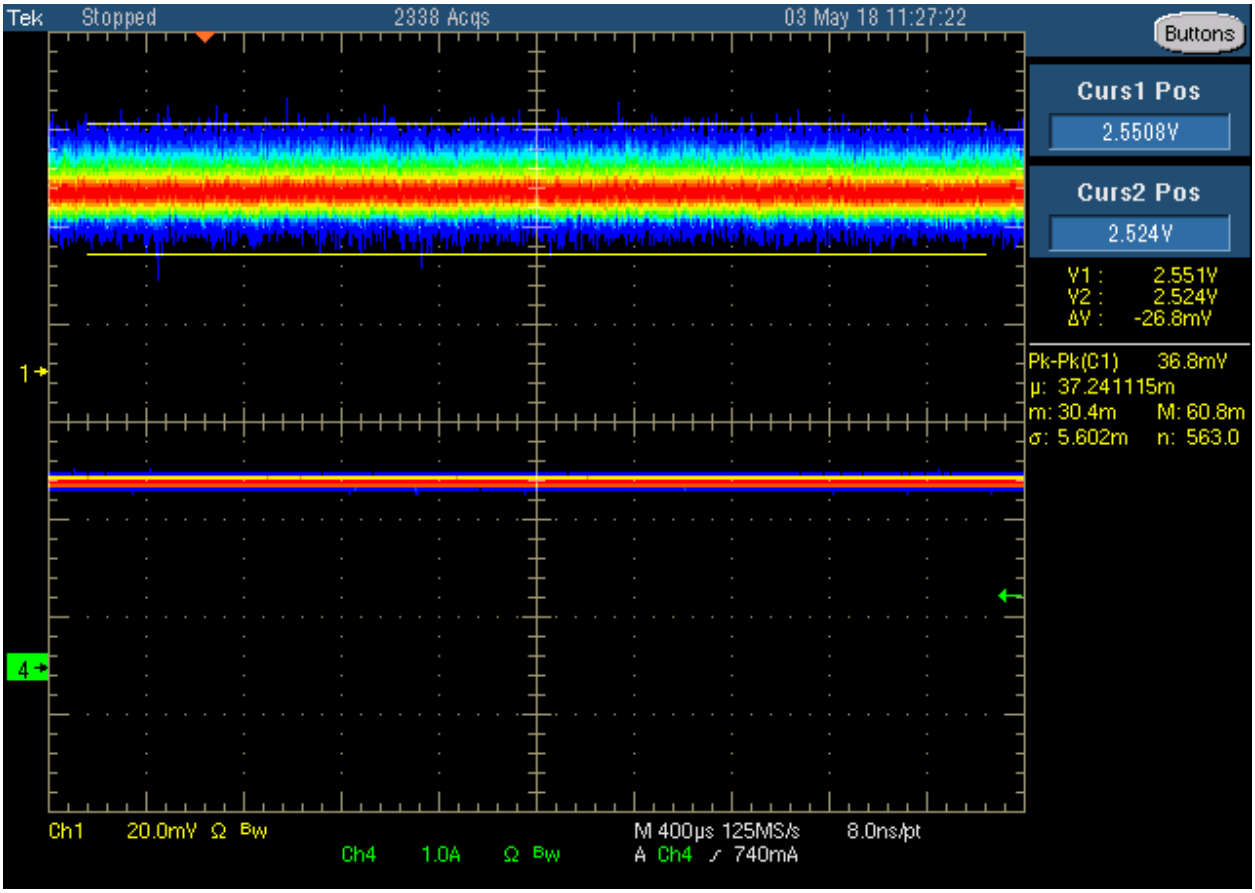


Figure - UTIL_2V5 DC Ripple, 2A

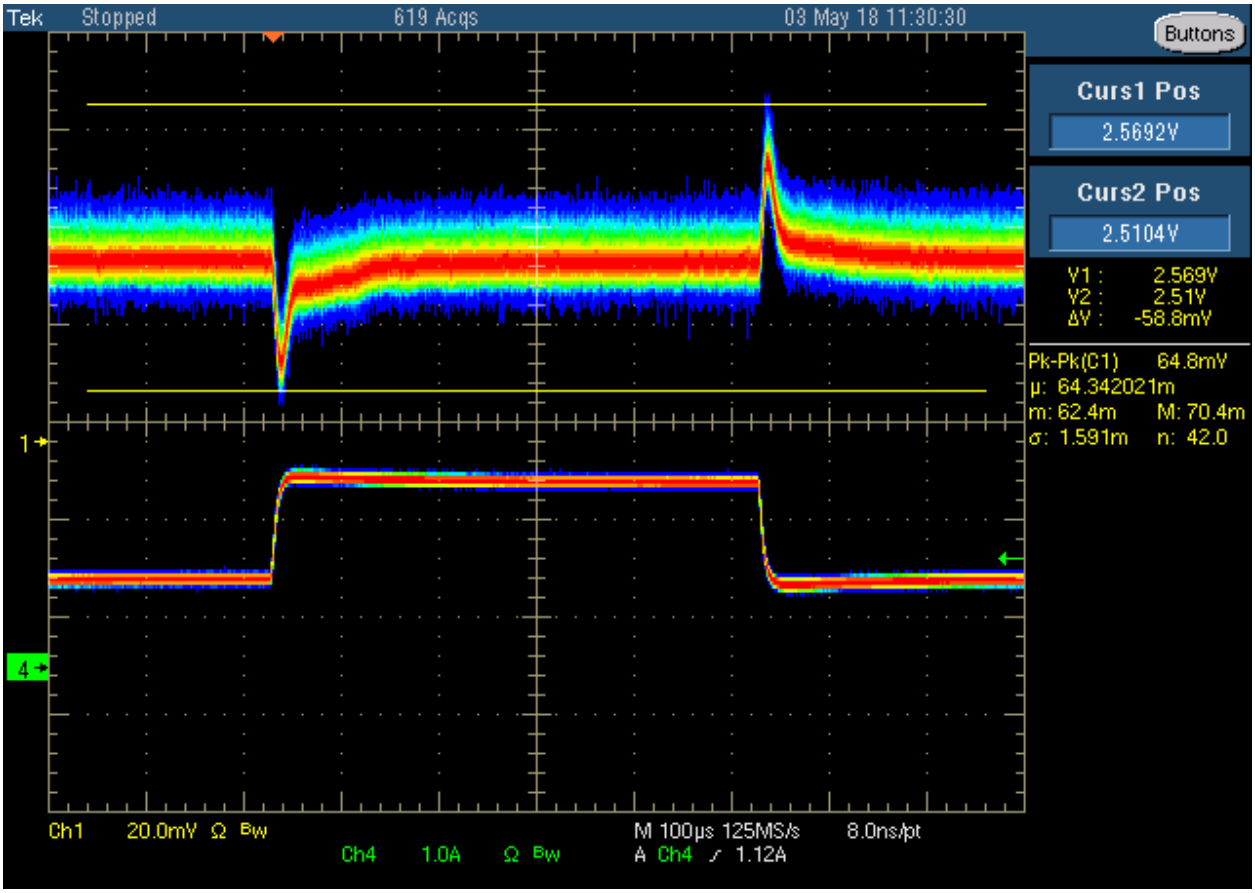


Figure 17 - UTIL_2V5 Transient Load: 1-2A load step

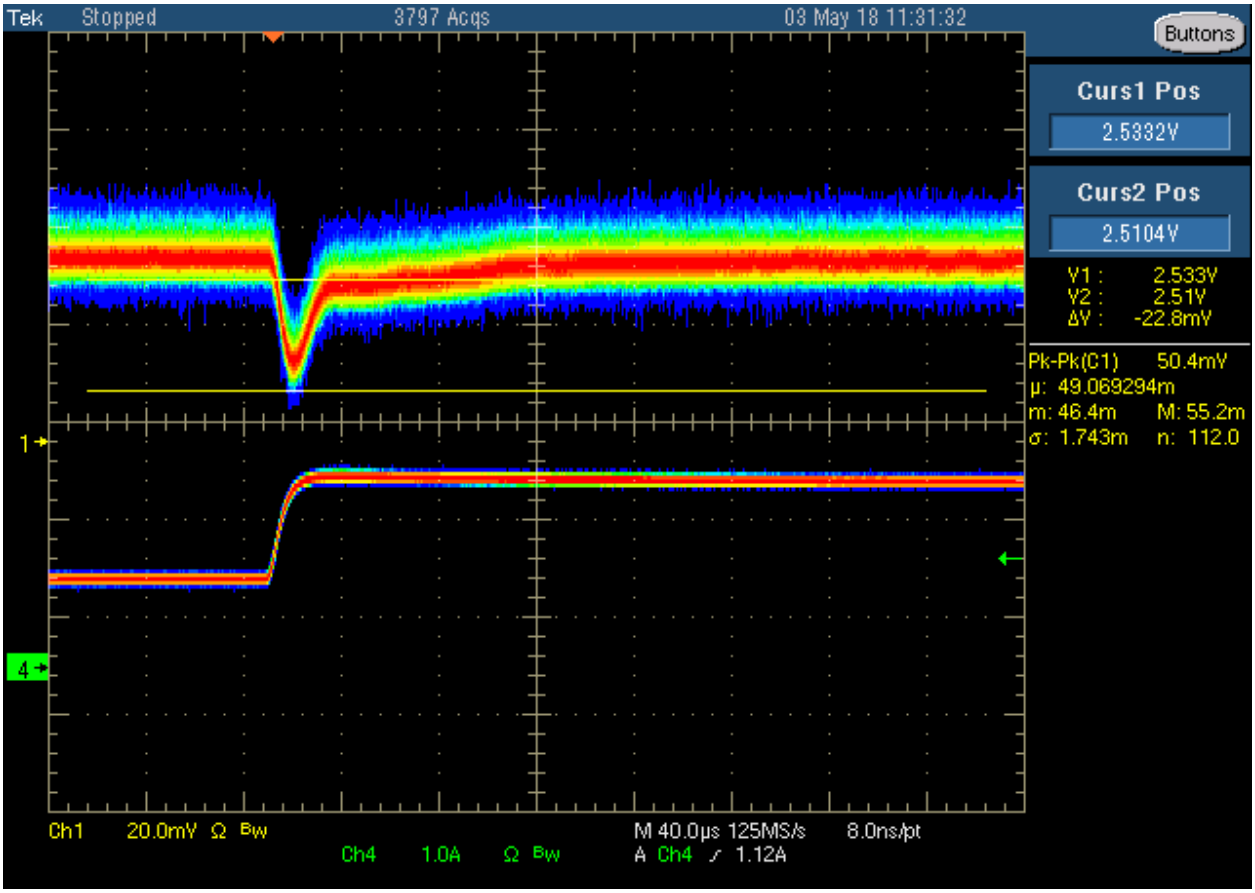


Figure 18 - UTIL_2V5 – Vout excursion during a transient load is around 22.8mV

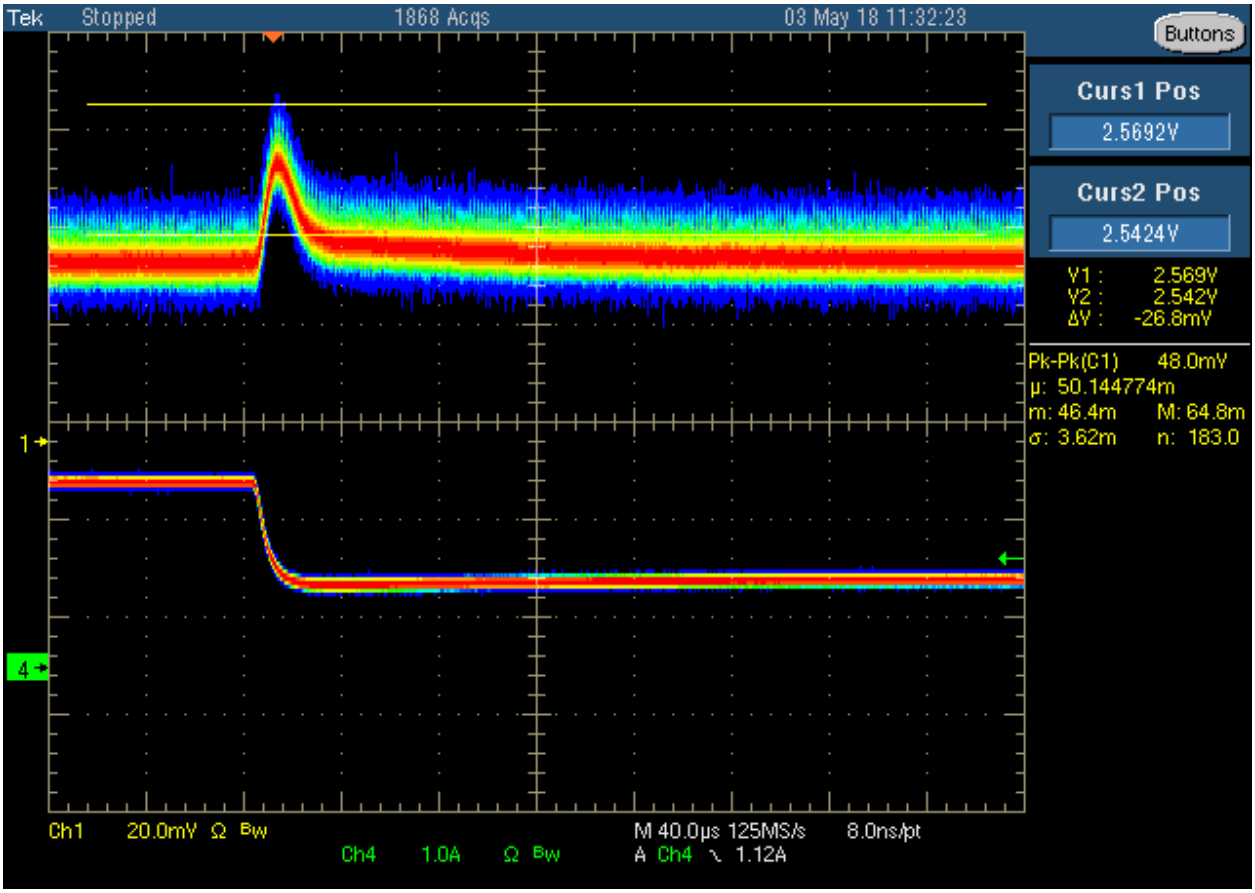


Figure – UTIL_2V5 Transient load release: Vout overshoot is around 26.8mV

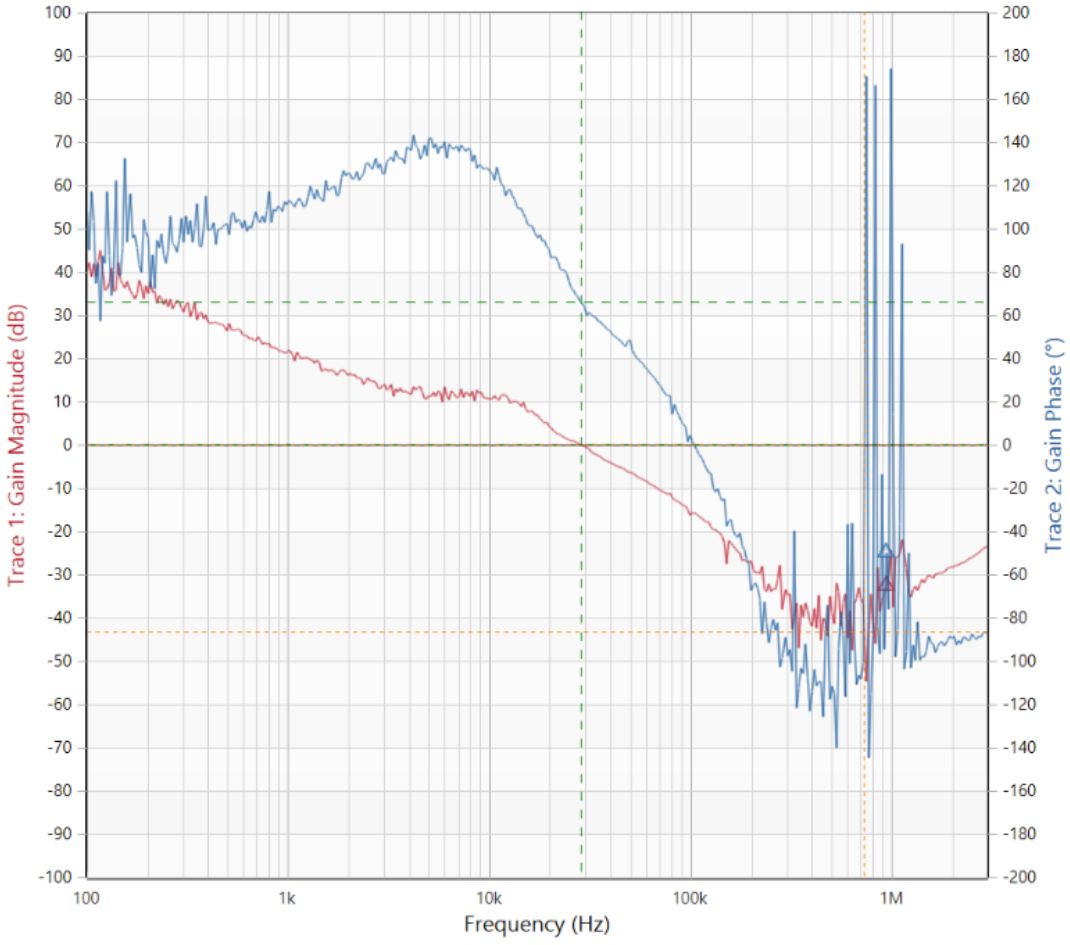
MGT1V2

Vin, 12V
Vout, 1.2V
Iout(pk), 6A
Istep, 2.5A
Iramp, 1A/us

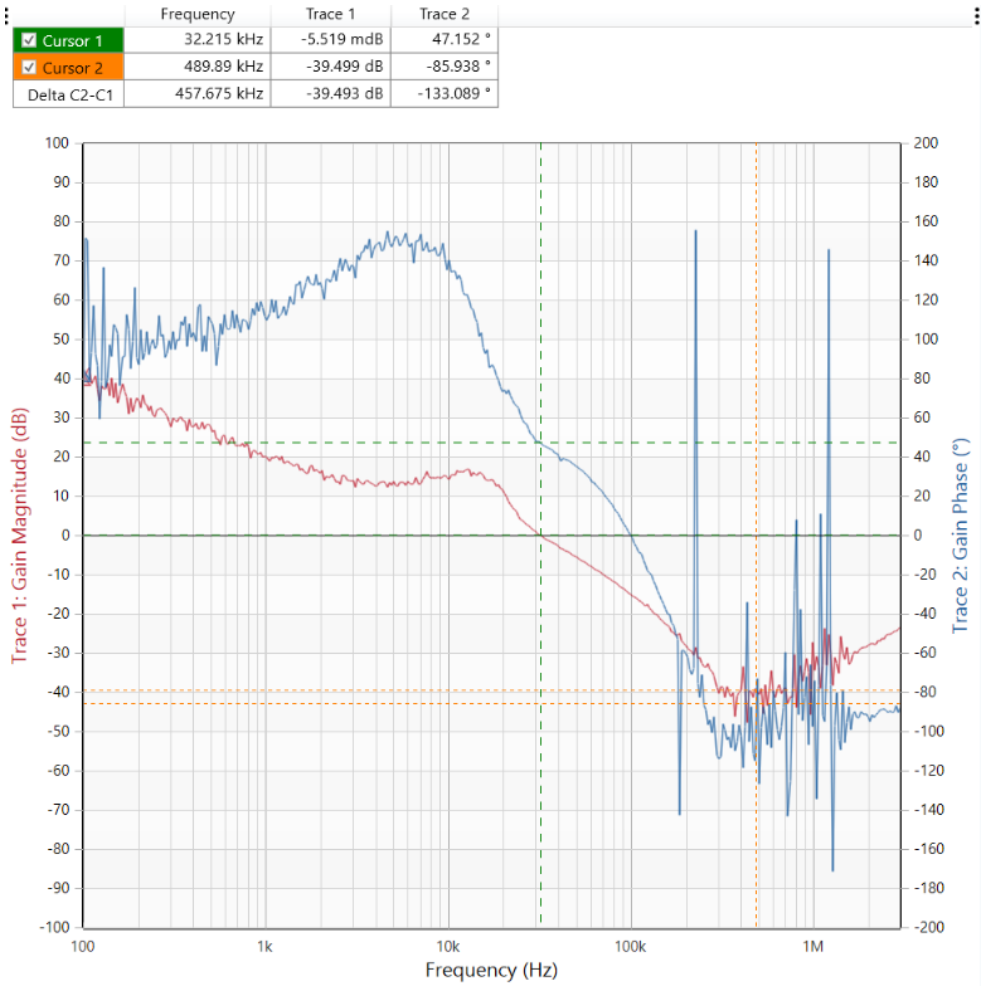
Vout Measurement Location, J67, C942, C124, C943
Load Test Location, J67
SW Node Measurement Location, L81
Jitter = 43ns (6A)

Bode Analysis

	Frequency	Trace 1	Trace 2
Cursor 1	28.795 kHz	0 dB	65.931 °
Cursor 2	733.95 kHz	-43.276 dB	-9.237 p°
Delta C2-C1	705.155 kHz	-43.276 dB	-65.931 °



With 0A load, the crossover frequency is 28.8kHz with 66deg phase margin and -43dB of Gain Margin



With 6A load, the crossover frequency is around 32.2kHz with 47 deg of phase margin and Gain Margin is around -30dB

Config: IRPS5401MXI04TRP_MTPplus6_3.3V_2.5V_1.2V__0.85V_800k_Rev2_2.txt

Table 9 – MGT1V2 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.207V	Pass	0A 6A	DMM
DC Ripple	14.3mV 14.2mV	Pass	0A 6A	Diff Probe
Isense	0.00A 5.89A	Pass	0A 6A	Telemetry/Eload
Vac(droop)	57mV	Pass	3.5A to 6.0A	
Vac(overshoot)	57mV	Pass	6.0A to 3.5A	

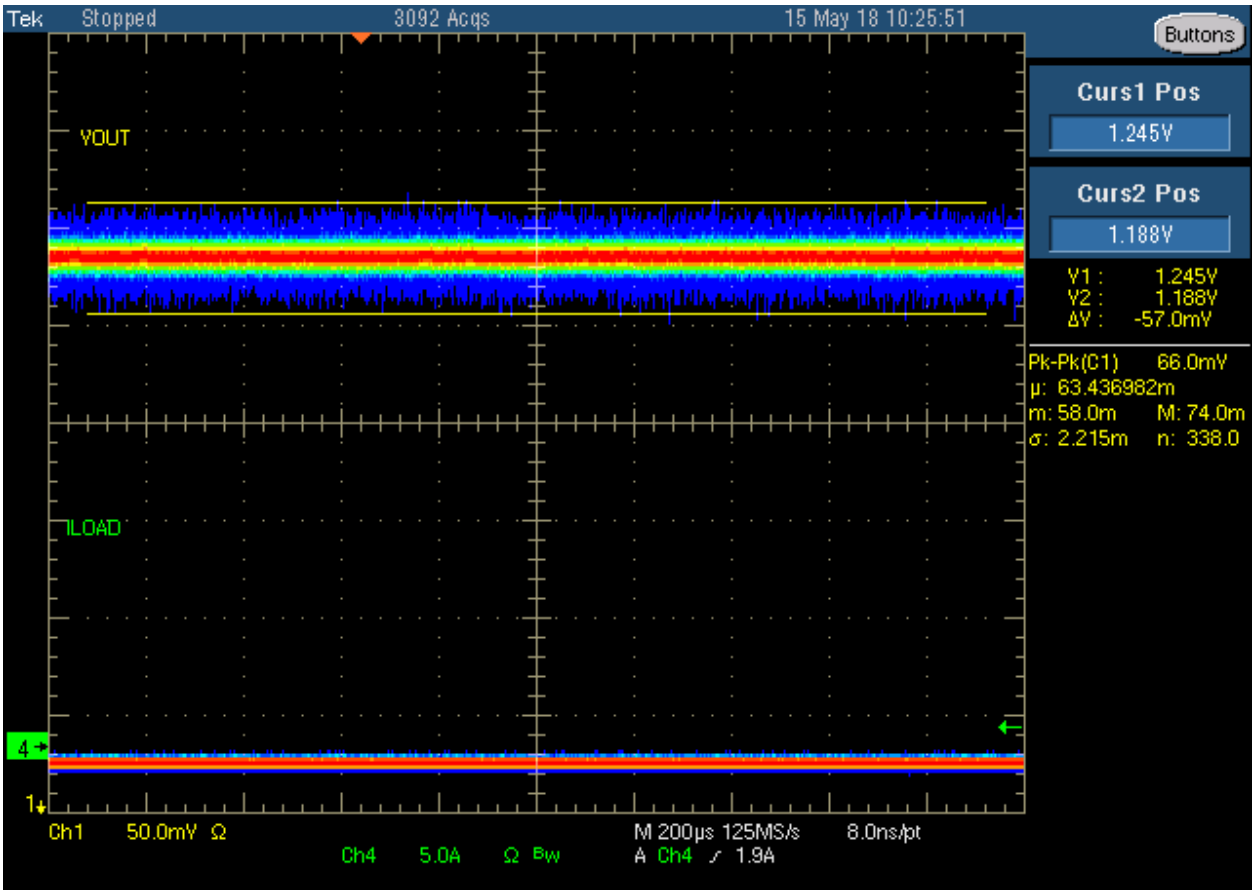


Figure 19 - MGT1V2 DC Ripple with 0A load

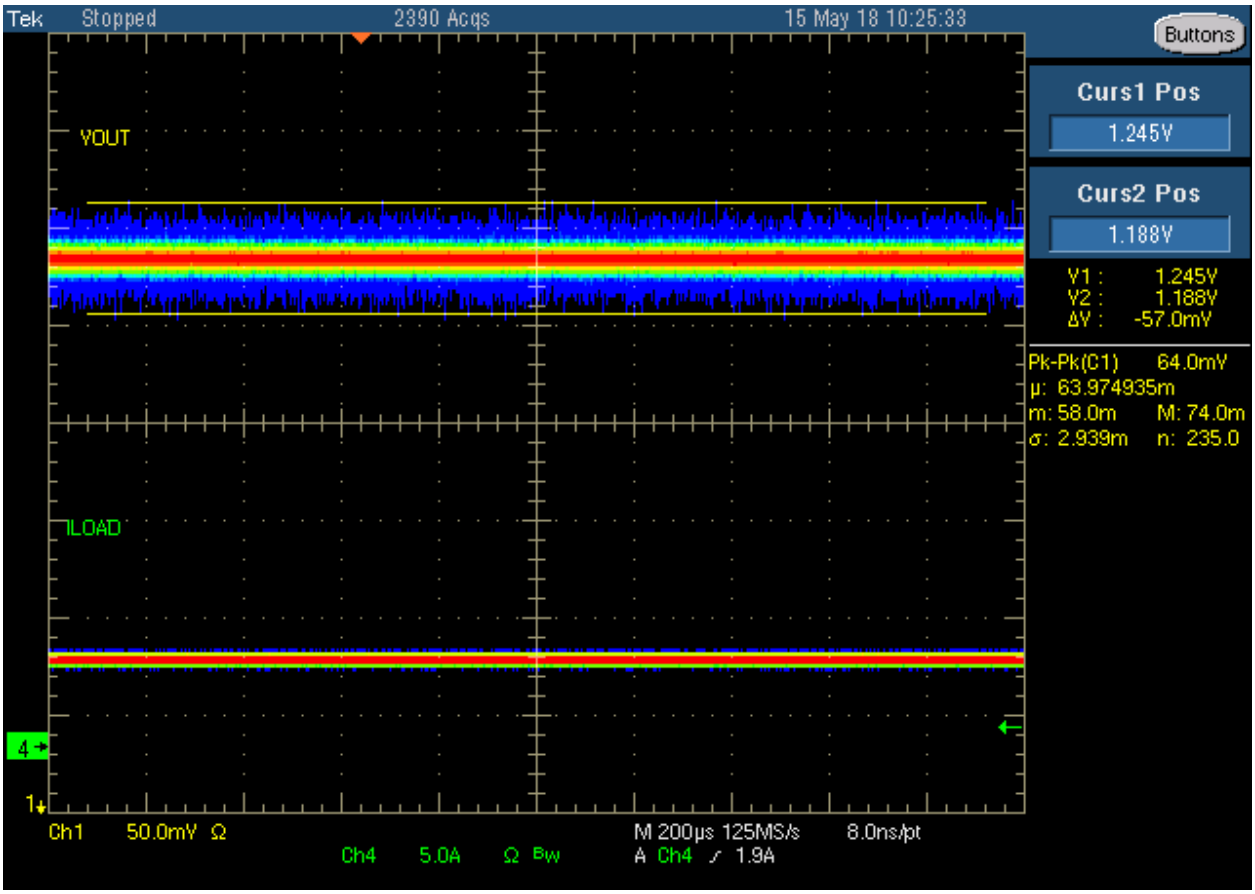


Figure: DC ripple with 6A load

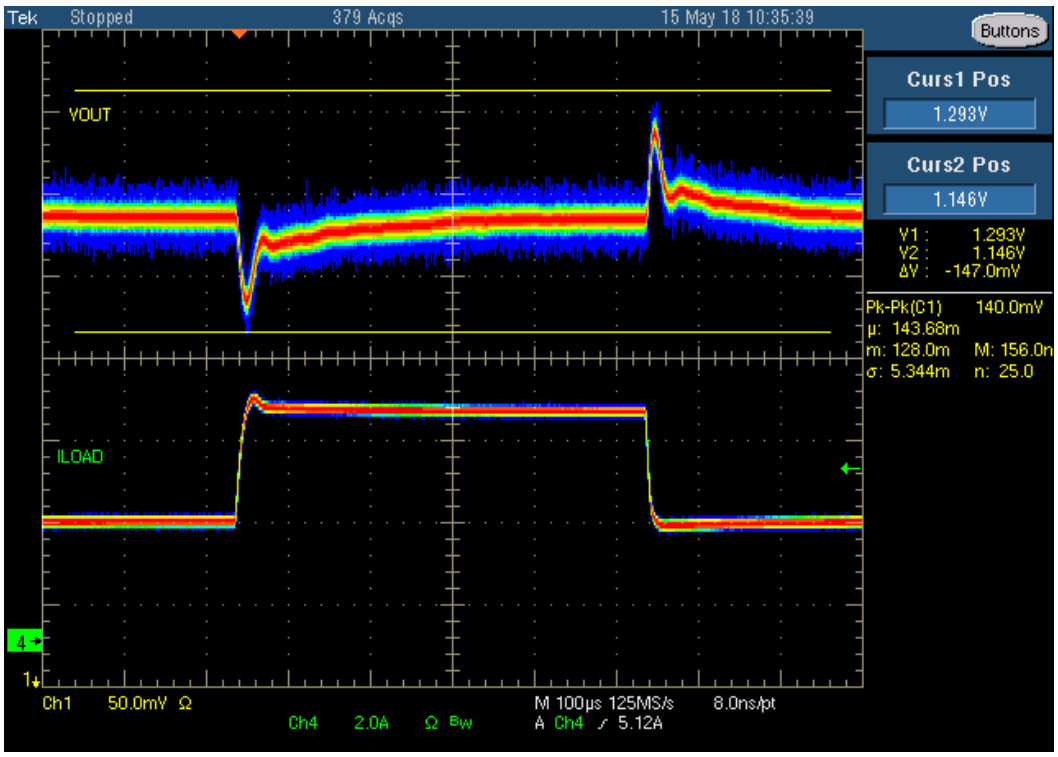


Figure 20 - MGT1V2 ac ripple load with 3.5A – 6A

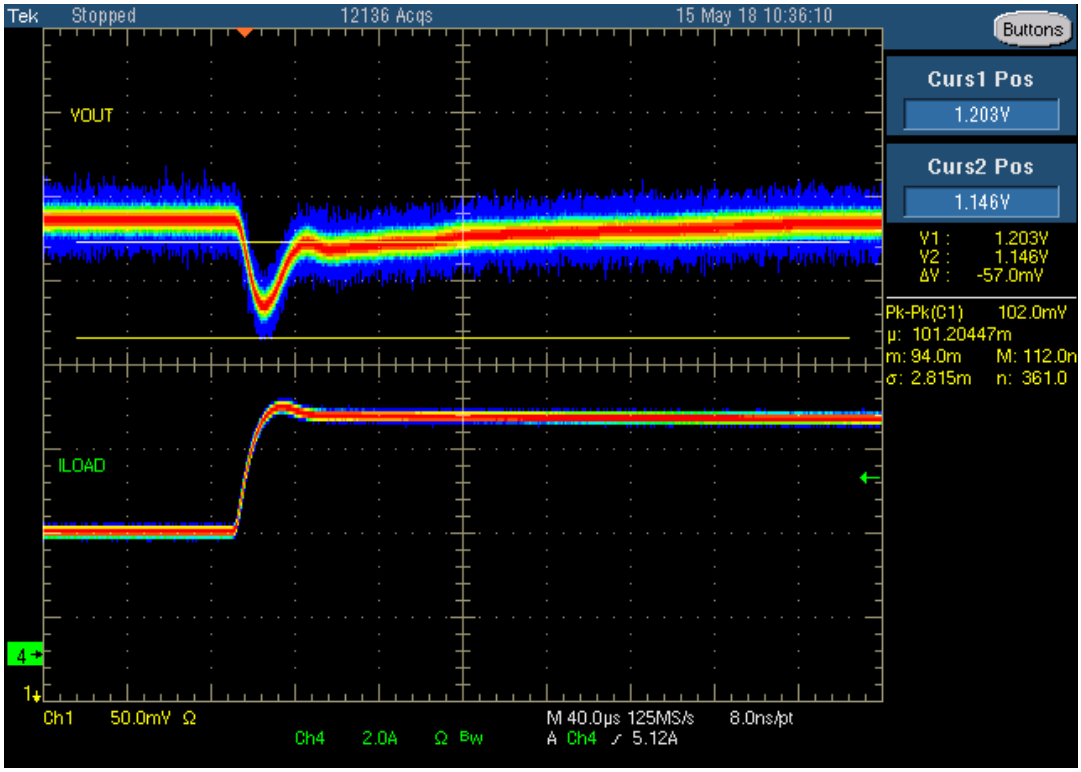


Figure: Vout excursion during a 3.5-6A load step is around 57mV

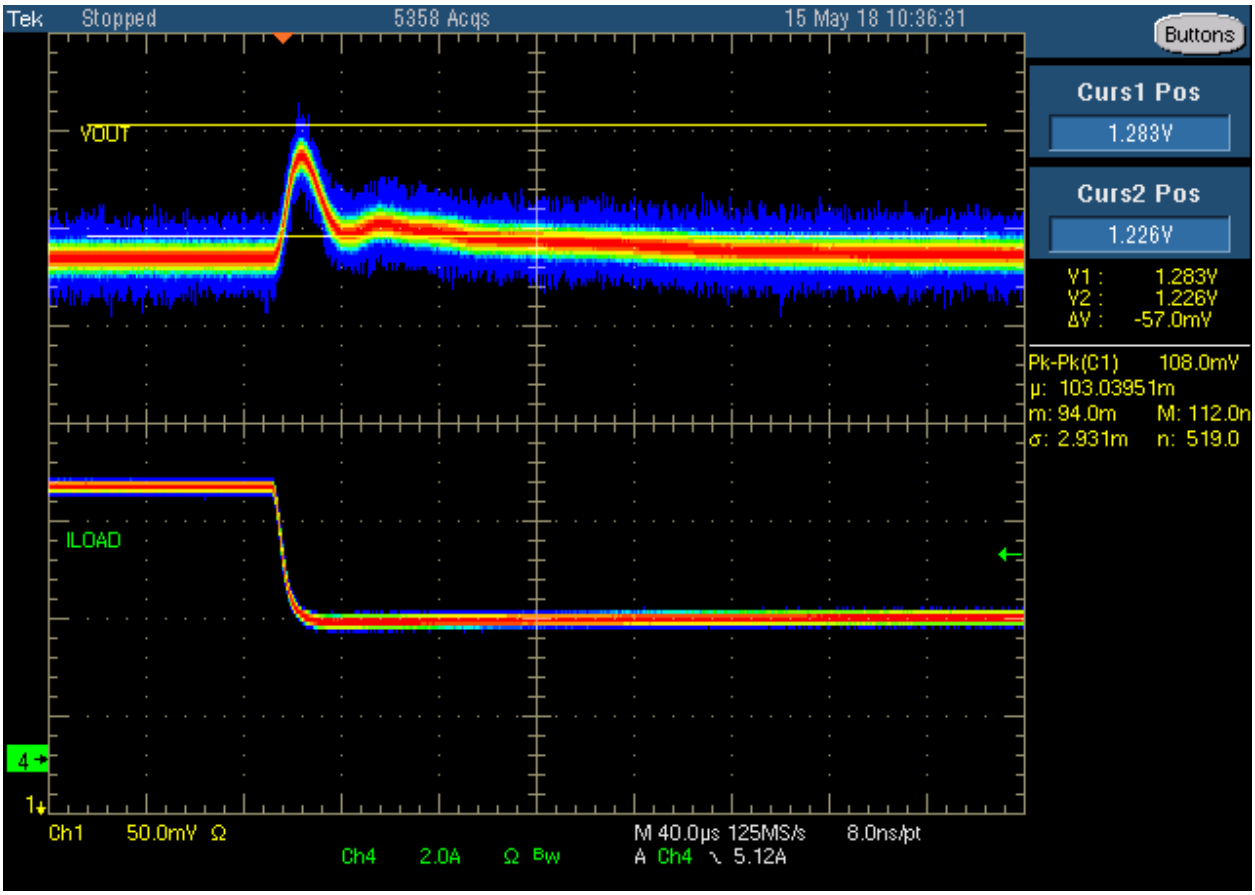


Figure: Vout overshoot during a 6A-3.5A load release is around 57mV

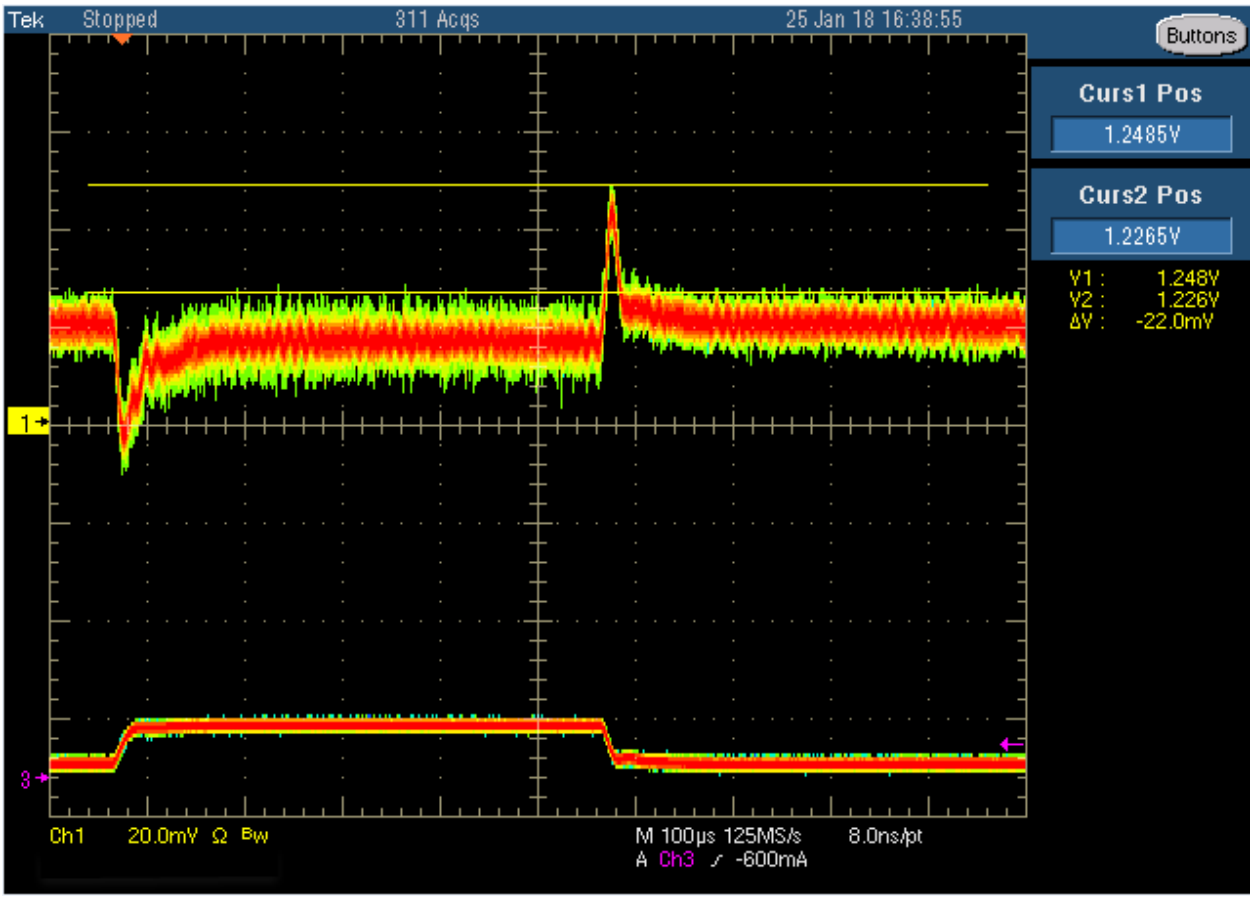


Figure 21 - MGT1V2 ac ripple release

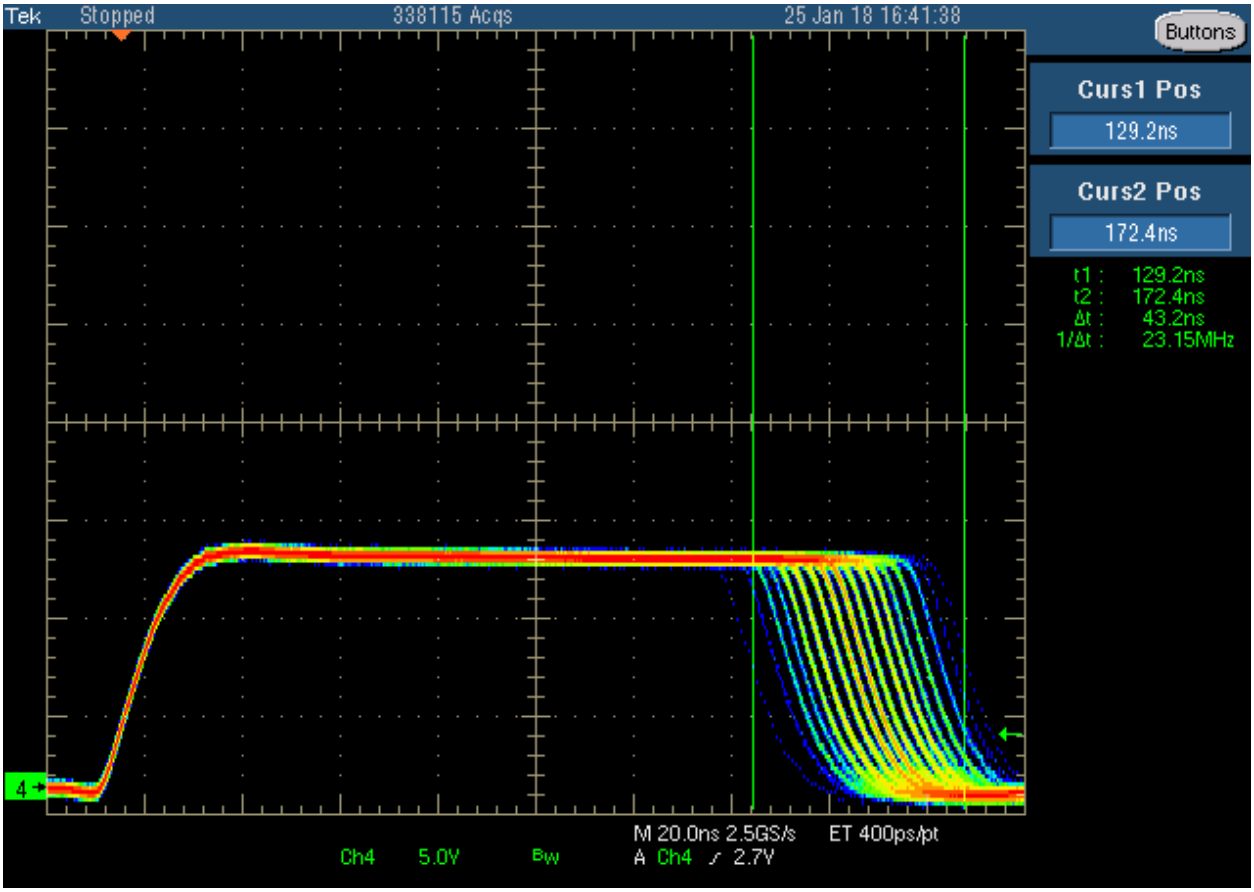


Figure 22 - MGT1V2 Jitter, 6A

MGTRAVCC

Vin, 2.5V
Vout, 0.85V
Iout(pk), 0.5A
Istep, 0.25A
Iramp, 1A/us

Vout Measurement Location, J68, C129
Load Test Location, J68

Config: IRPS5401MXI04TRP_MTPplus6_3.3V_2.5V_1.2V__0.85V_800k_Rev2_2.txt

Table 10 – MGTRAVCC Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.842V 0.844V	Pass	0.0A 0.5A	DMM
DC Ripple	5.8mV 5.8mV	Pass	0.0A 0.5A	Coax
Isense	0.0A 0.5A	Pass	0A 0.5A	Telemetry/E-load
Vac(droop)	3.6mV	Pass	0.25A to 0.5A	
Vac(overshoot)	3.8mV	Pass	0.5A to 0.25A	

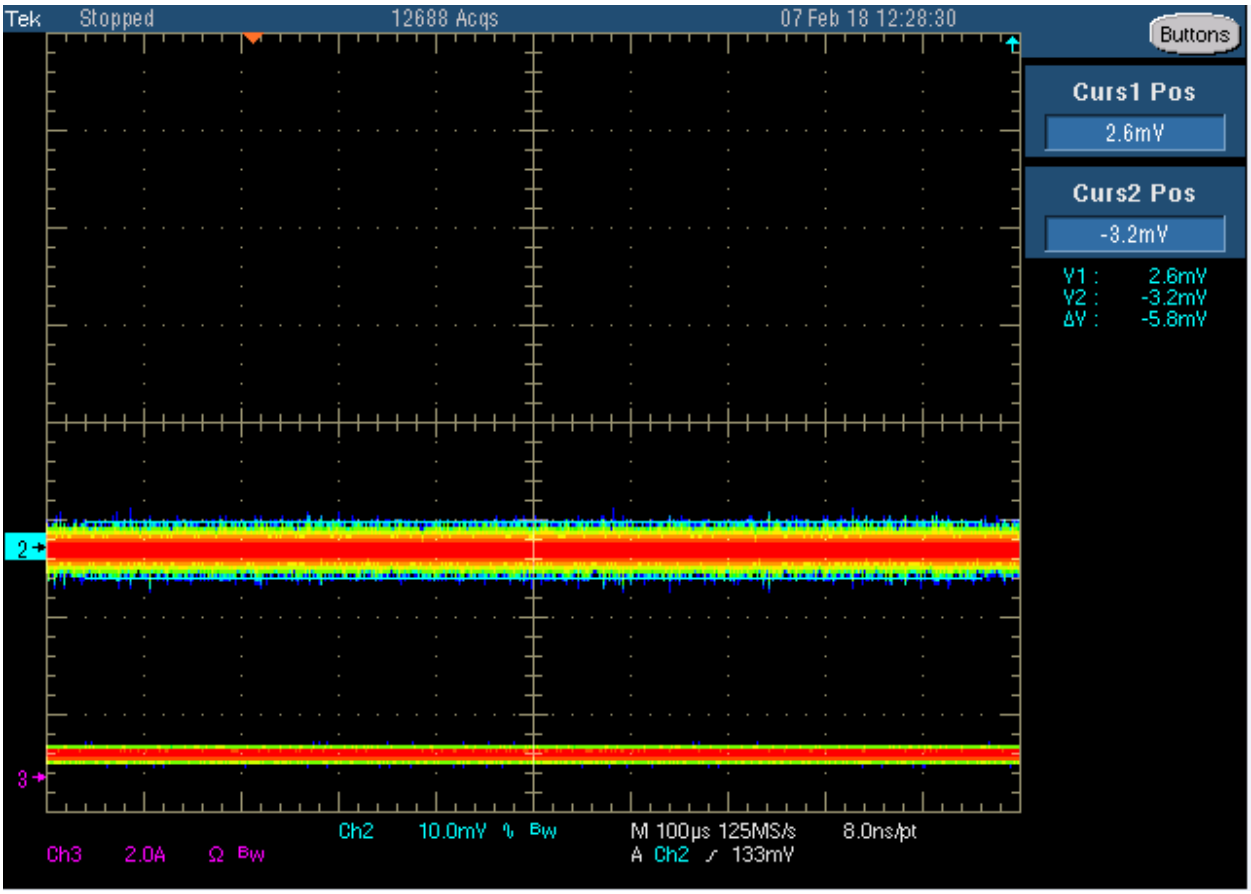


Figure 23 - MGTRAVCC DC Ripple, 0.5A

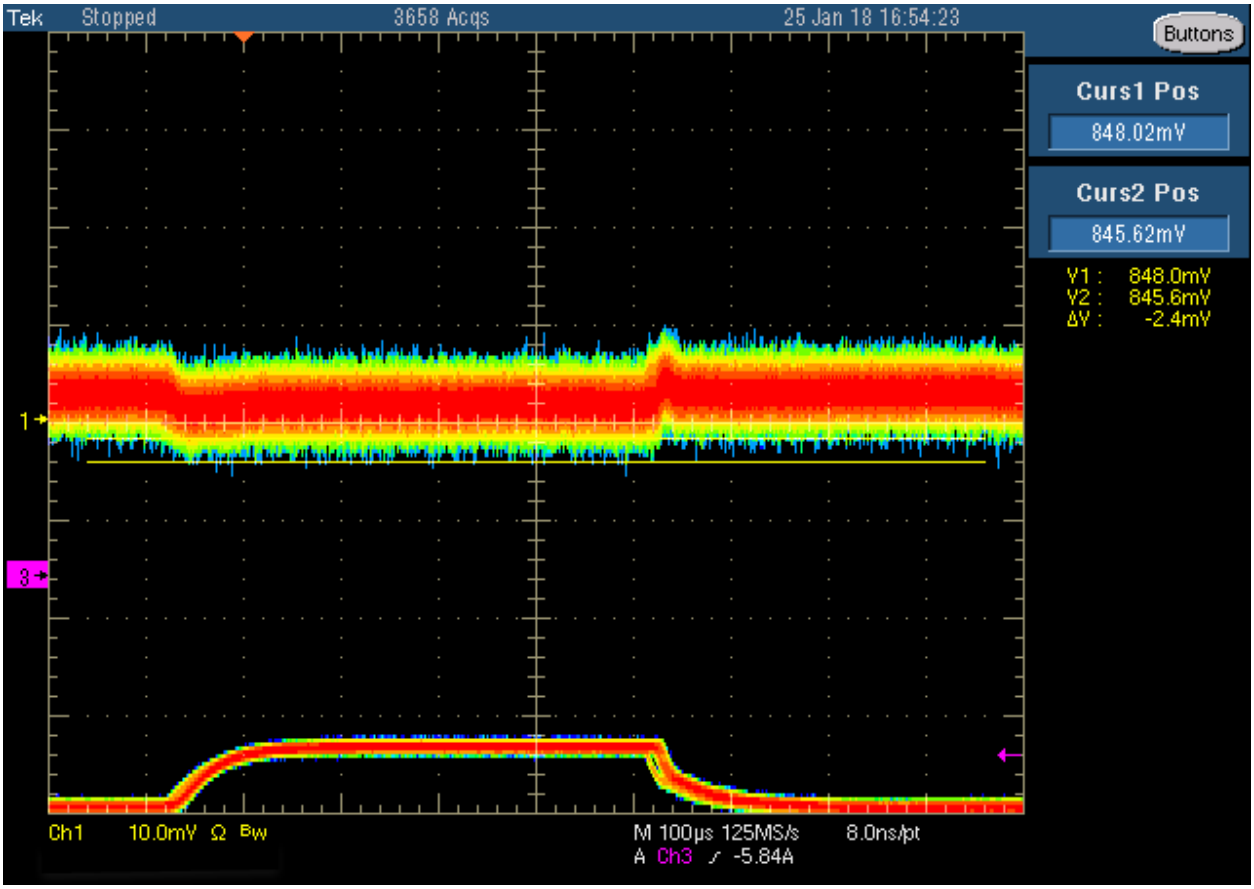


Figure 24 - MGTRAVCC ac ripple load

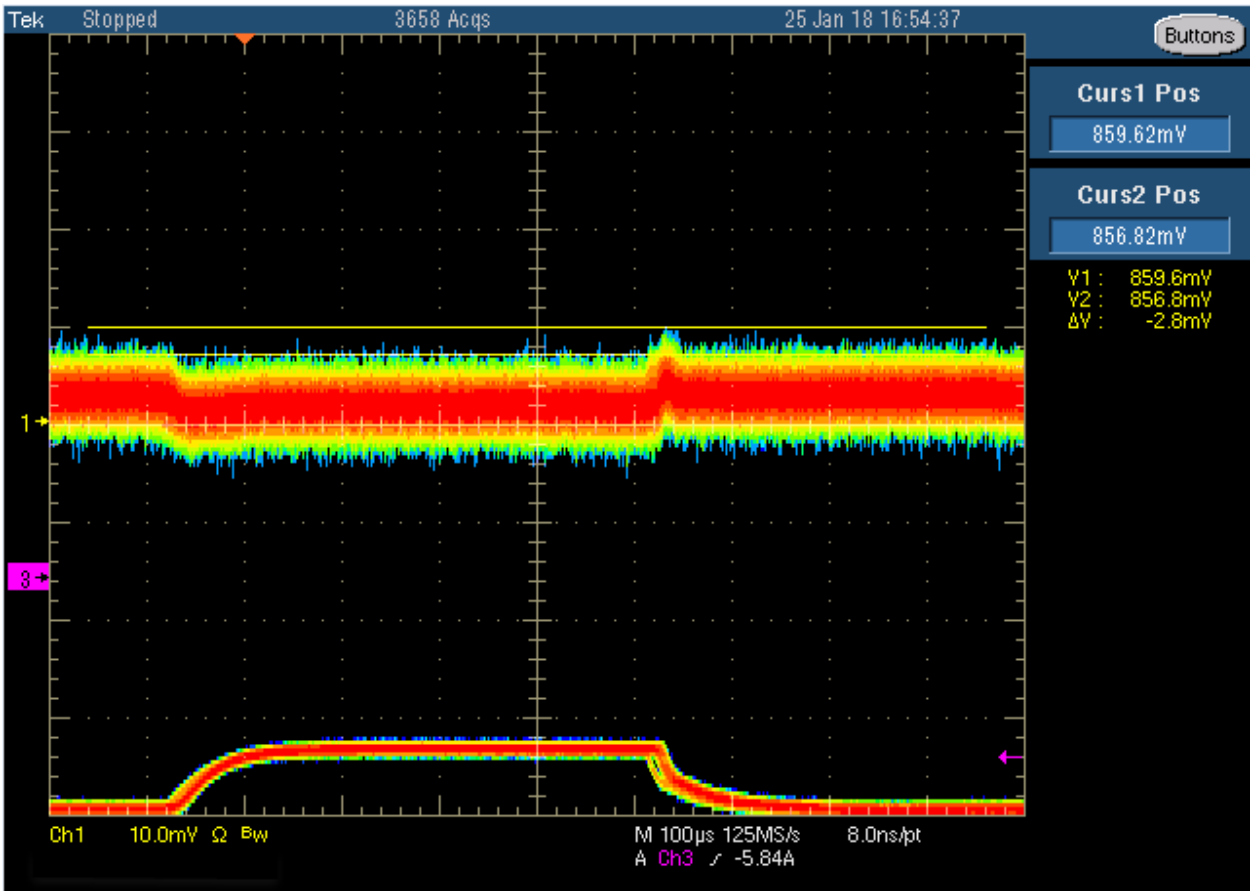


Figure 25 - MGTRAVCC ac ripple release

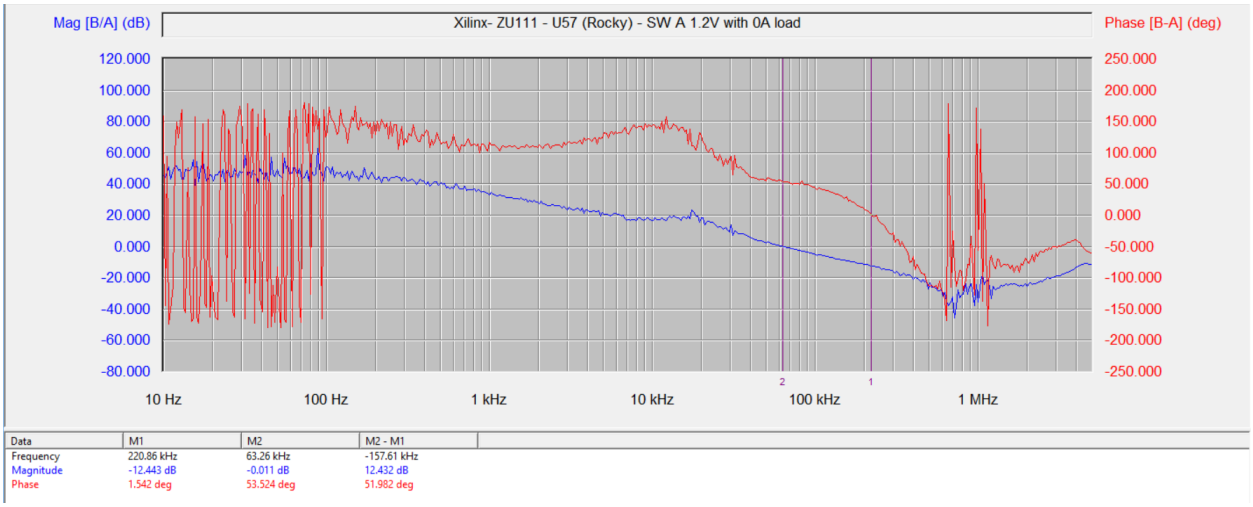
VCC1V2

Vin, 12V
Vout, 1.2V
Iout(pk), 6.0A
Istep, 3.0A
Iramp, 1A/uS

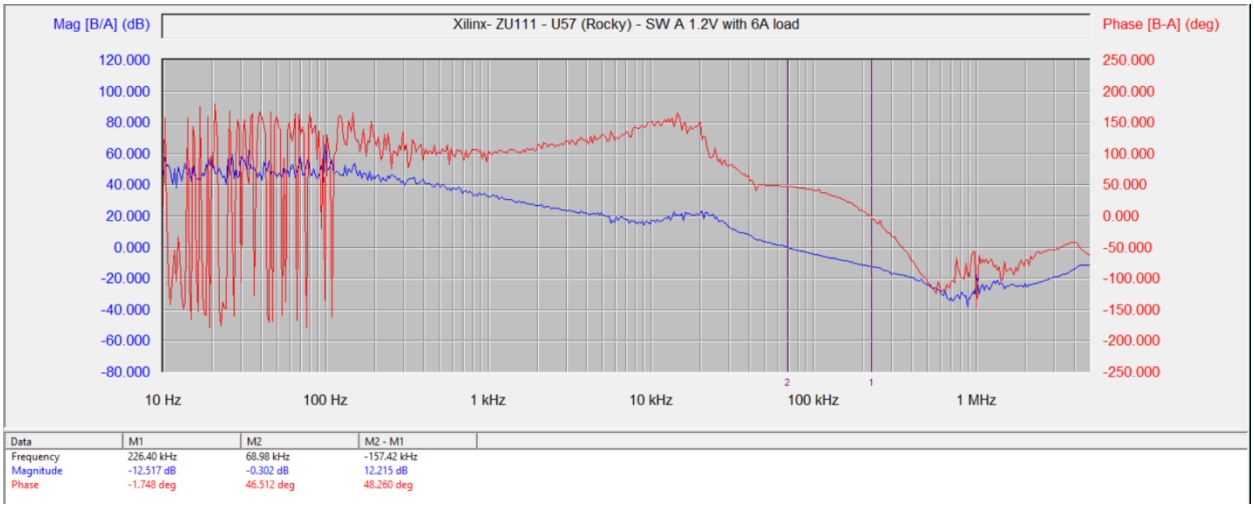
Vout Measurement Location, J74, C101, C107, C108
Load Test Location, J74
SW Node Measurement Location, L30

Jitter = 26ns (6A load)

Bode Analysis



With 0A load, the crossover frequency is around 63.26kHz and phase margin of 53.5 deg with Gain Margin of -12dB



With 6A Load, the crossover frequency is around 69 kHz and Phase Margin is 46.5 deg with Gain Margin of -12.5dB

Config: IRPS5401MXI04TRP_MTPplus7_1.2V_2.5V_1.8V_1.8V_800k_Rev2_2.txt

Table 11 – VCC1V2 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.197V	Pass	0A 6A	DMM
DC Ripple	10.4mV 10.4mV	Pass	0A 6A	Active probe
Isense	0.0A 3.0A 5.9A	Pass	0.0A 3.0A 6.0A	Telemetry/E-load
Vac(droop)	16.4mV	Pass	3.0A to 6.0A	
Vac(overshoot)	19.0mV	Pass	6.0A to 3.0A	

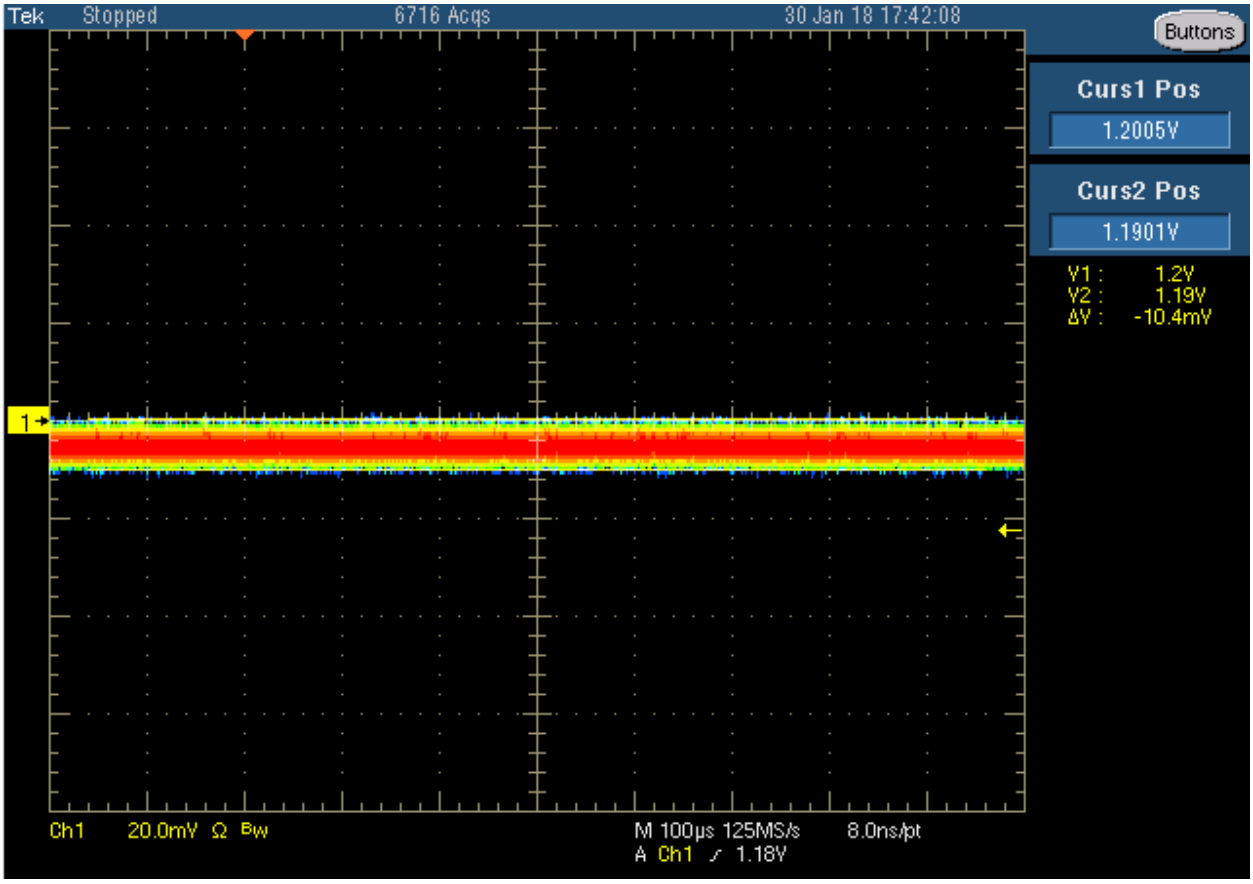


Figure 26 - VCC1V2 DC Ripple, 5A

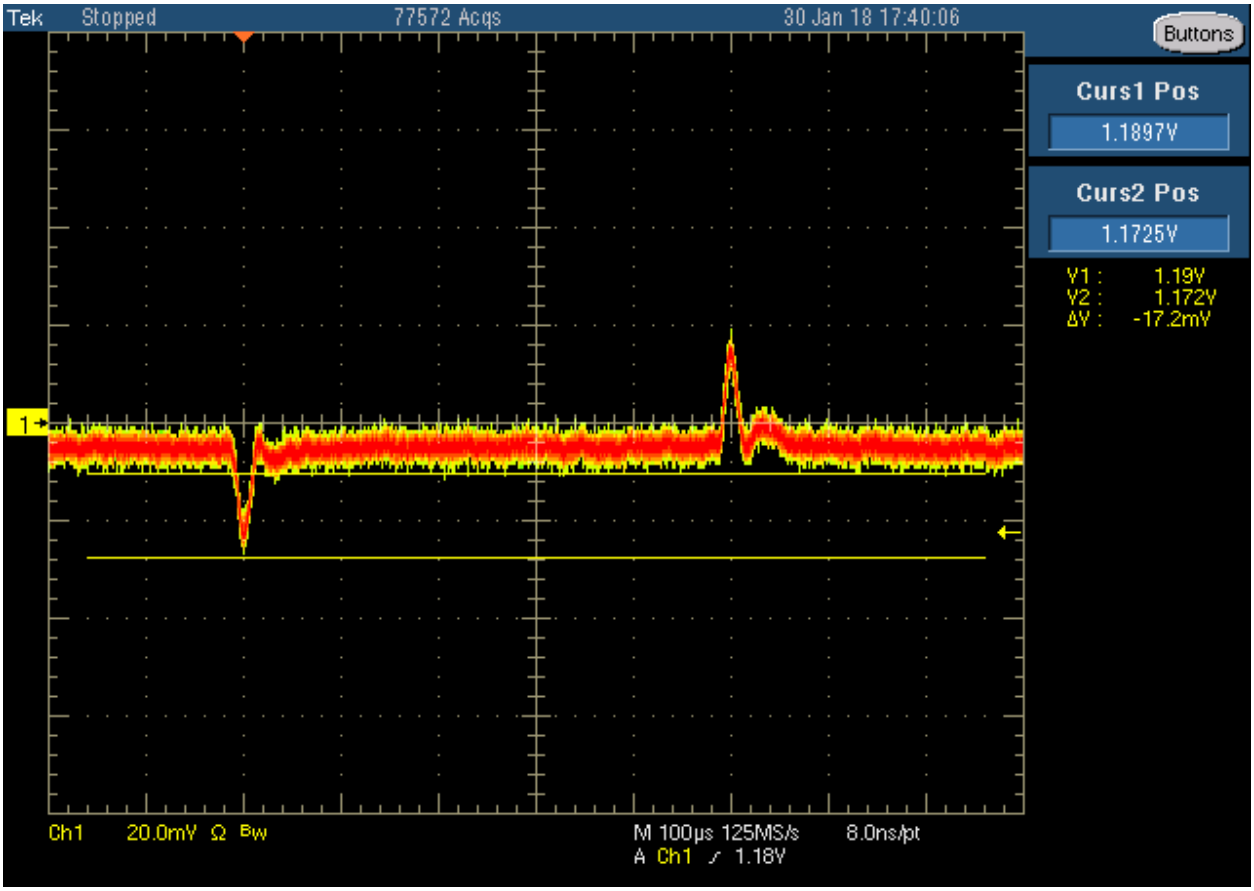


Figure 27 - VCC1V2 ac ripple load

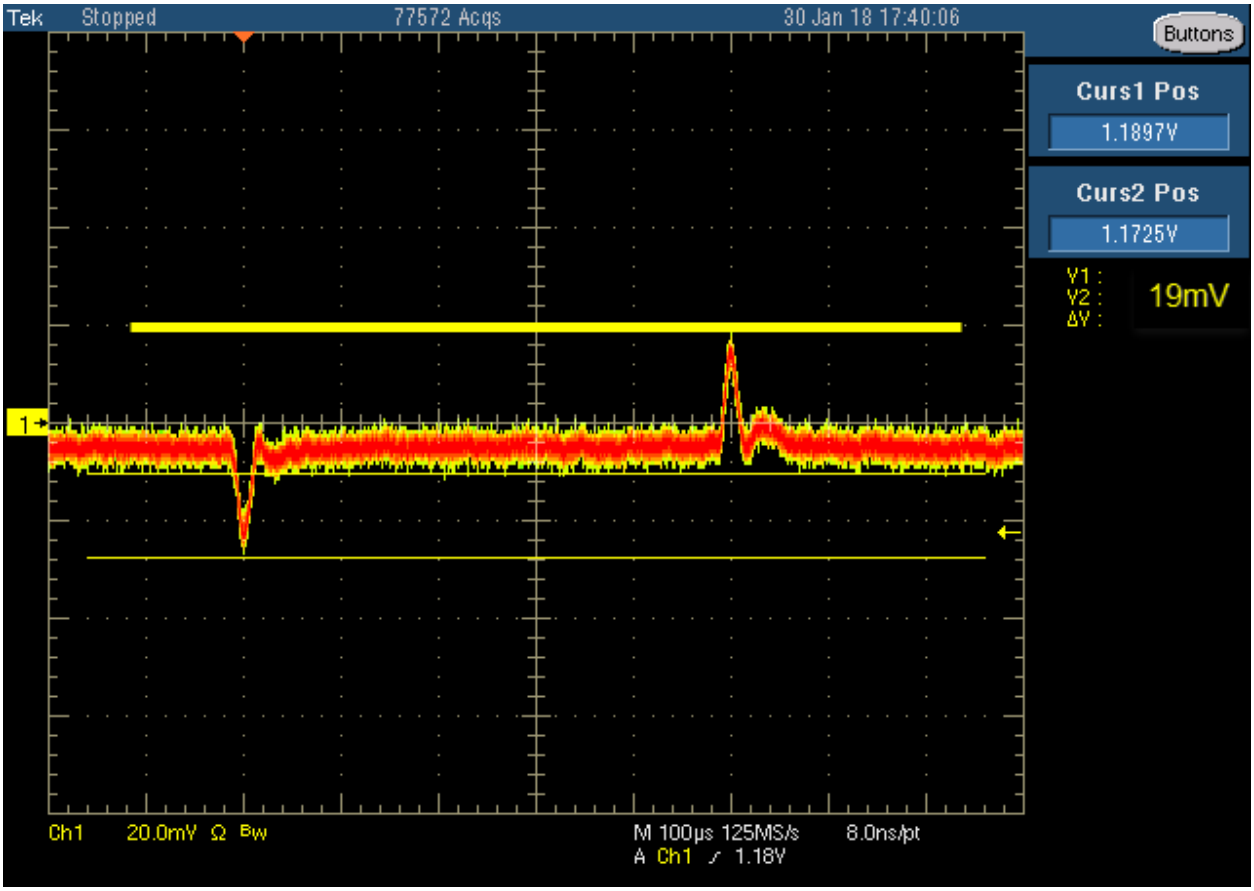


Figure 28 - VCC1V2 ac ripple release

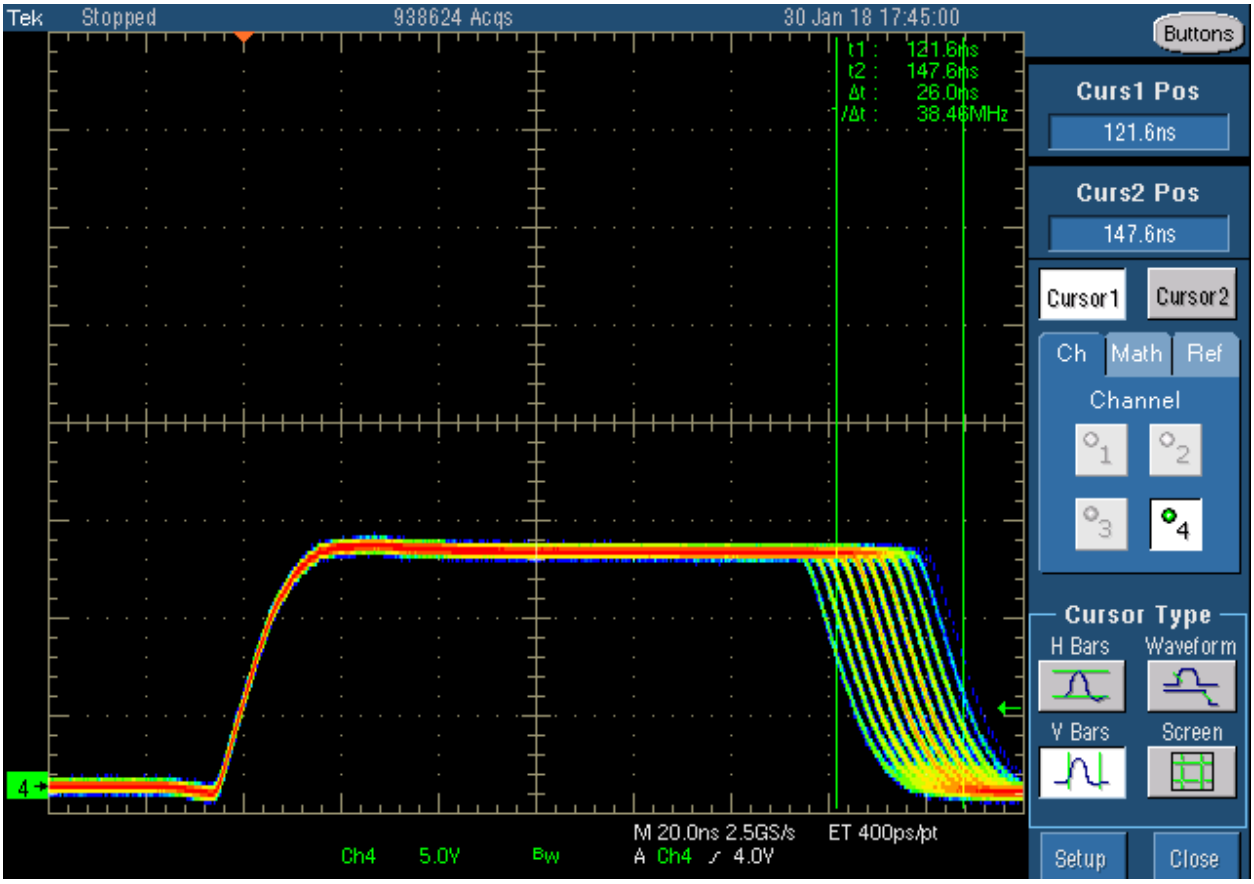


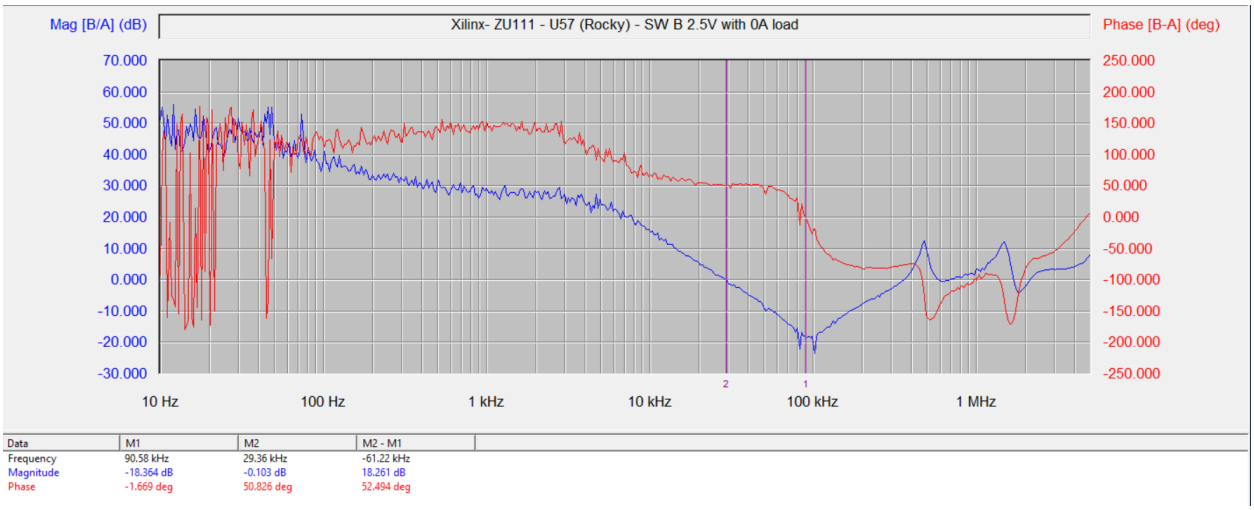
Figure 29 - VCC1V2 Jitter, 5A

DAC_AVTT

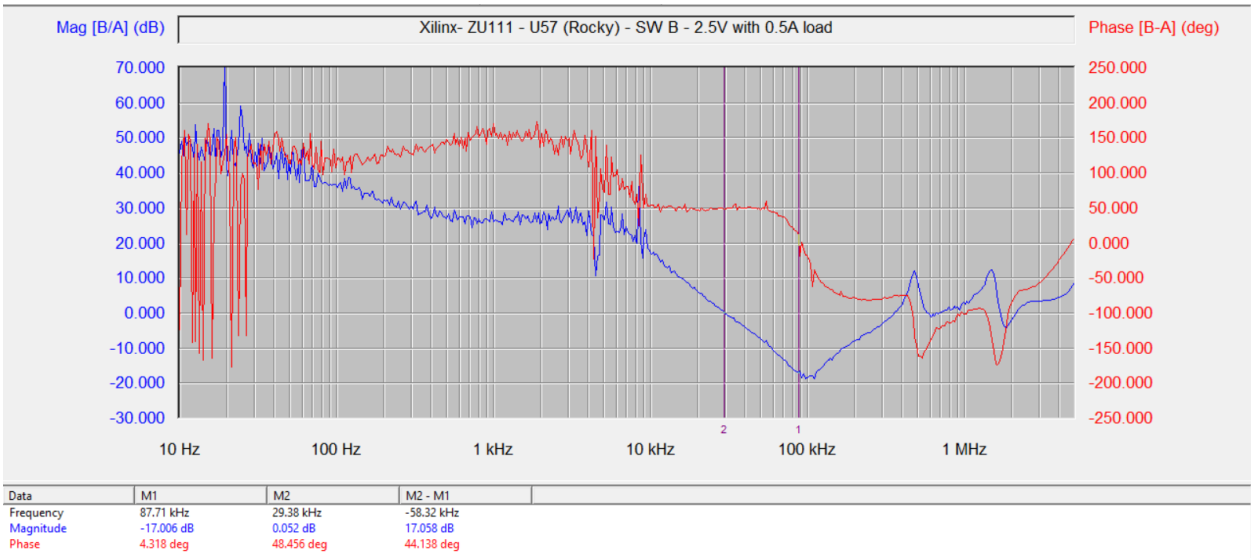
Vin, 12V
Vout, 3.0V/2.5V
Iout(pk), 0.5A
Istep, 0.5A
Iramp, 1A/uS

Vout Measurement Location, J71, C145, C146, C143, C144
Load Test Location, J71
SW Node Measurement Location, L27
Jitter = 31.2ns (6A load)

Bode Analysis



With 0A load, the crossover frequency is around 29.36kHz with 50.86 deg Phase Margin and Gain Margin of -18.3dB



With 500mA of load current, the crossover frequency is around 29.38kHz with 48.5deg Phase Margin and Gain Margin of -17dB

Config: IRPS5401MXI04TRP_MTPplus7_1.2V_2.5V_1.8V_1.8V_800k_Rev2_2.txt

Table 12 – DAC_AVTT Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	2.508V	Pass	0A 0.5A	DMM
DC Ripple	4.8mV 7.4mV	Pass	0A 0.5A	Coax
Isense	0A 0.52A	Pass	0.0A 0.5A	Telemetry/E-load
Vac(droop)	17.2mV	Pass	0A to 0.5A	
Vac(overshoot)	24.0mV	Pass	0.5A to 0A	

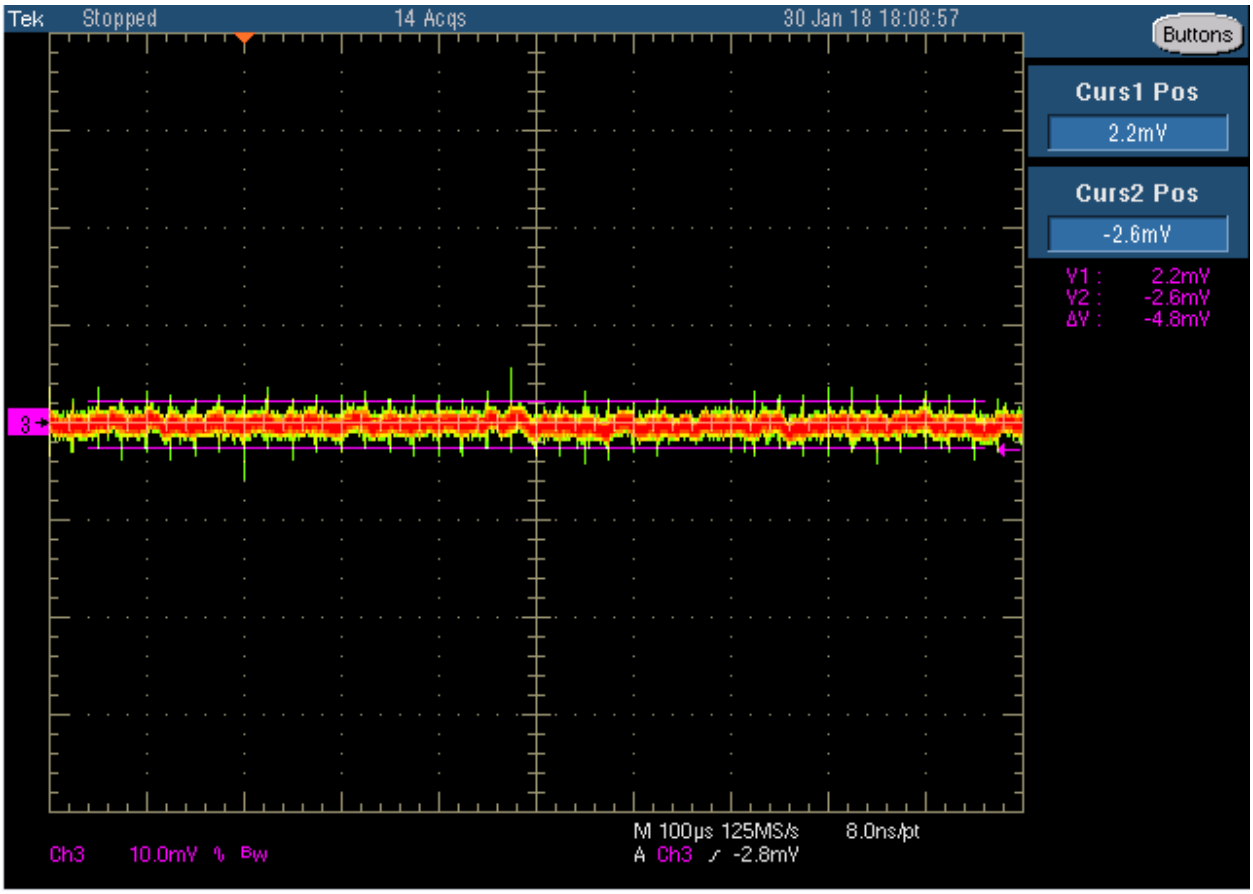


Figure 30 - DAC_AVTT DC Ripple, 0.5A

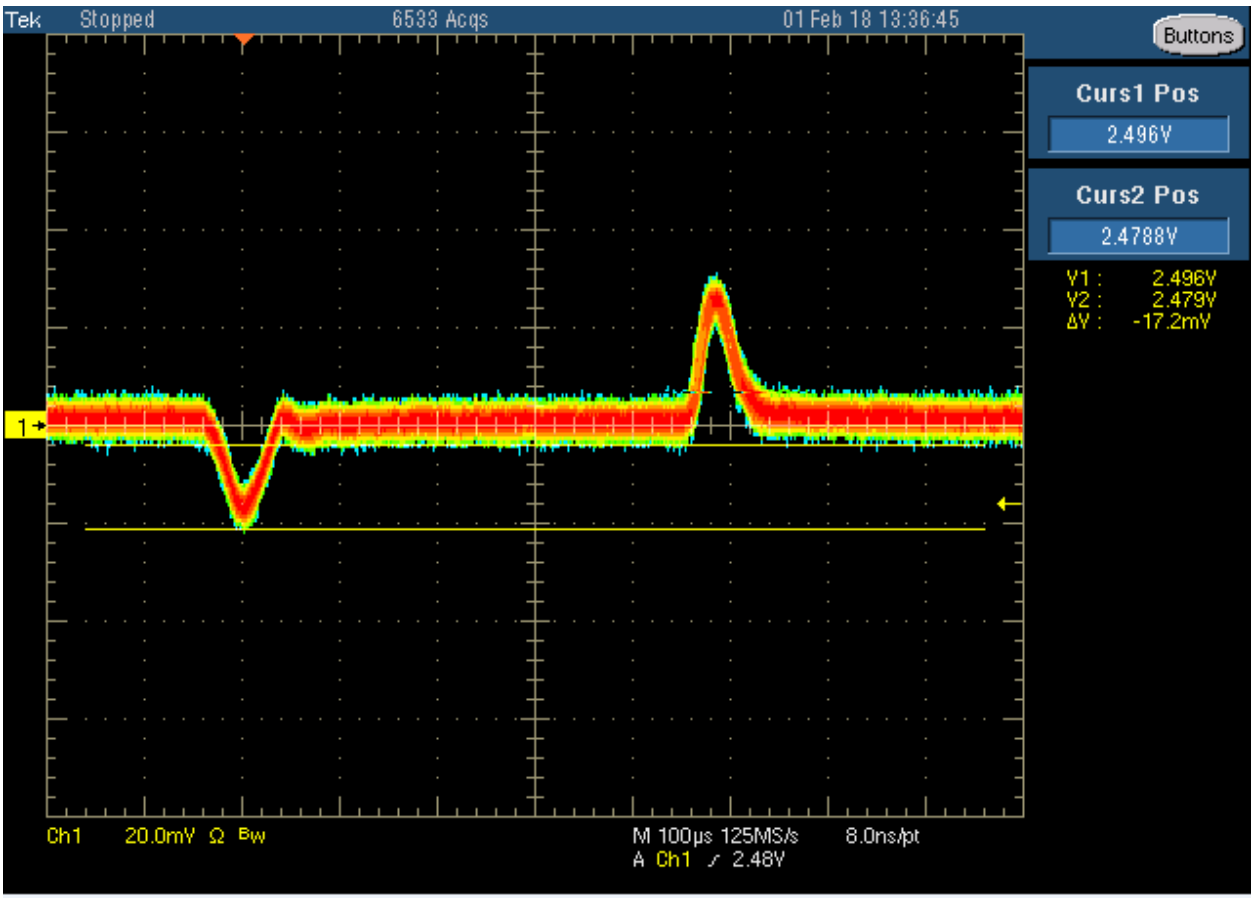


Figure 31 - DAC_AVTT ac ripple load

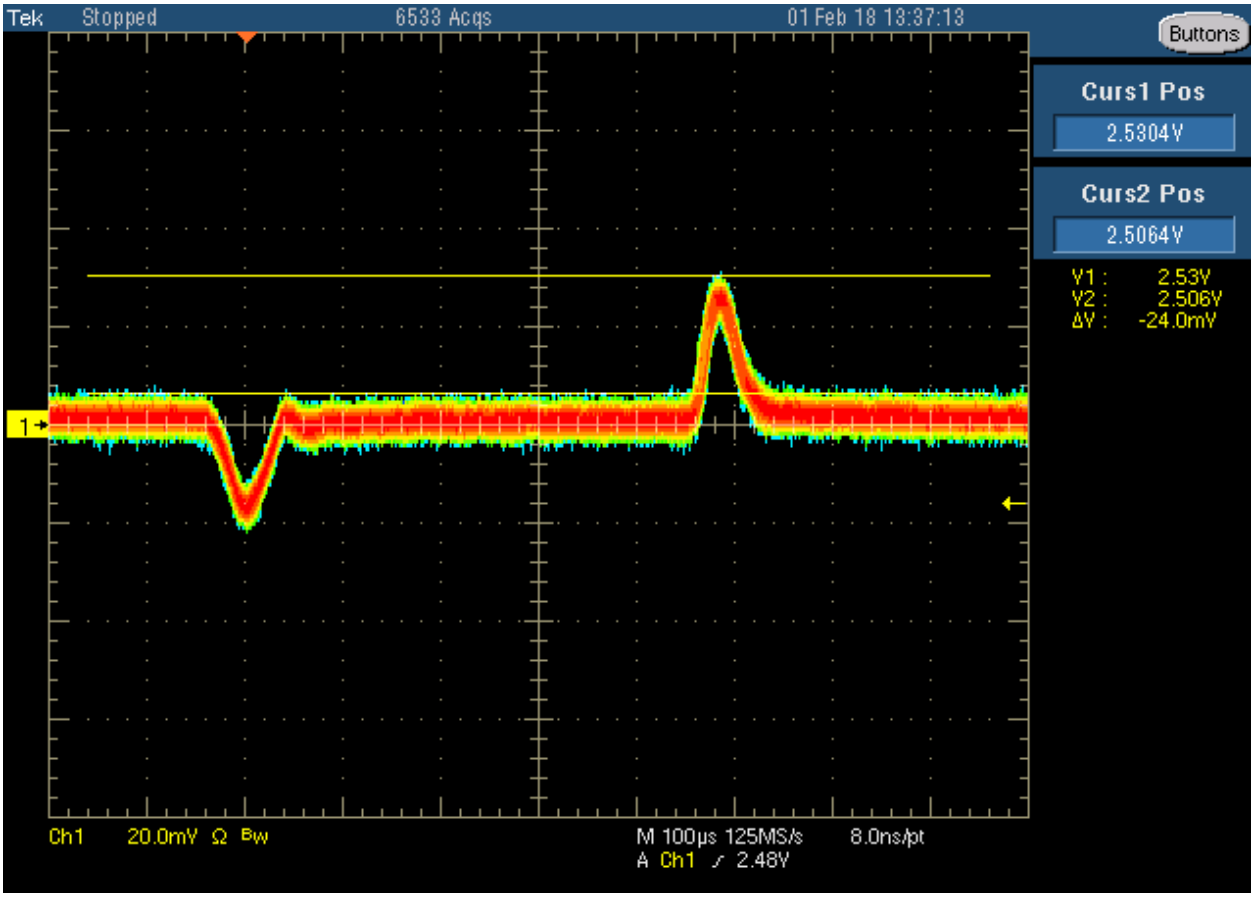


Figure 32 - DAC_AVTT ac ripple release

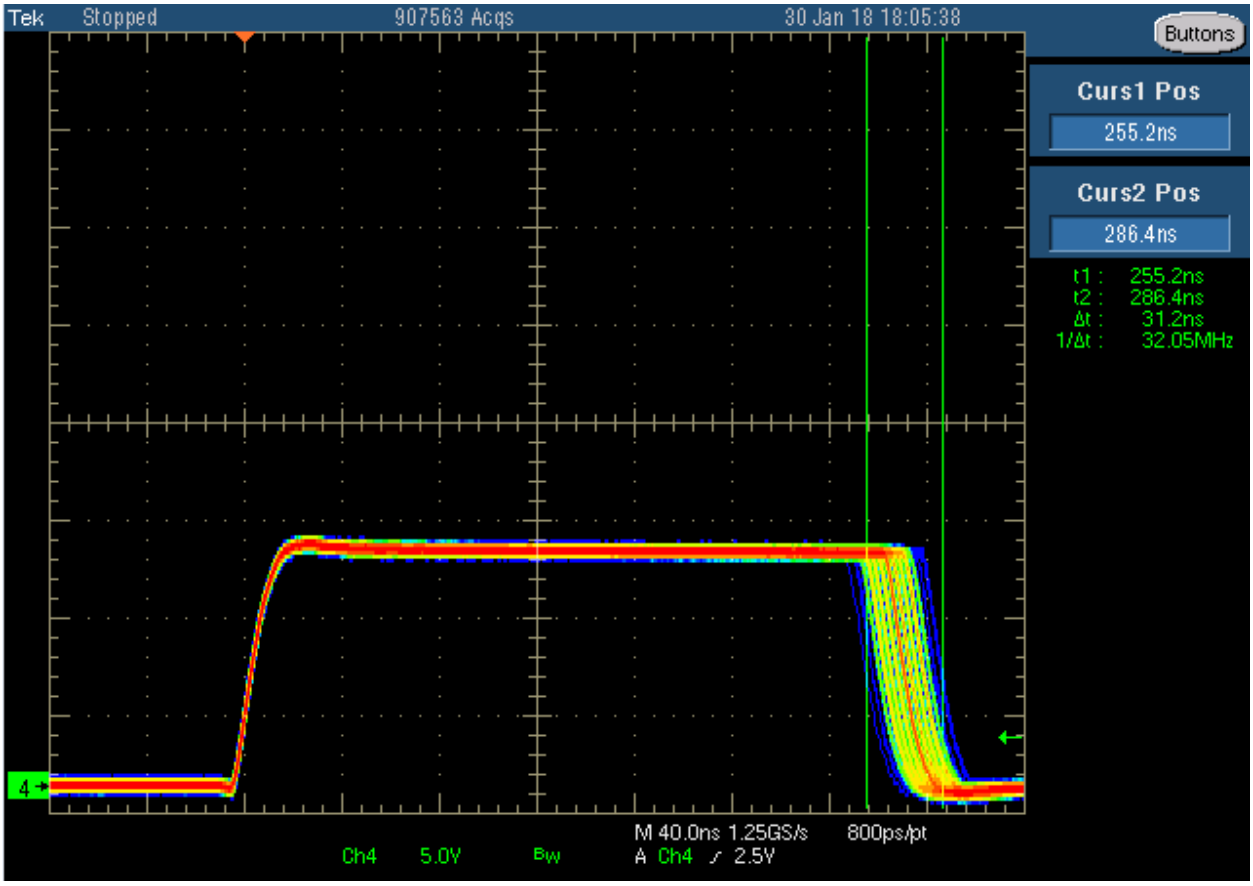


Figure 33 - DAC_AVTT Jitter, 0.5A

FMC_VADJ

Vin, 12V

Vout, 1.8V

Iout(pk), 5A

Istep, 2A

Iramp, 1A/us

Vout Measurement Location, J72, C96, C97, C98, C287 (BUS side)

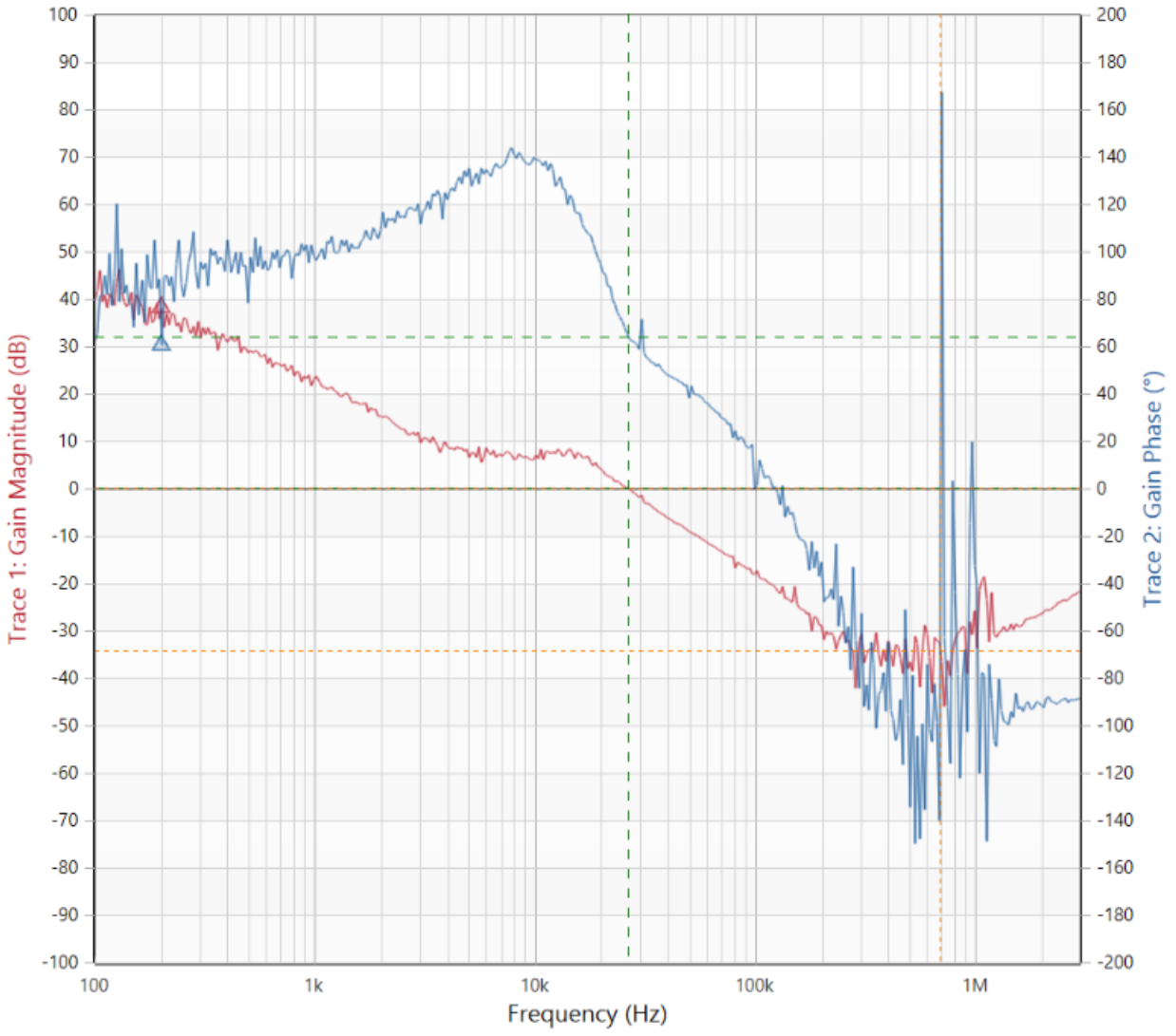
Load Test Location, J72

SW Node Measurement Location, L28, L29

Jitter = 32.8ns (5A load)

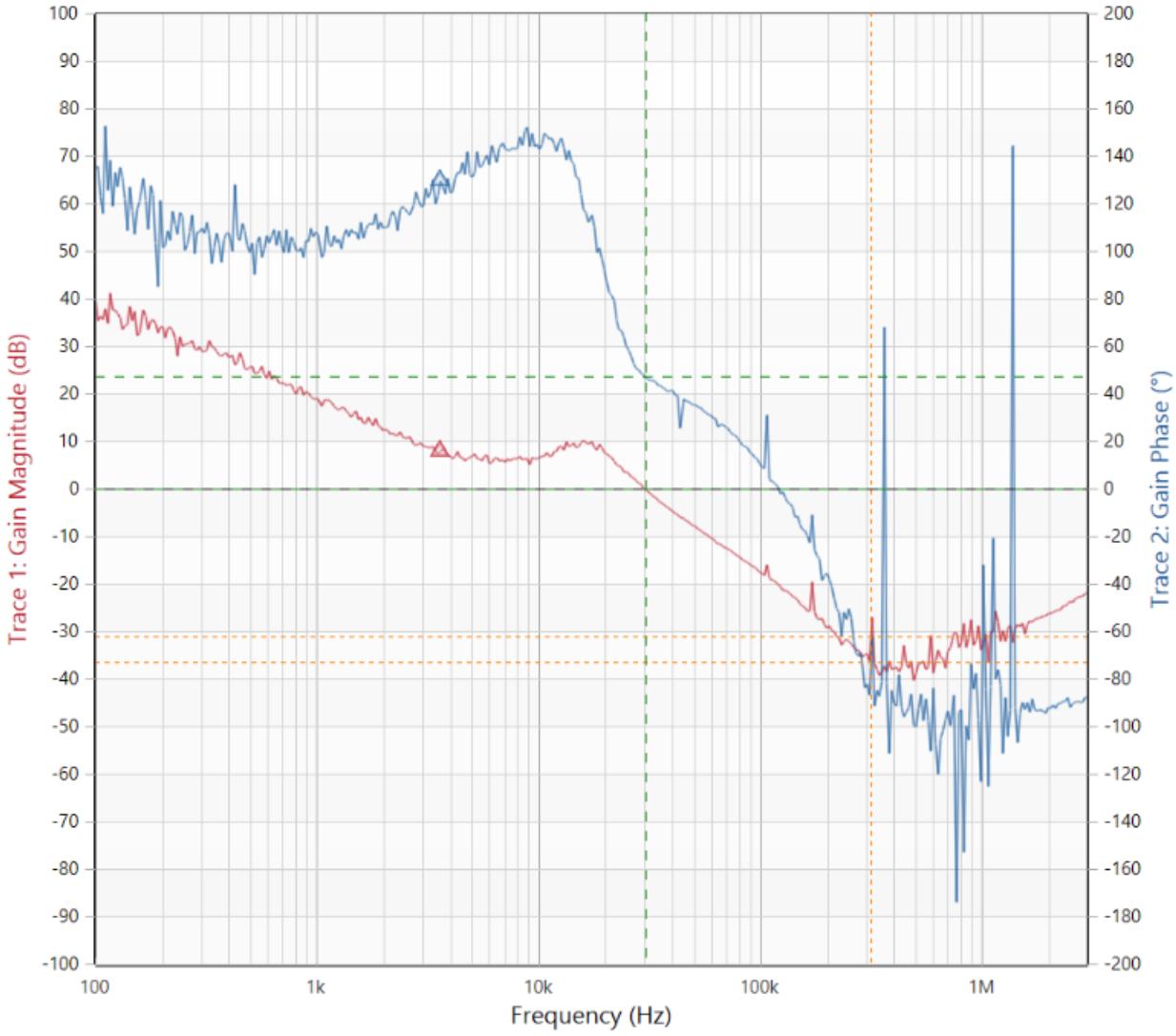
Bode Analysis

	Frequency	Trace 1	Trace 2
Cursor 1	26.644 kHz	0 dB	63.854 °
Cursor 2	698.591 kHz	-34.205 dB	-1.961 p°
Delta C2-C1	671.946 kHz	-34.205 dB	-63.854 °



With 0A load, the crossover frequency is 26.6kHz and phase margin is 63.9 deg with Gain Margin around -34dB

	Frequency	Trace 1	Trace 2
Cursor 1	30.333 kHz	-119.128 mdB	47.024 °
Cursor 2	314.843 kHz	-31.233 dB	-73.267 °
Delta C2-C1	284.509 kHz	-31.114 dB	-120.29 °



With 5A load, the crossover frequency is 30.33kHz and phase margin is around 47deg and Gain Margin is around –31.3dB.

Config: IRPS5401MXI04TRP_MTPplus7_1.2V_2.5V_1.8V_1.8V_800k_Rev2_2.txt

Table 13 – FMC_VADJ Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.81V	Pass	0A	DMM

			5A	
DC Ripple	56mV 80mV	Pass	0A 5A	Active probe
Isense	0A 4.98A	Pass	0A 5A	Telemetry/E-load
Vac(droop)	108mV	Pass	3A to 5A	
Vac(overshoot)	68mV	Pass	5A to 3A	

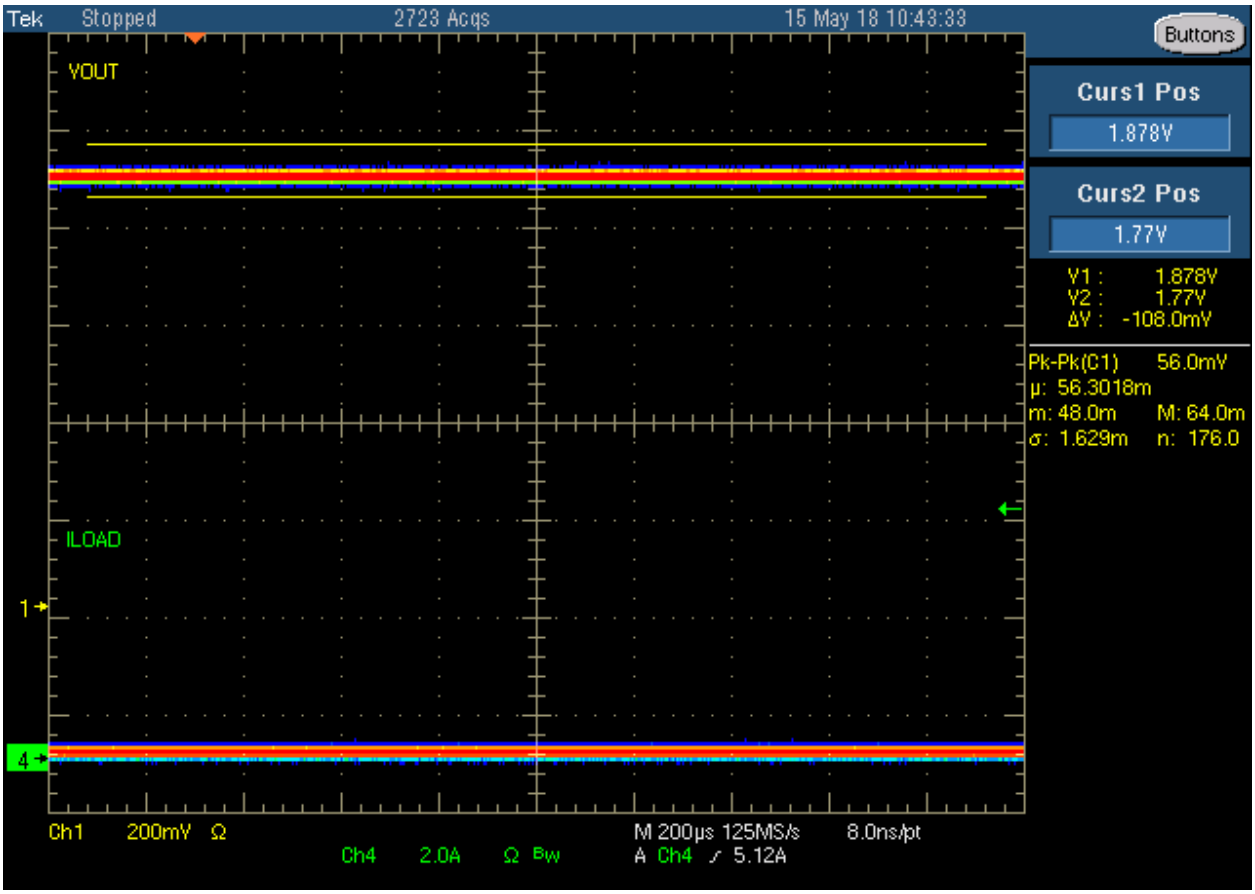


Figure 34 - FMC_VADJ DC Ripple, 0A: The ripple voltage is around 56mV

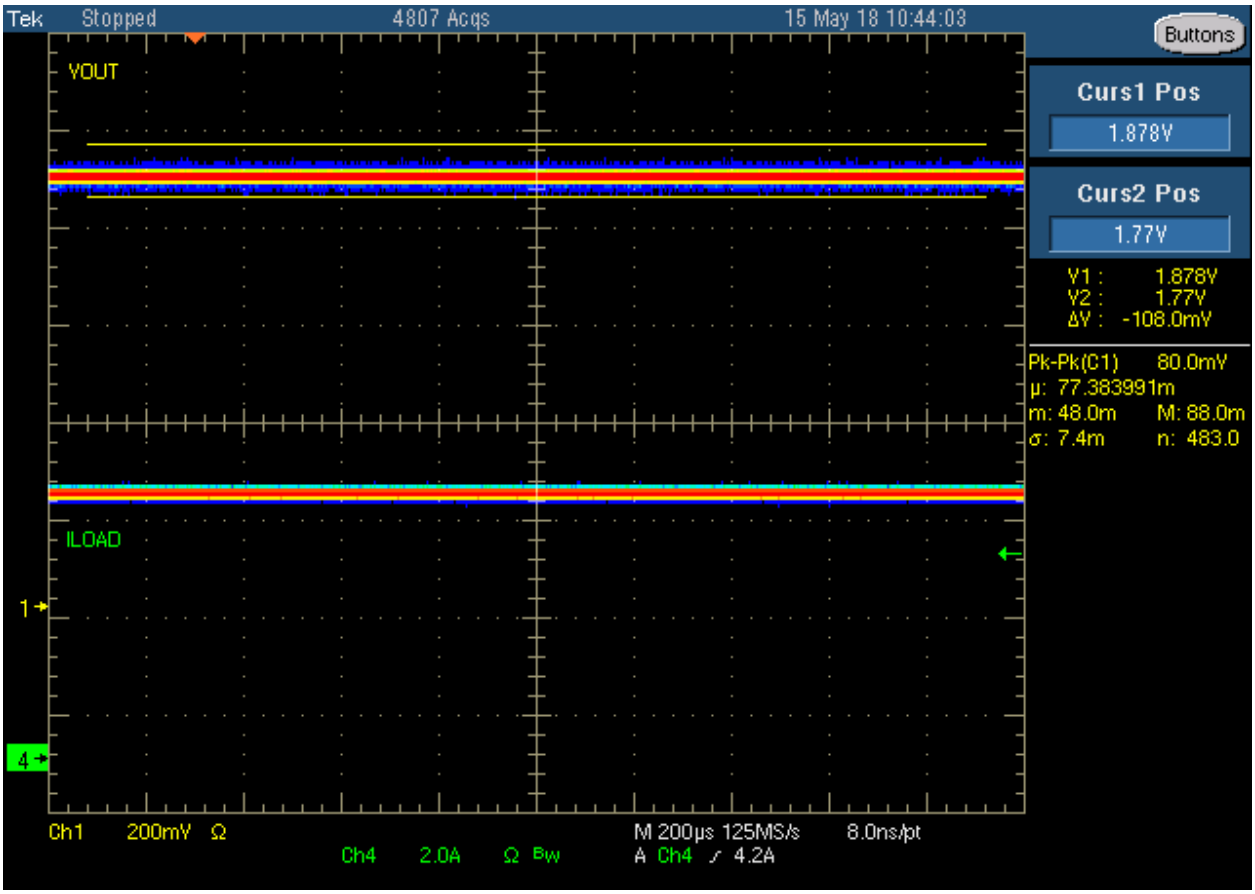


Figure – FMC_VADJ: Vout ripple with 5A load is around 80mV

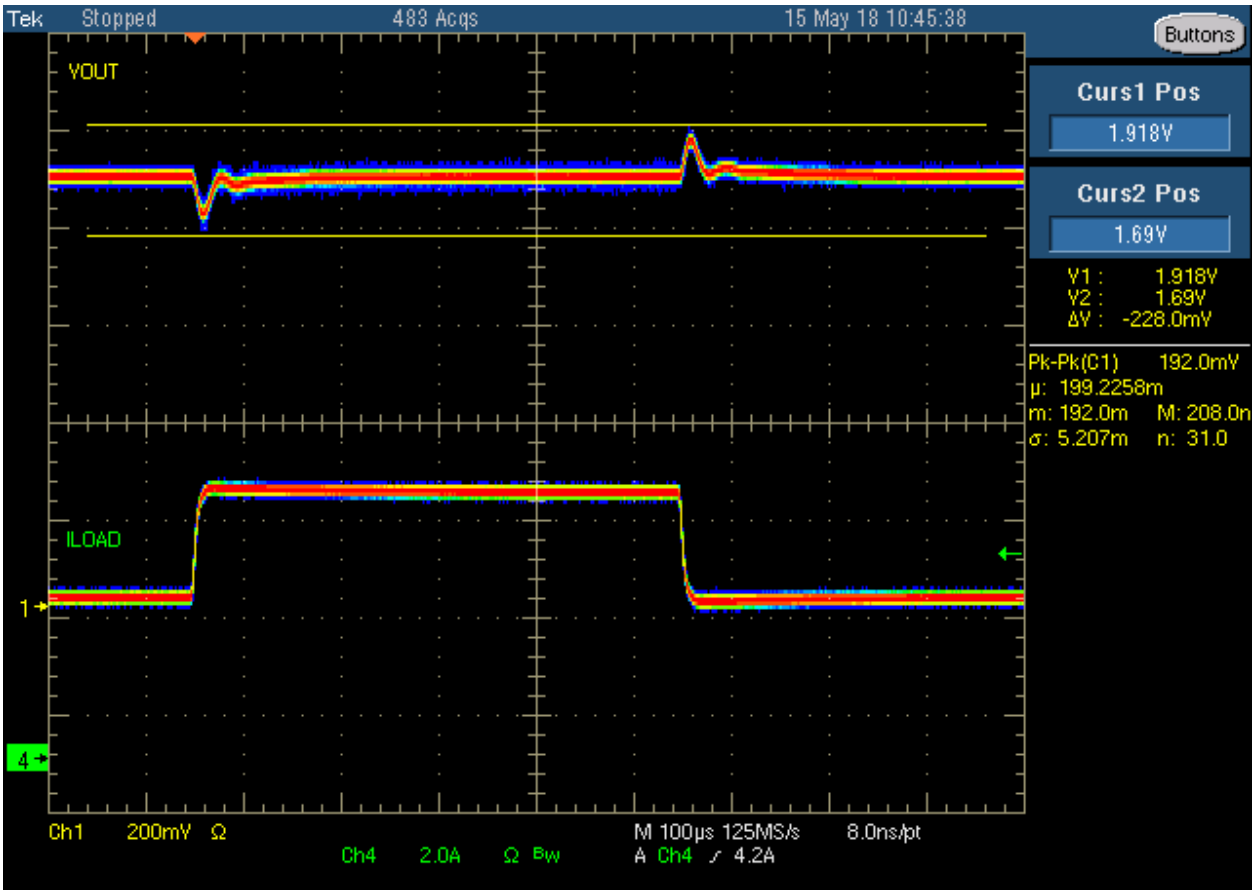


Figure 35 - FMC_VADJ Transient load response during 3-5A load step is around 192mV

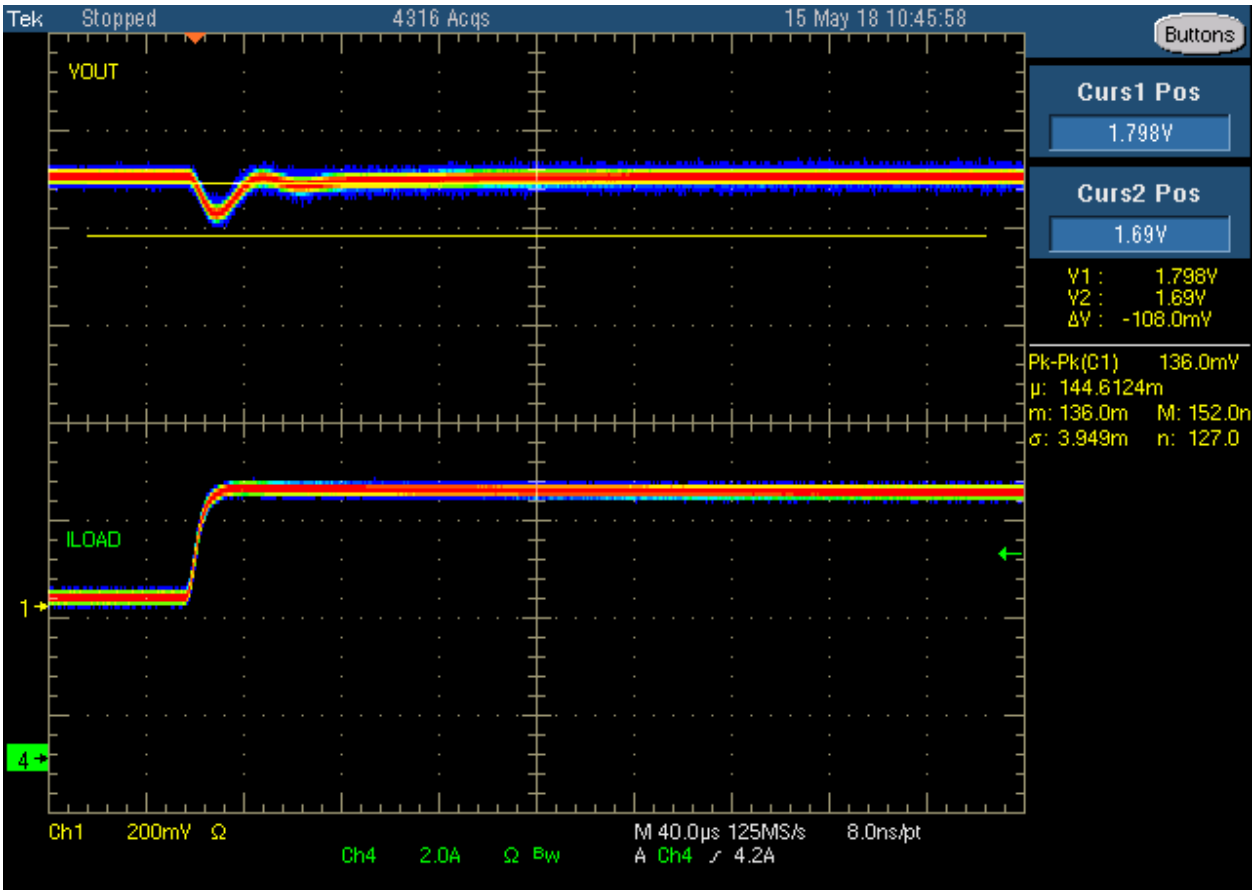


Figure 36 - FMC_VADJ transient load step: Vout excursion is around 108mV

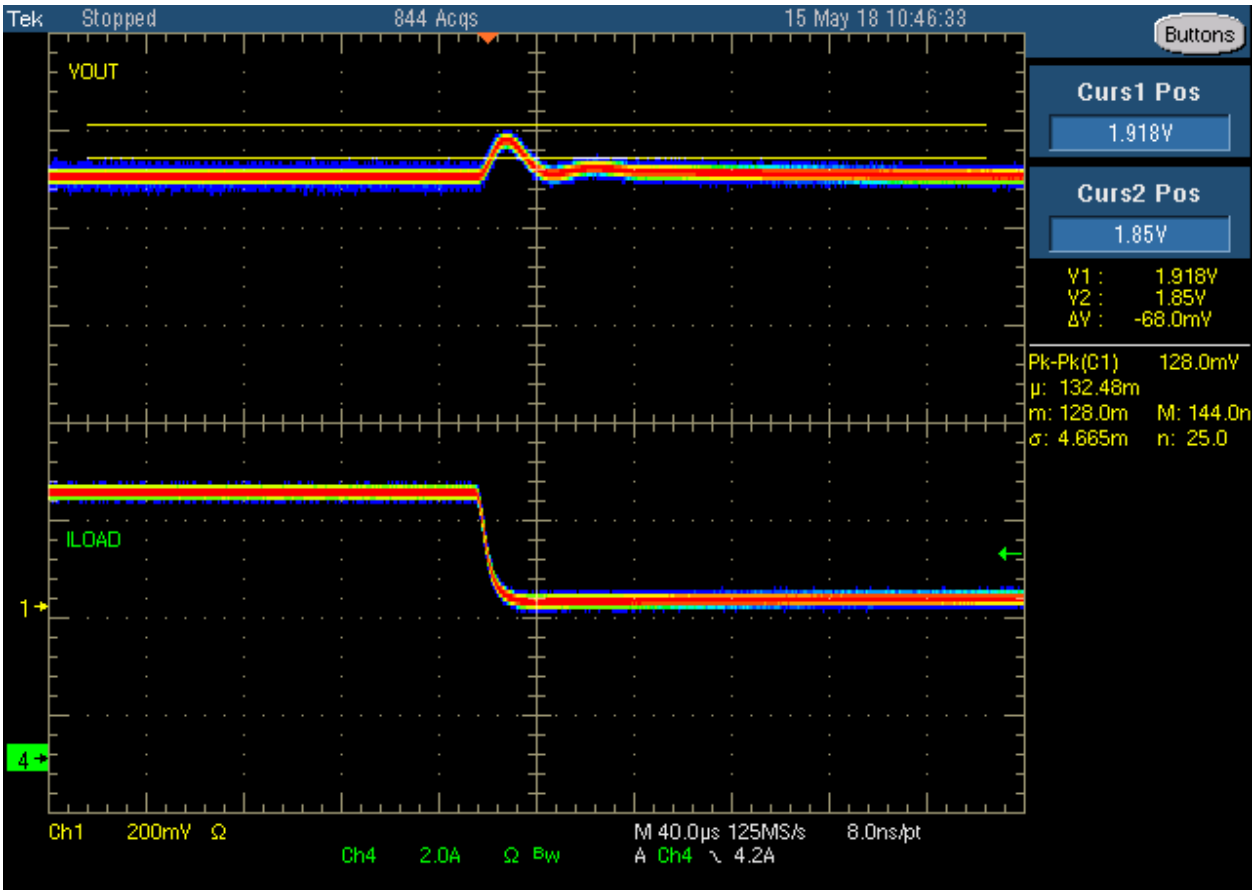


Figure 37 - FMC_VADJ Transient load release Vout overshoot is around 68mV

MGT1V8

Vin, 2.5V
Vout, 1.8V
Iout(pk), 0.5A
Istep, 0.5A
Iramp, 1A/us

Vout Measurement Location, J41, C944
Load Test Location, J41

Config: IRPS5401MXI04TRP_MTPplus7_1.2V_2.5V_1.8V_1.8V_800k_Rev2_2.txt

Table 14 – MGT1V8 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.797V 1.794V	Pass	0A 0.5A	DMM
DC Ripple	4.8mV 4.8mV	Pass	0A 0.5A	Coax
Isense	0.0A 0.5A	Pass	0A 0.5A	Telemetry/Eload
Vac(droop)	18.8mV	Pass	0A to 0.5A	
Vac(overshoot)	12.8mV	Pass	0.5A to 0A	

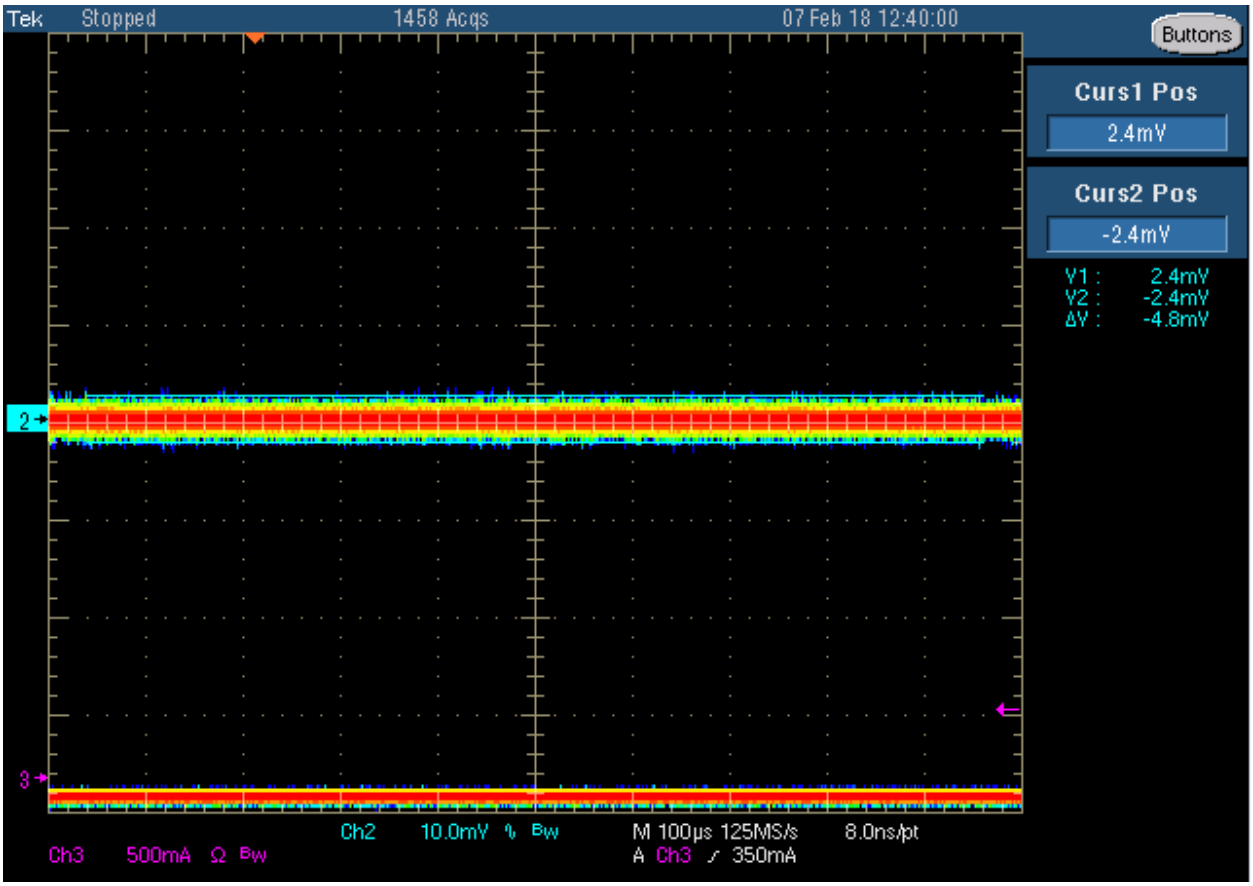


Figure 38 - MGT1V8 DC Ripple, 0.5A

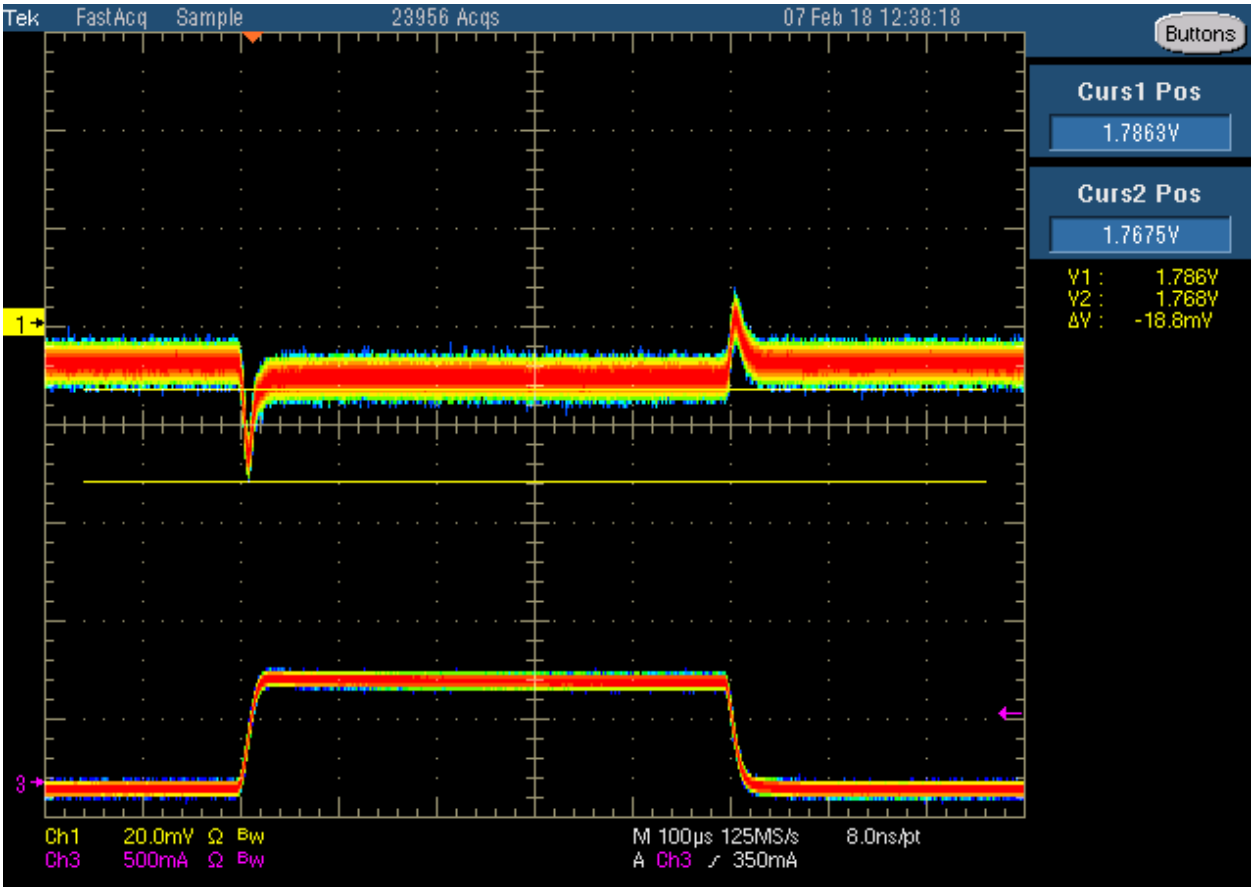


Figure 39 - MGT1V8 ac ripple load

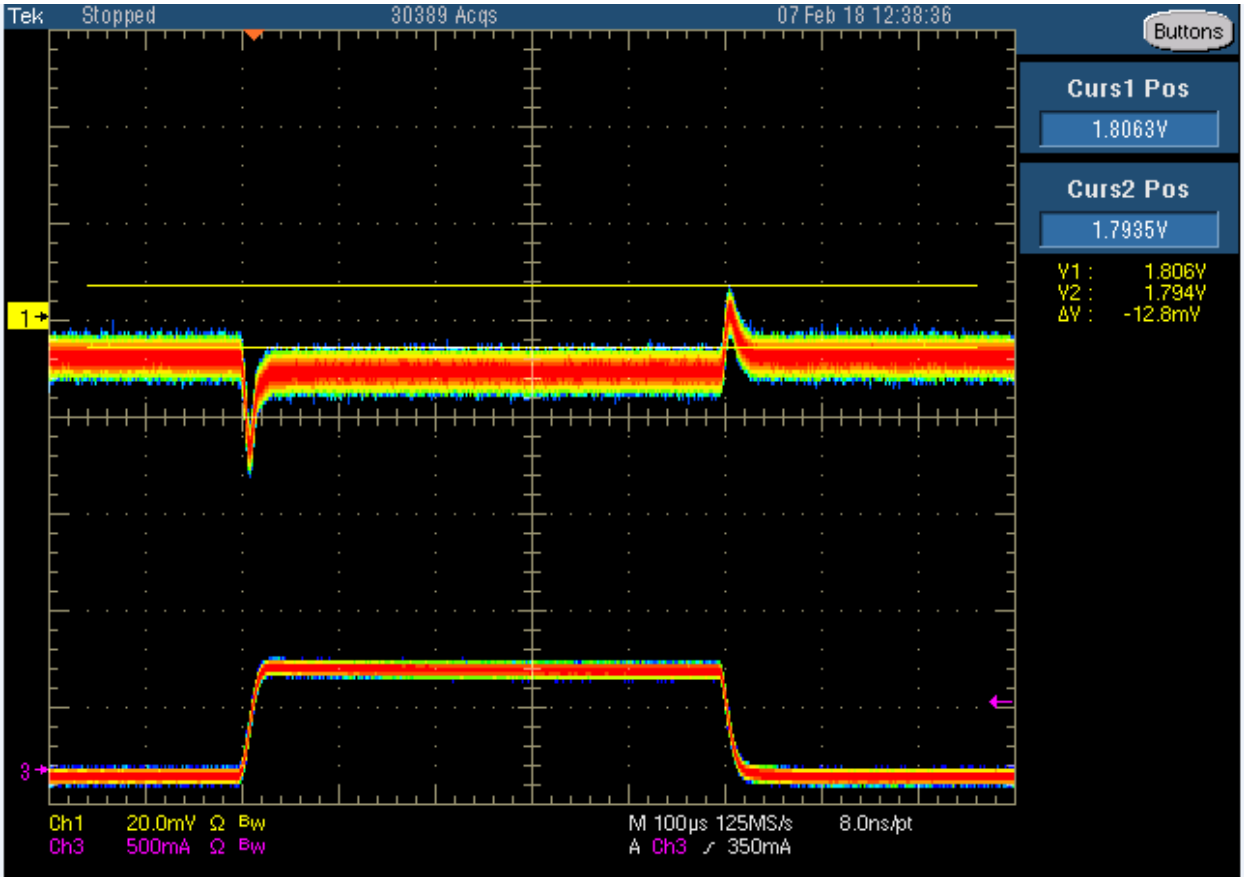


Figure 40 - MGT1V8 ac ripple release

VCCINT

Vin, 12V
Vout, 0.85V
Iout(pk), 30A
Istep, 7.5A (12.5A to 20A)
Iramp, 2A/us

Vout Measurement Location, J76, C51, C52, (or BGA pad where FPGA not populated)
Load Test Location, J76
SW Node Measurement Location, L31

Test Needs

- ***VOUT_OV_WARN is persistent. This is being investigated.***

Table 15 – VCCINT Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.8526V 0.8527V 0.8543V	Pass	0A 15A 30A	DMM At load
DC Ripple	14.4mV 12.82mV 13.6mV 12.4mV	Pass	0A 10A 15A 30A	Active Probe
Isense	0.0A 4.00A 9.00A 13.94 18.94 29.94A	Pass	0A 5A 10A 15A 20A 30A	Telemetry/E-load
Vac(droop)	20.8mV	Pass	12.5A to 20A	Active Probe/ E-Load
Vac(overshoot)	18.8mV	Pass	20A to 12.5A	Active Probe/ E-Load

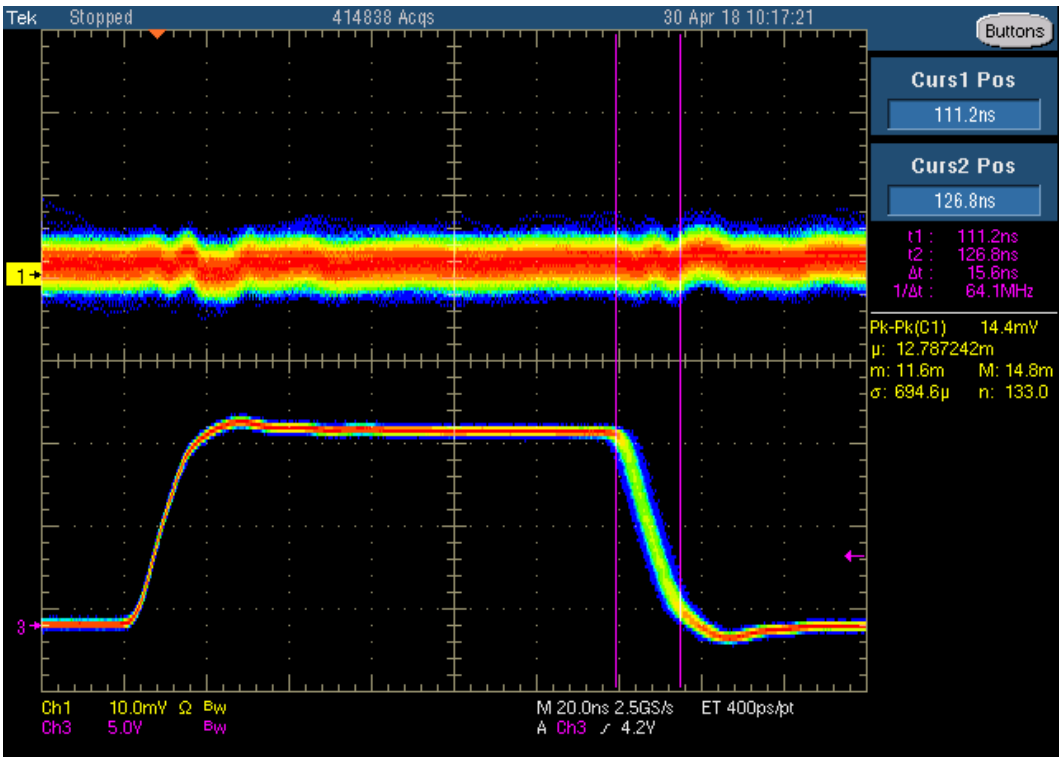


Figure – VCCINT Ripple, 0A – Jitter is around 16ns

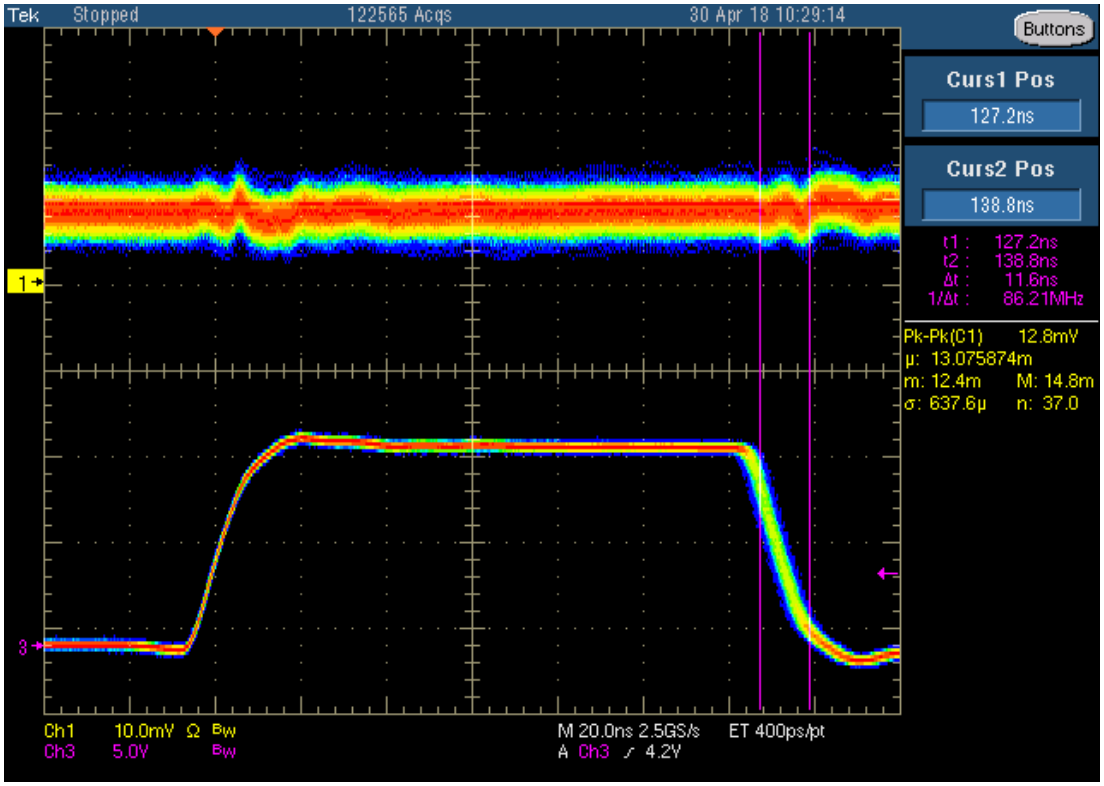


Figure – VCCINT Ripple, 10A – Jitter is around 12ns

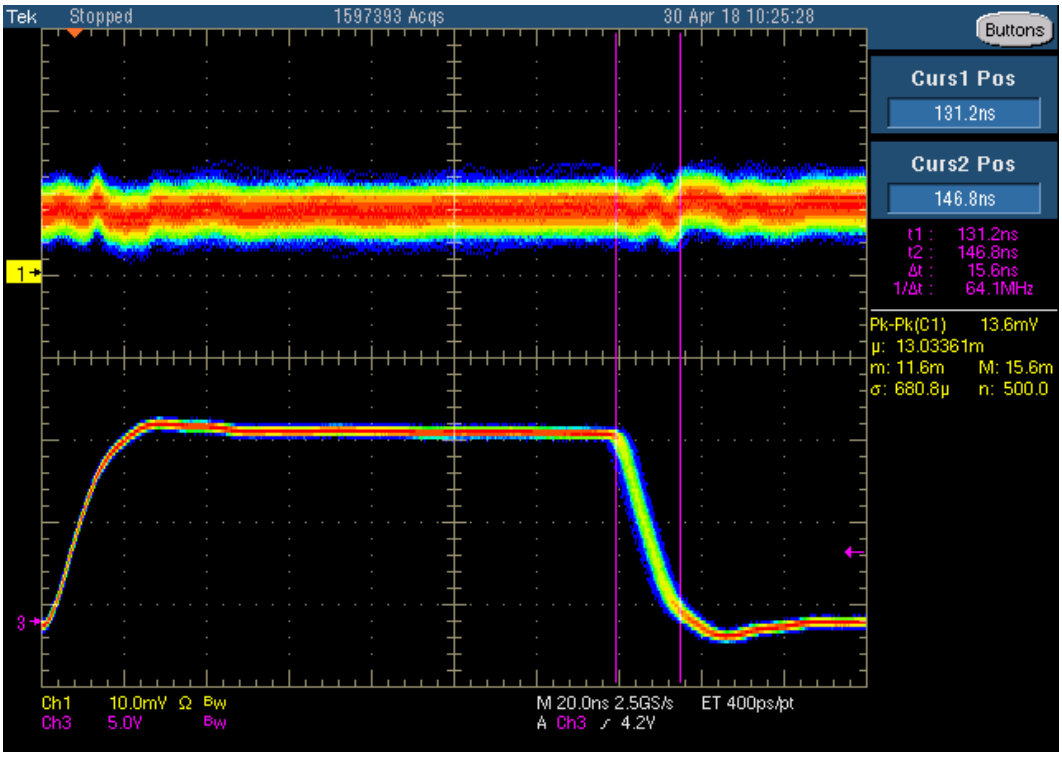


Figure 41 - VCCINT Ripple, 15A – Jitter is around 16ns

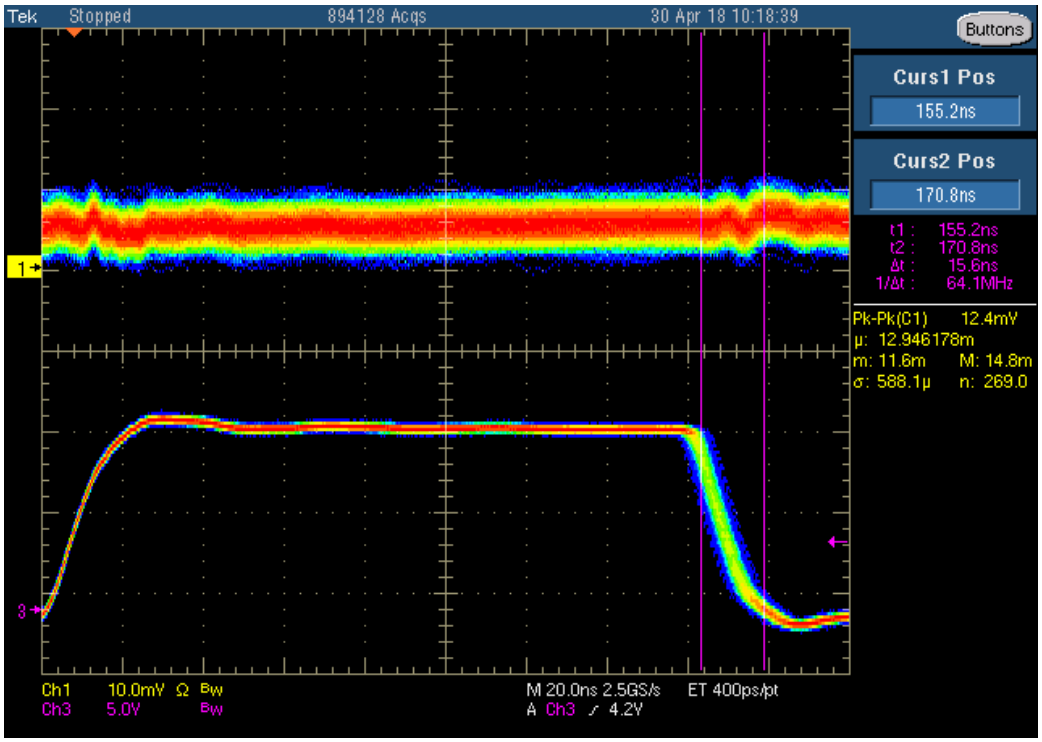


Figure 44 – VCCINT Ripple, 30A – Jitter is around 16ns

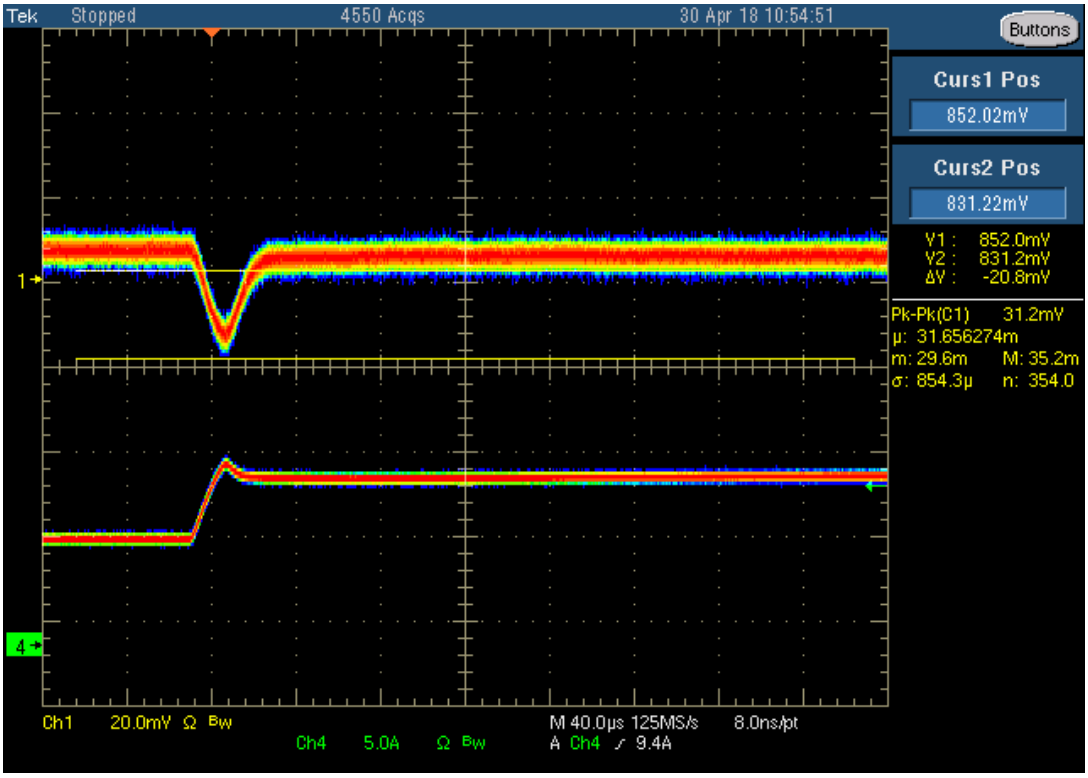


Figure 42 - VCCINT excursion during a 12.5A to 20A load step, 20.8mV

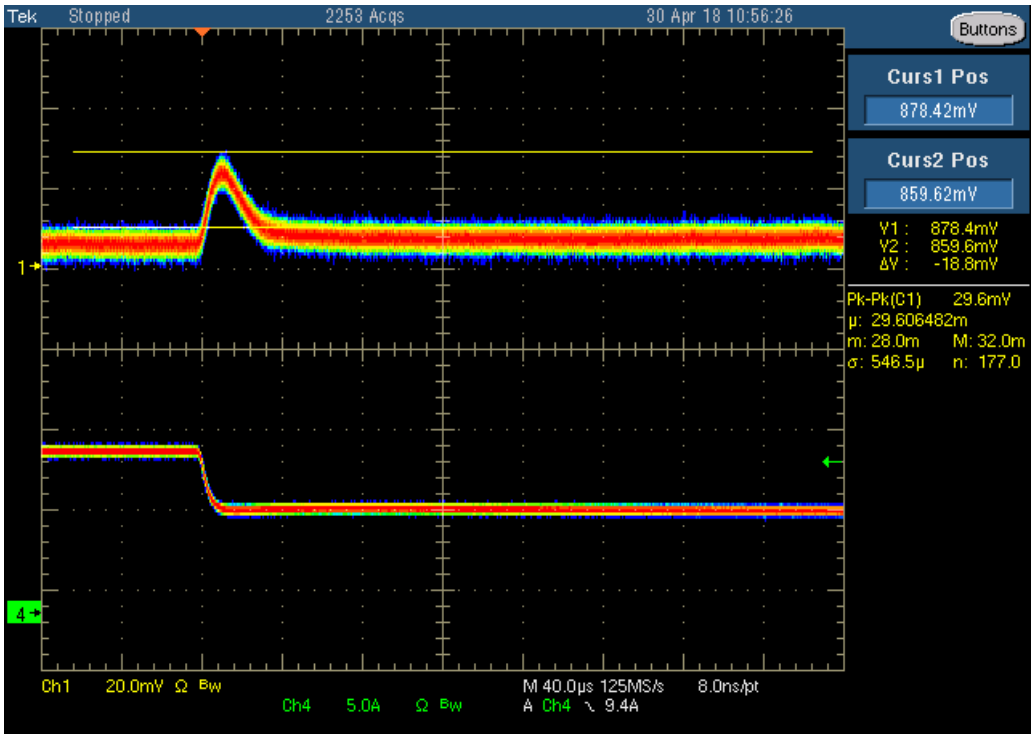


Figure 43 - VCCINT deviation during a 20A to 12.5A load release.

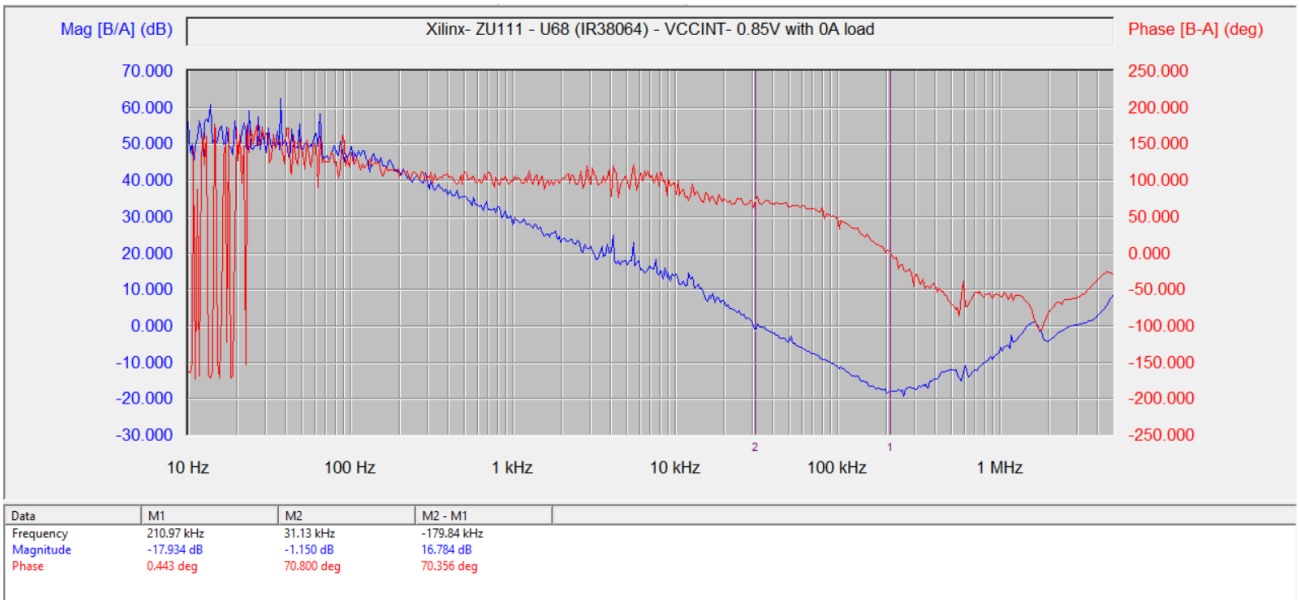


Figure – With 0A load, crossover frequency is 31.13kHz with 70 deg of Phase Margin and Gain Margin of -18dB

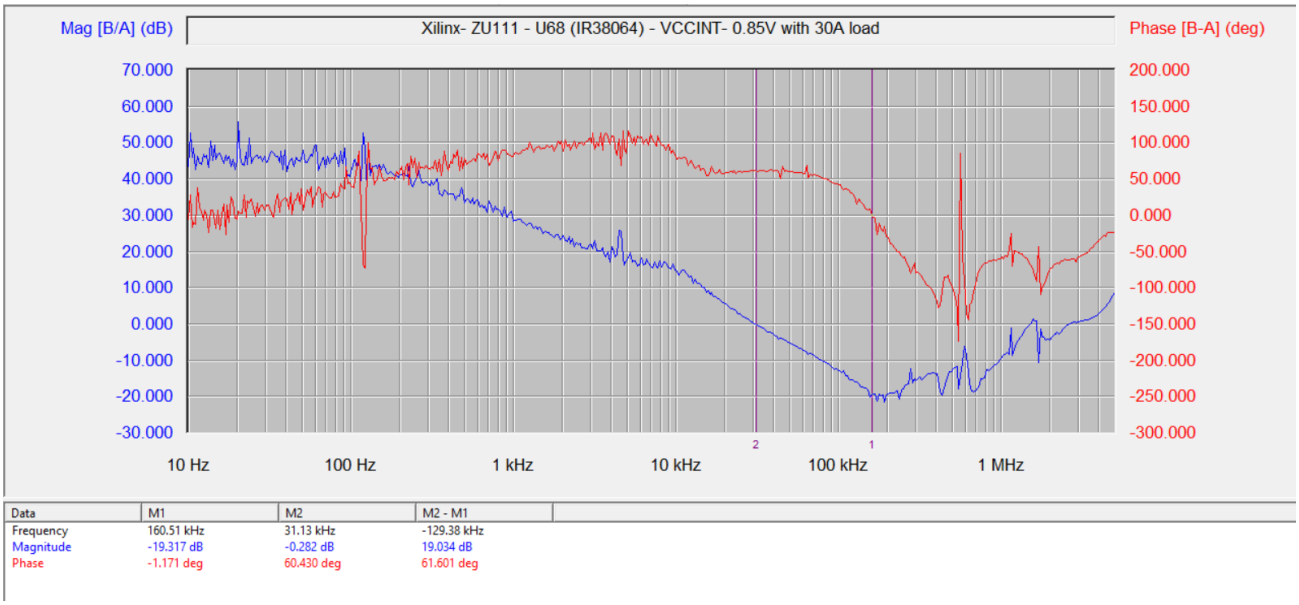


Figure – With 30A Load, crossover frequency is 31.13kHz with 60.4 deg of Phase Margin and Gain Margin of -19dB

MGTAVCC

Vin, 2.5V
Vout, 0.9V
Iout(pk), 3.0A
Istep, 1.5A
Iramp, 1A/us

Vout Measurement Location, J77, C131
Load Test Location, J77

Jitter = 26.8ns (3A load)
** note - large pigtail loop present due to load equip location*

Design Recommendations:

- **Add BODE resistor**

Test Needs

- ***BODE***

Table 16 – MGTAVCC Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.903V	Pass	0A 3.0A	DMM
DC Ripple	10mV 10mV	Pass	0A 3.0A	Active Probe
Isense	0.0A 3.2A	Pass	0A 3.1A	Telemetry/E-load
Vac(droop)	12.8mV	Pass	1.5A to 3.0A	
Vac(overshoot)	11.2mV	Pass	3.0A to 1.5A	

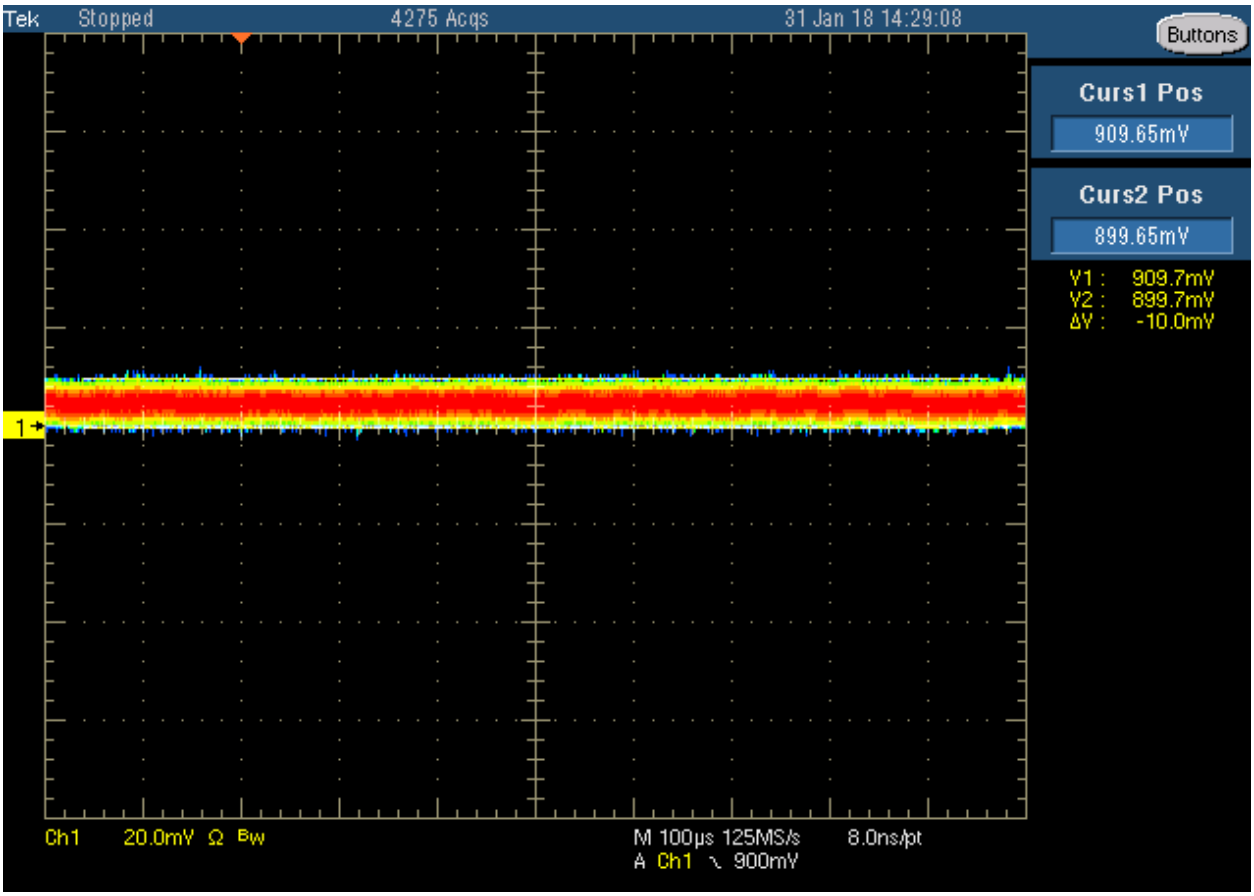


Figure 44 - MGTAVCC DC Ripple, 0.5A

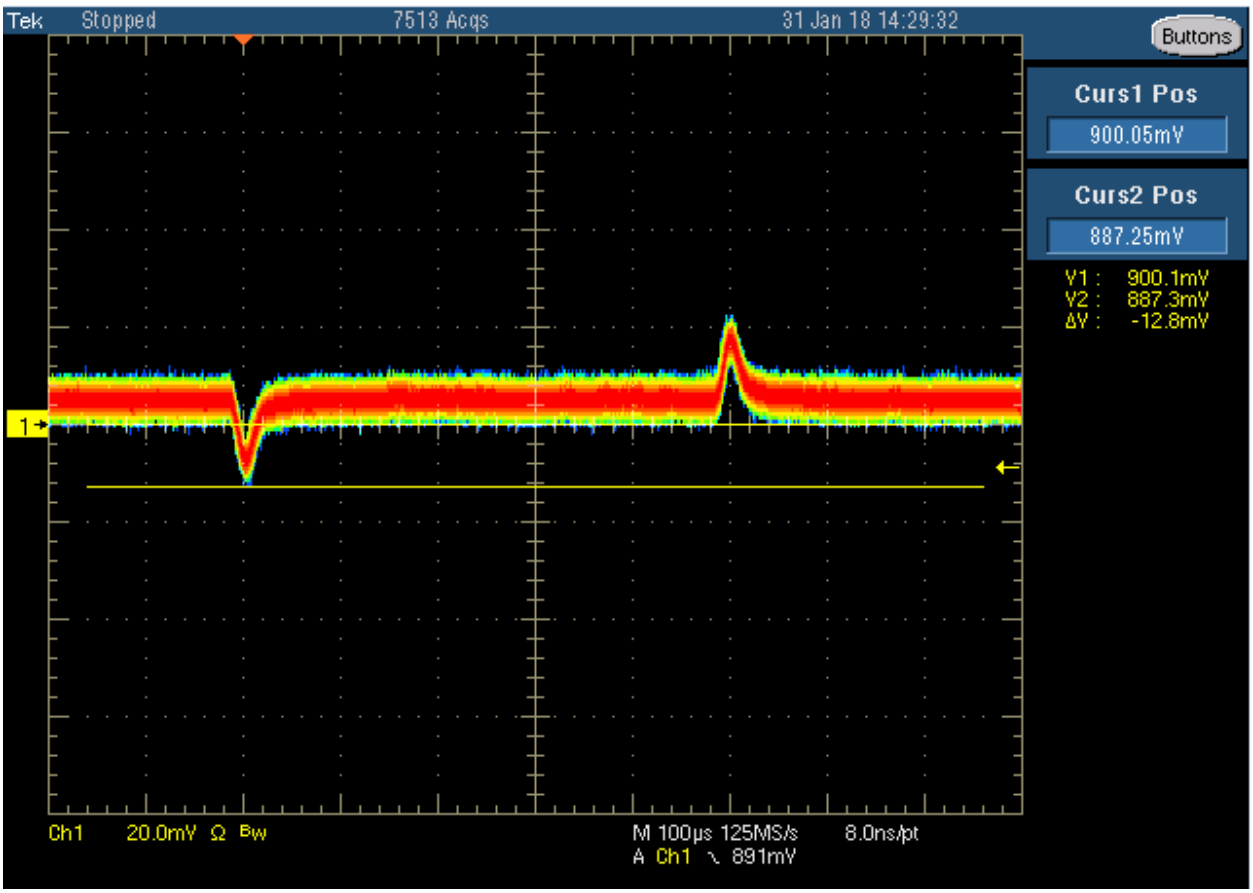


Figure 45 - MGTAVCC ac ripple load

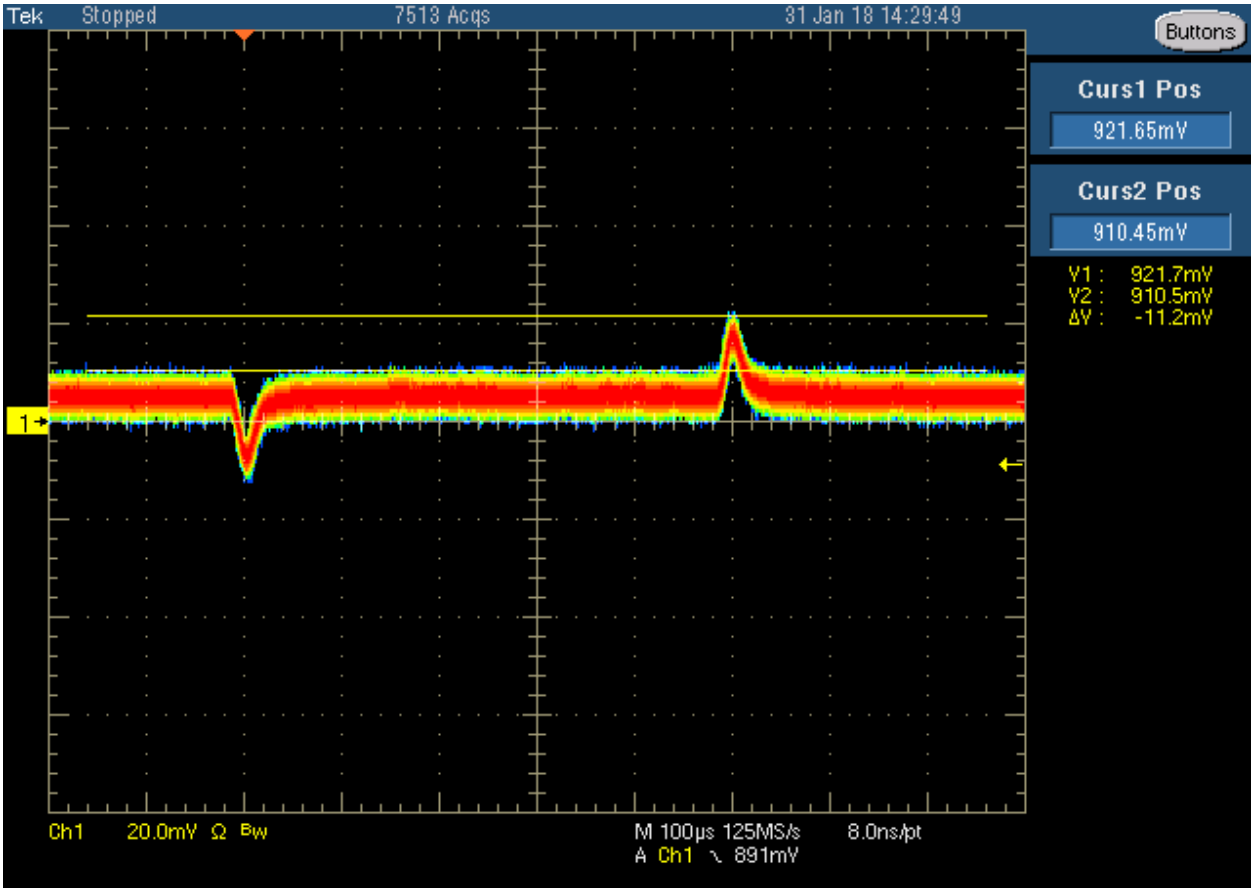


Figure 46 - MGTAVCC ac ripple release

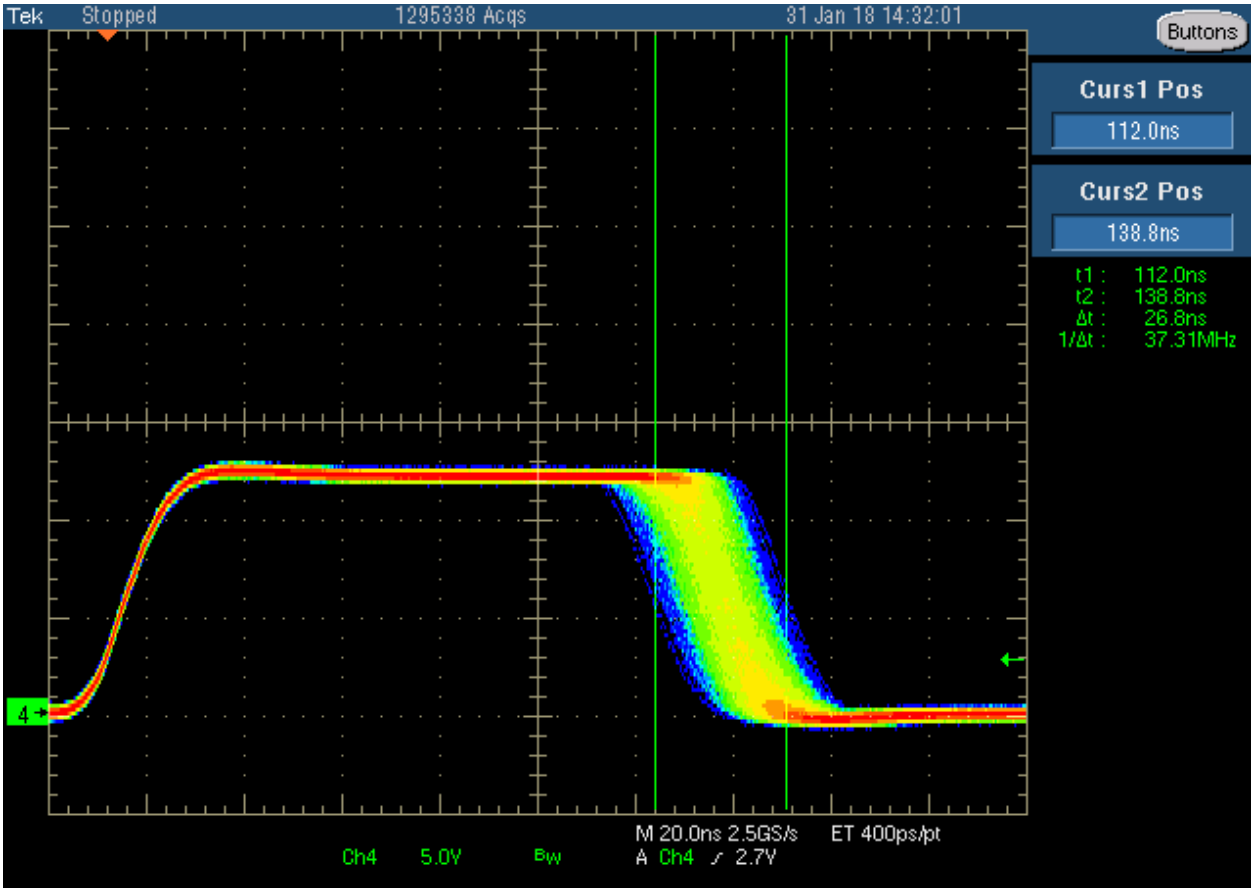


Figure 47 - MGTAVCC Jitter, 3A

DAC_AVCCAUX

Vin, 2.5V
Vout, 1.8V
Iout(pk), 0.5A
Istep, 0.125A
Iramp, 1A/us

Vout Measurement Location, J77, C326
Load Test Location, J77

Design Recommendations:

-

Test Needs

- ***DC Ripple – special test equip required***

Table 17 – DAC_AVCC_AUX Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.802V 1.800V	Pass	0A 0.5A	DMM
DC Ripple			0A 0.5A	Require STE for target spec Reached coax noise floor
Vac(droop)	7.2mV	Pass	0.375A to 0.5A	
Vac(overshoot)	8.0mV	Pass	0.5A to 0.375A	

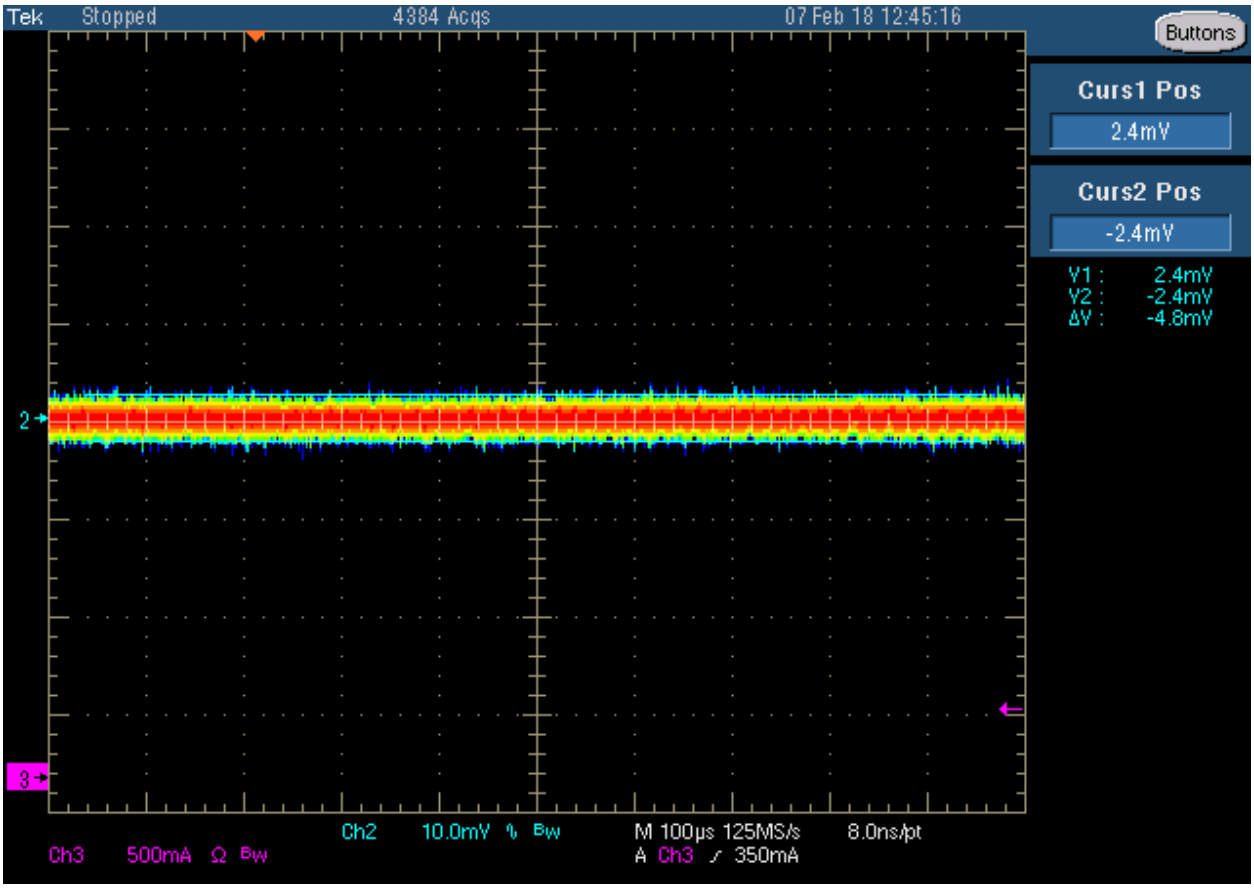


Figure 48 - DAC_AVCC_AUX DC Ripple, 0.5A

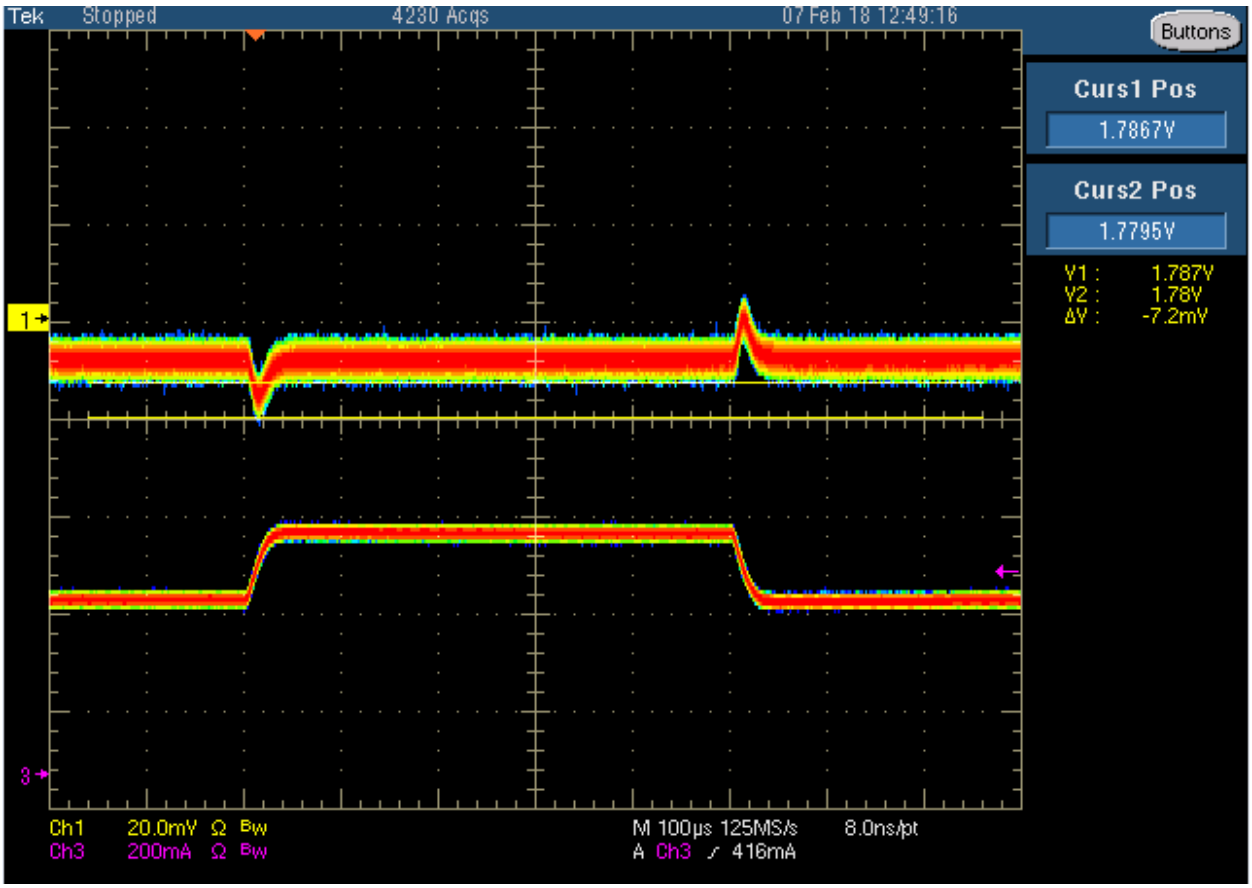


Figure 49 – DAC_AVCC_AUX ac ripple load

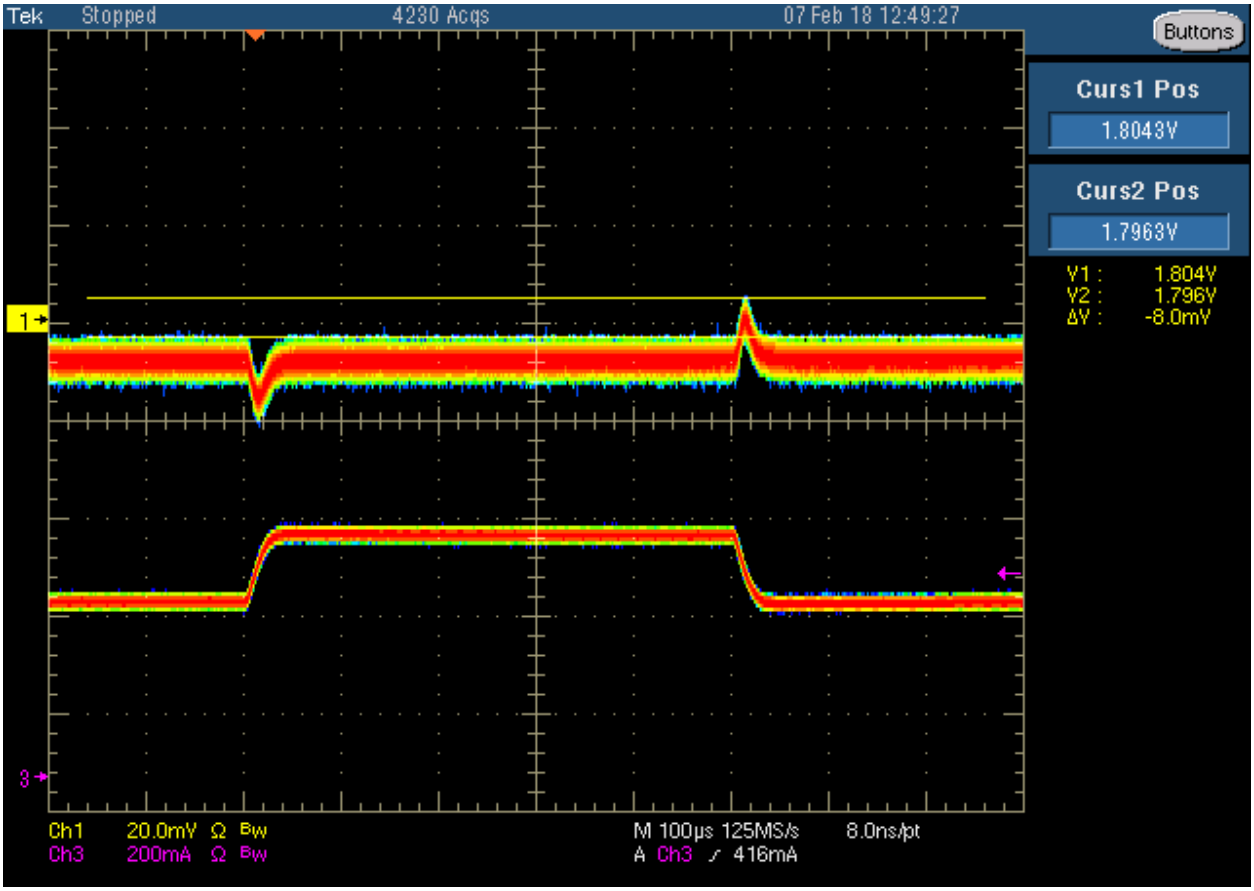


Figure 50 – DAC_AVCC_AUX ac ripple unload

ADC_AVCCAUX

Vin, 12V
Vout, 1.8V
Iout(pk), 2.0A
Istep, 2.0A
Iramp, 1A/us

Vout Measurement Location, J79, C135
Load Test Location, J79

Jitter = 50ns (no load)
** note - large pigtail loop present due to load equip location*

Design Recommendations:

- **Add BODE resistor**

Test Needs

- ***BODE***

Table 18 – ADC_AVCC_AUX Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.804V	Pass	0A 0.5A	DMM
DC Ripple	8.4mV 8.0mV	Pass	0A 0.5A	Coax
Isense	0.0A 2.19A	Pass	0A 2A	Telemetry/E-load
Vac(droop)	11.2mV	Pass	0.0A to 2.0A	
Vac(overshoot)	12.0mV	Pass	2.0A to 0.0A	

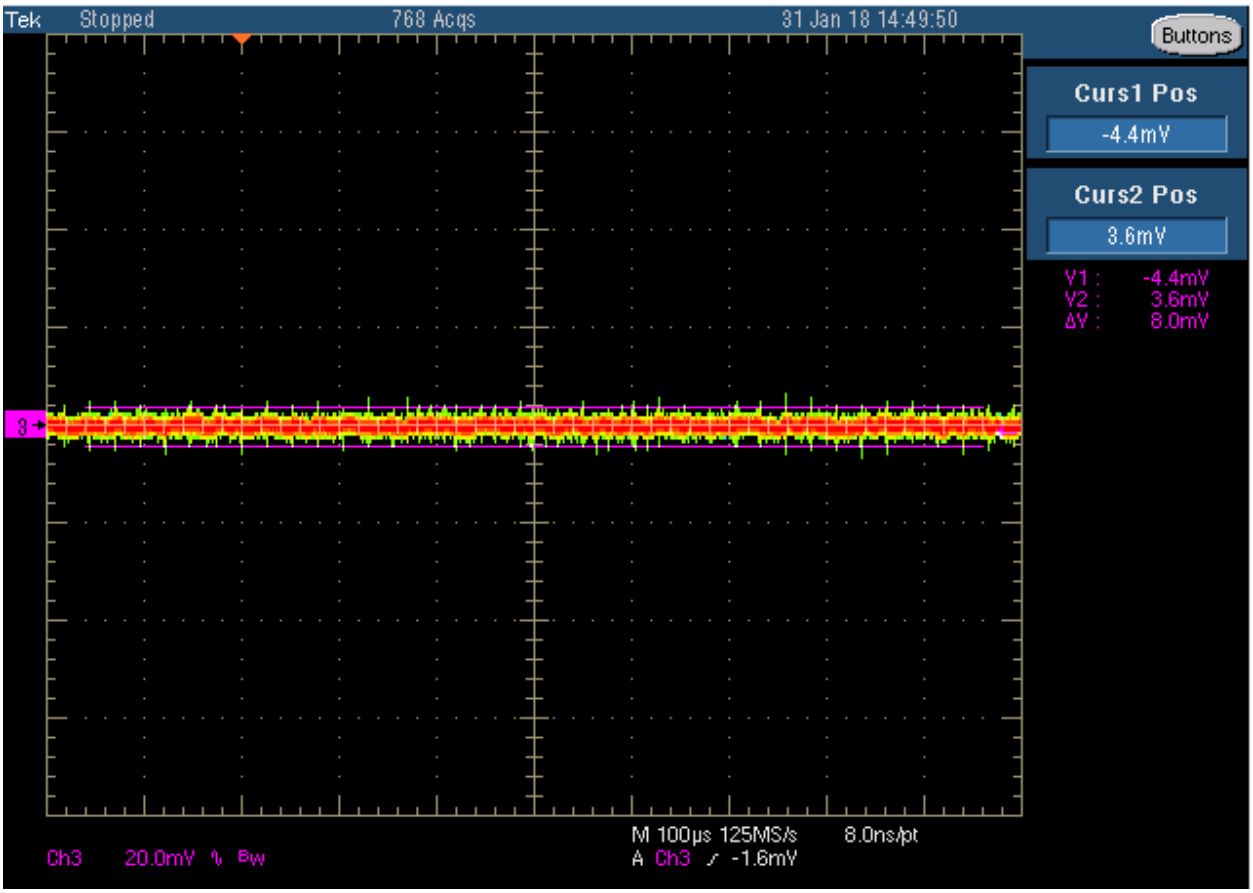


Figure 51 - ADC_AVCCAUX DC Ripple, 0.5A

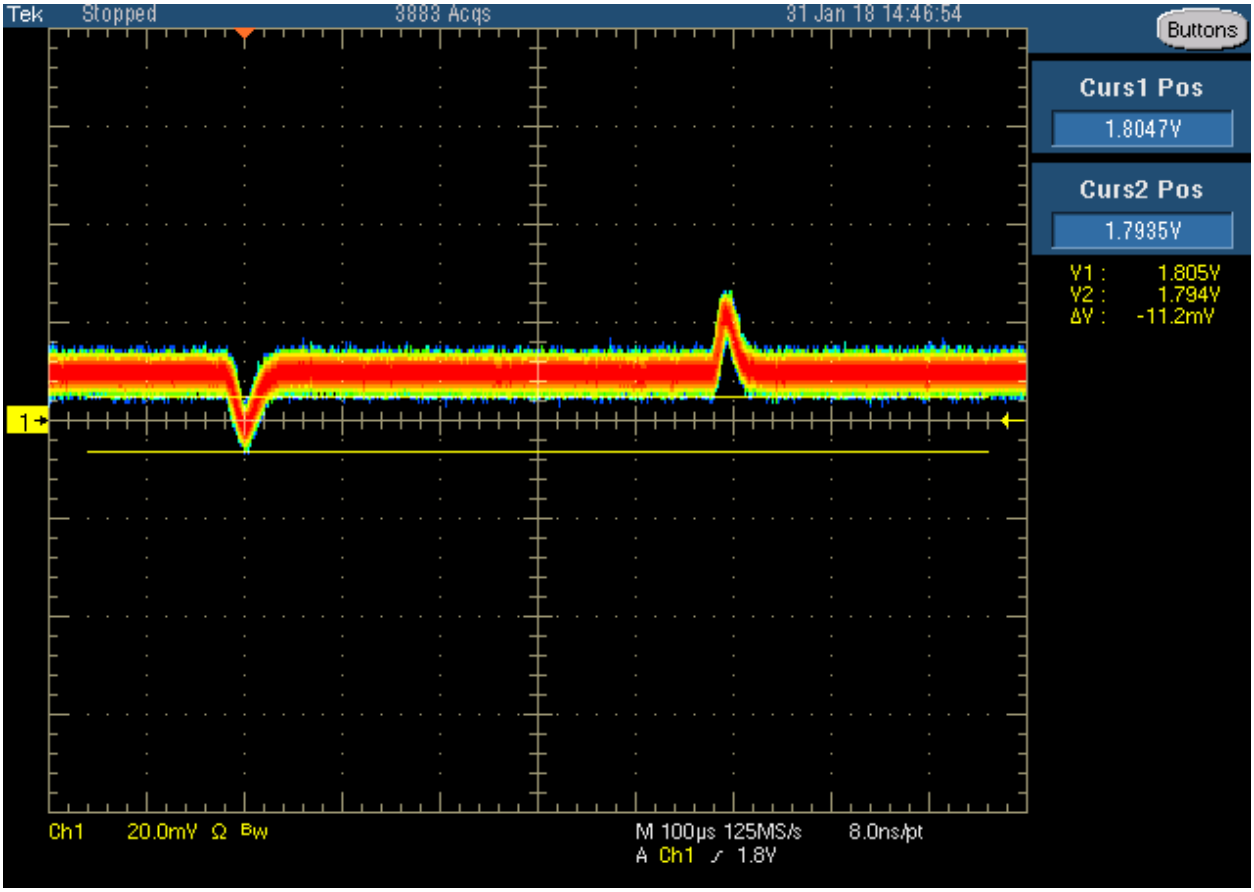


Figure 52 – ADC_AVCCAUX ac ripple load

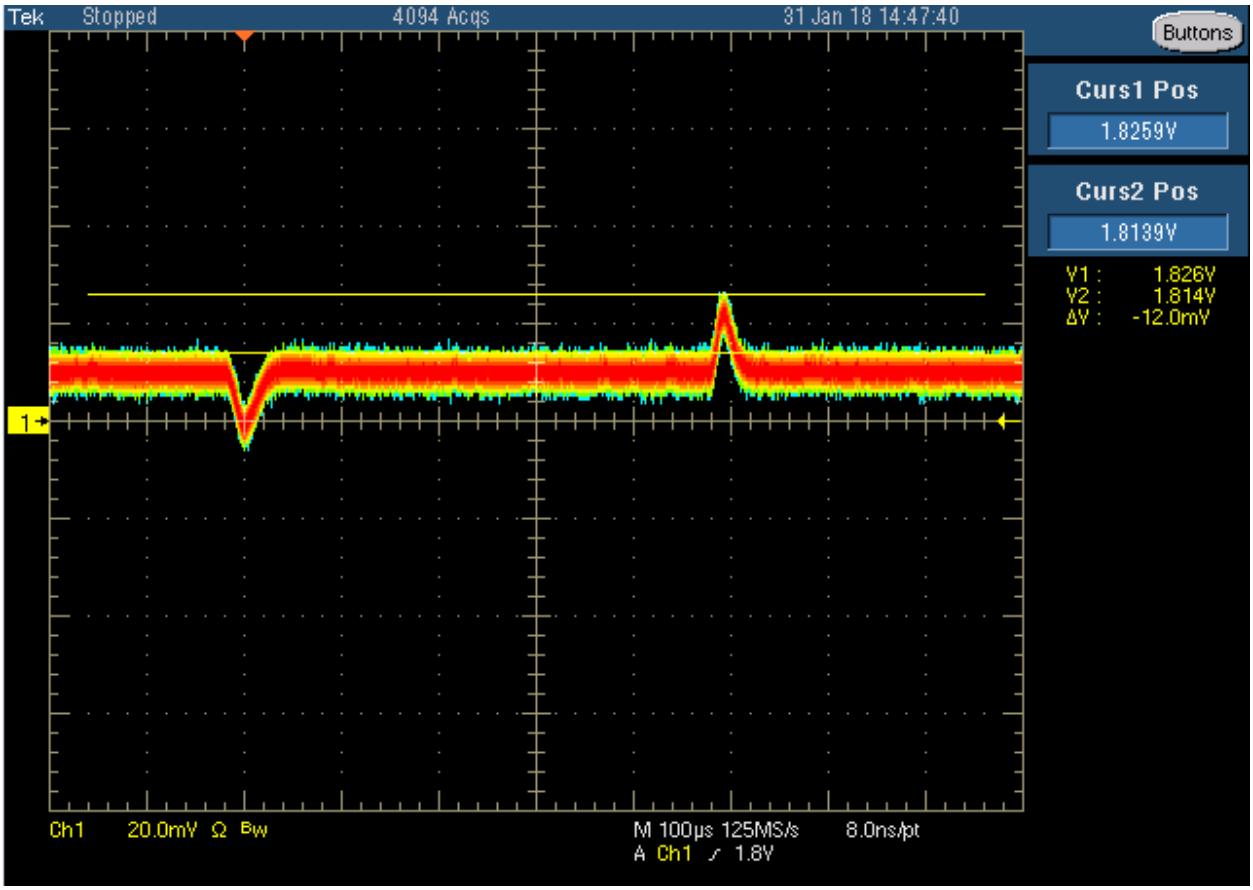


Figure 53 – ADC_AVCCAUX ac ripple unload

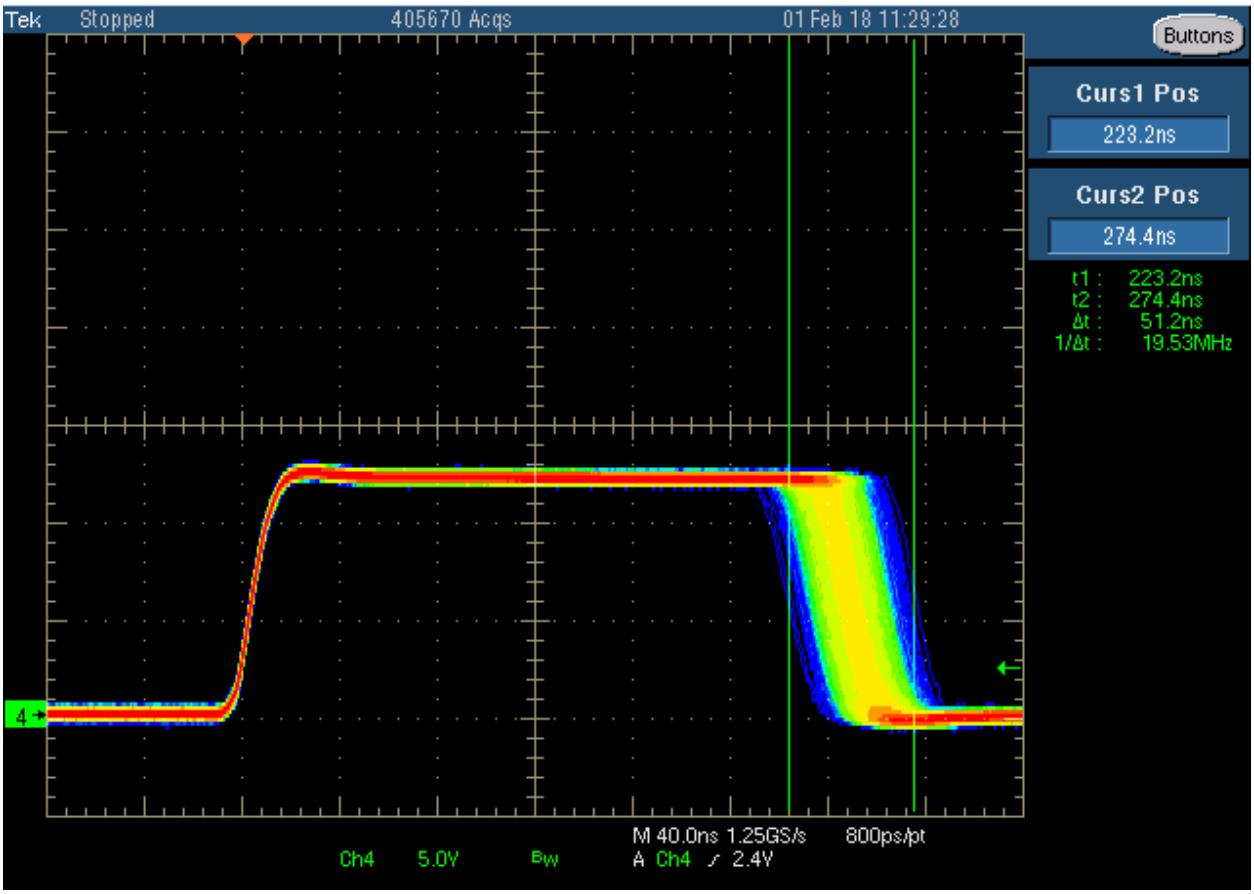


Figure 54 – ADC_AVCAUX Jitter, 2A

UTIL_1V13

Vin, 12V
Vout, 1.13V
Iout(pk), 4A
Istep, 4A
Iramp, 0.5A/us

Vout Measurement Location, J80, load cap
Load Test Location, J80
SW Node Measurement Location, L34

Jitter = 23.6ns (4A load)

Design Recommendations:

- **Add BODE resistor**

Test Needs

- ***BODE***
- ***Waveforms at load bypass caps for lower ripple***

Table 19 – UTIL_1V13 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.136V	Pass	0A 4A	DMM
DC Ripple	14.4mV 34.0mV	Pass	0A 4A	Active probe at VR. Confirmed tighter specs at load.
Isense	0.0A 4.25A	Pass	0A 4A	Telemetry/E-load
Vac(droop)	33.2mV	Pass	0A to 4A	
Vac(overshoot)	18.4mV	Pass	4A to 0A	

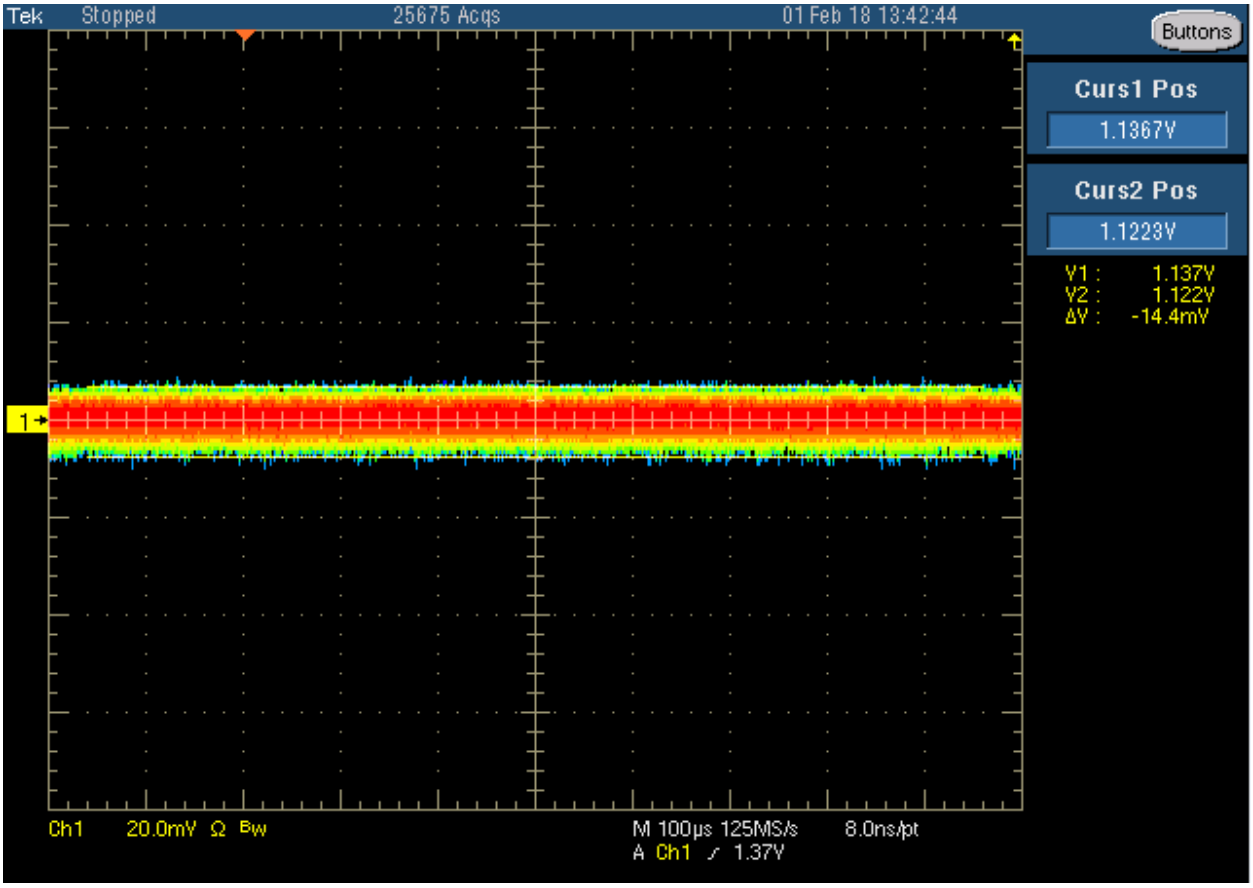


Figure 55 - UTIL_1V13 DC Ripple, 1A

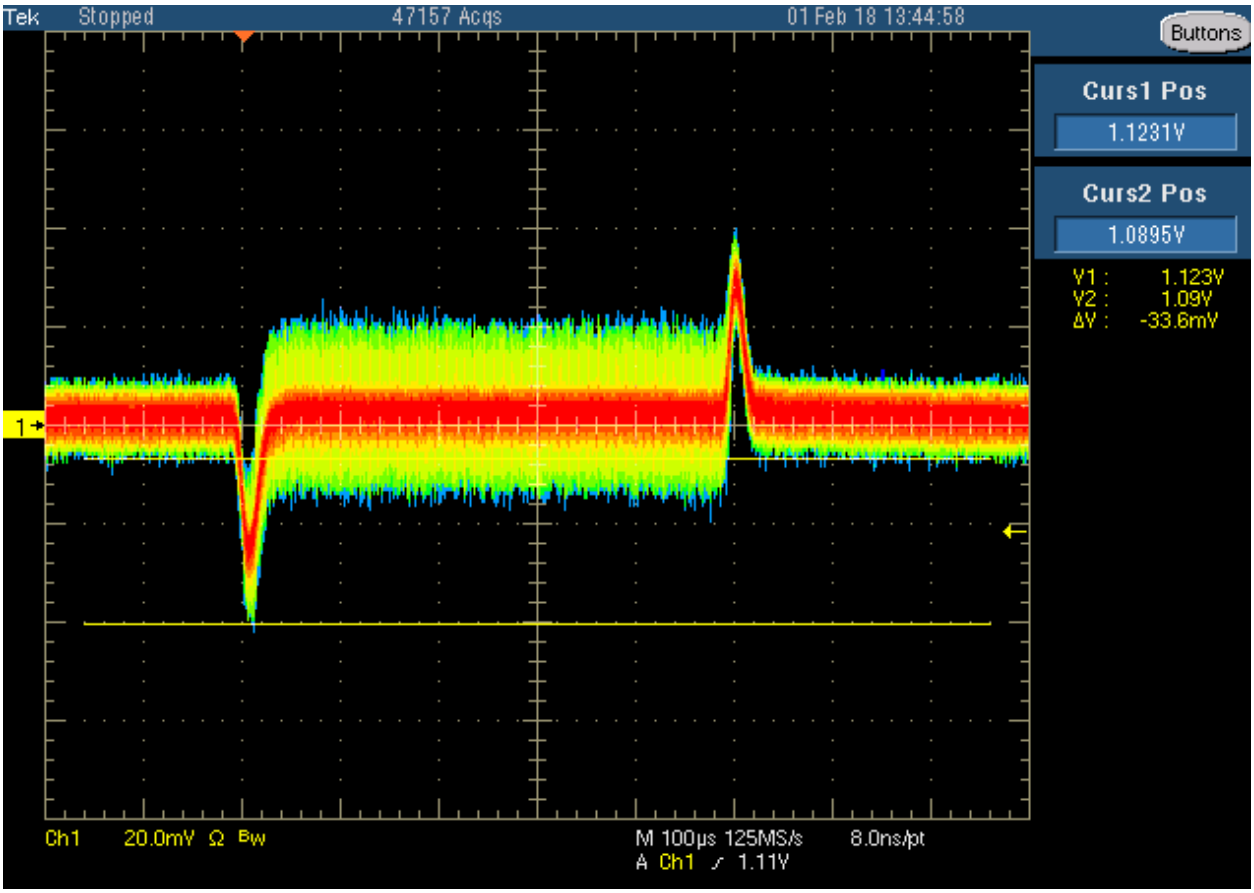


Figure 56 - UTIL_1V13 ac ripple load

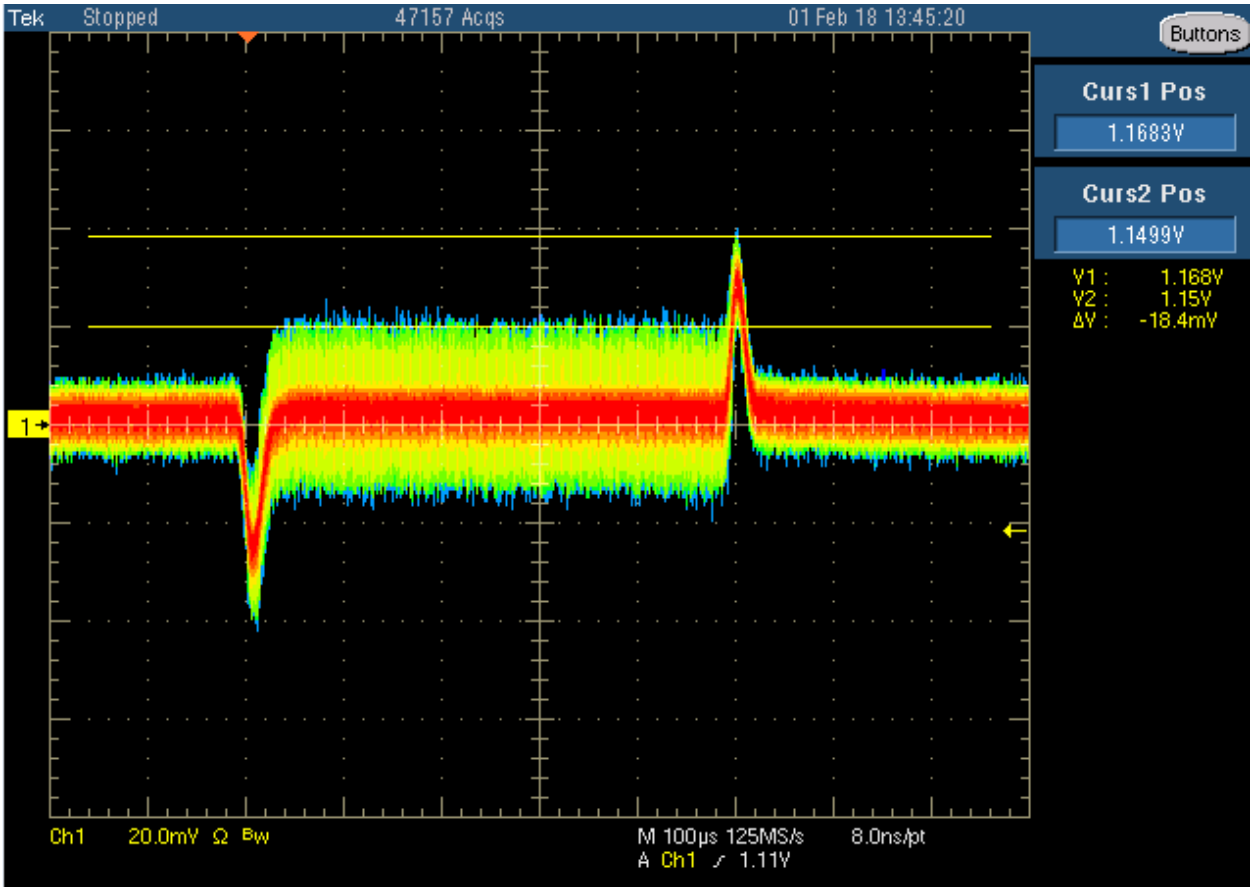


Figure 57 - UTIL_1V13 ac ripple release

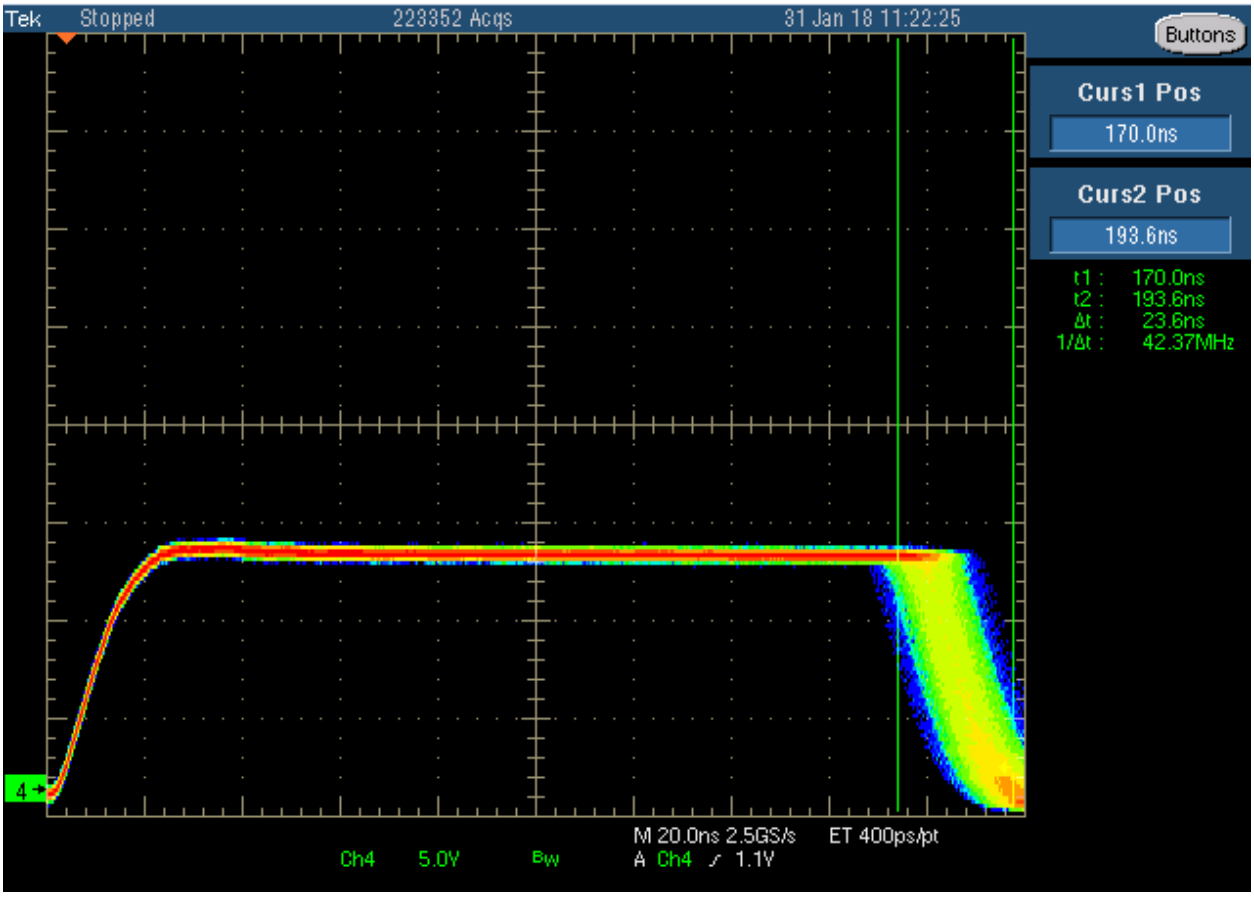


Figure 58 - UTIL_1V13 Jitter, 1A

UTIL_5V0

Vin = 12V
Vout = 5.0V
Iout(pk) = 2.7A
Istep, 1A
Iramp, 1A/us

Vout Measurement Location, J81, Cout
Load Test Location, J81
SW Node Measurement Location, L35

Design Recommendations:

-

Test Needs

-

Table 20 – UTIL_5V0 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	5.V	Pass	0A	DMM
DC Ripple	41.6mV 19.6mV	Pass	0A 2.7A	Active probe
Vac(droop)	23.6mV	Pass	1.7A to 2.7A	
Vac(overshoot)	35.6mV	Pass	2.7A to 1.7A	

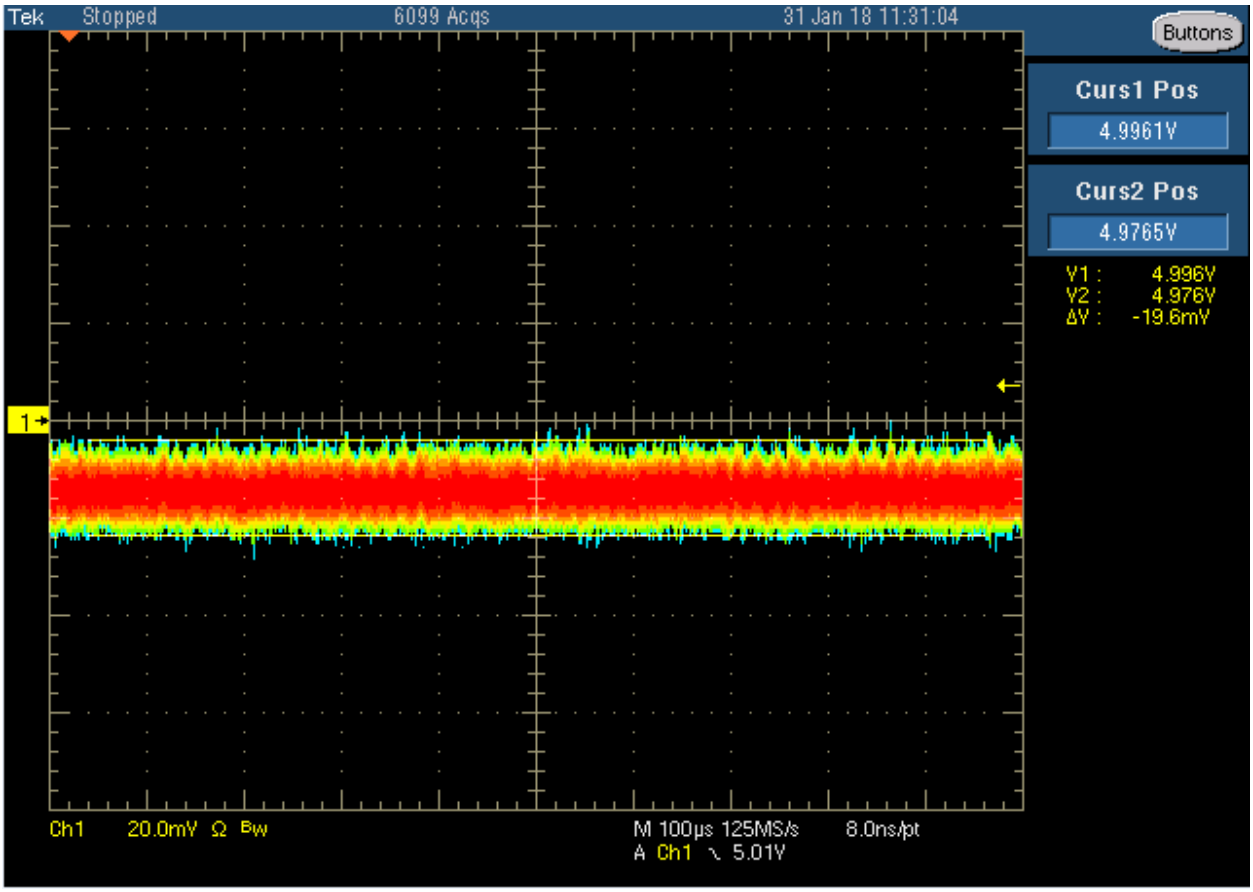


Figure 59 - UTIL_5V0 DC Ripple, 2.1A

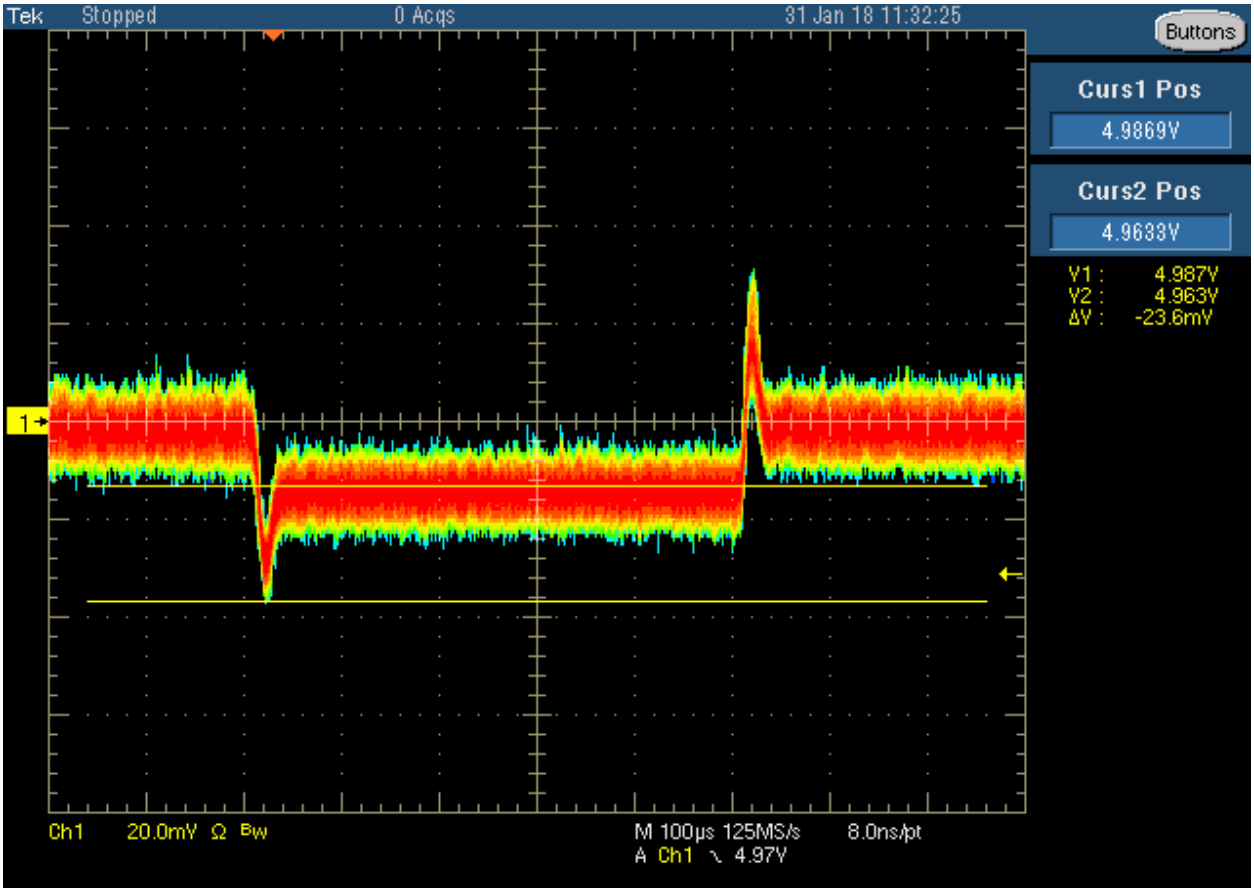


Figure 60 - UTIL_5V0 ac ripple load

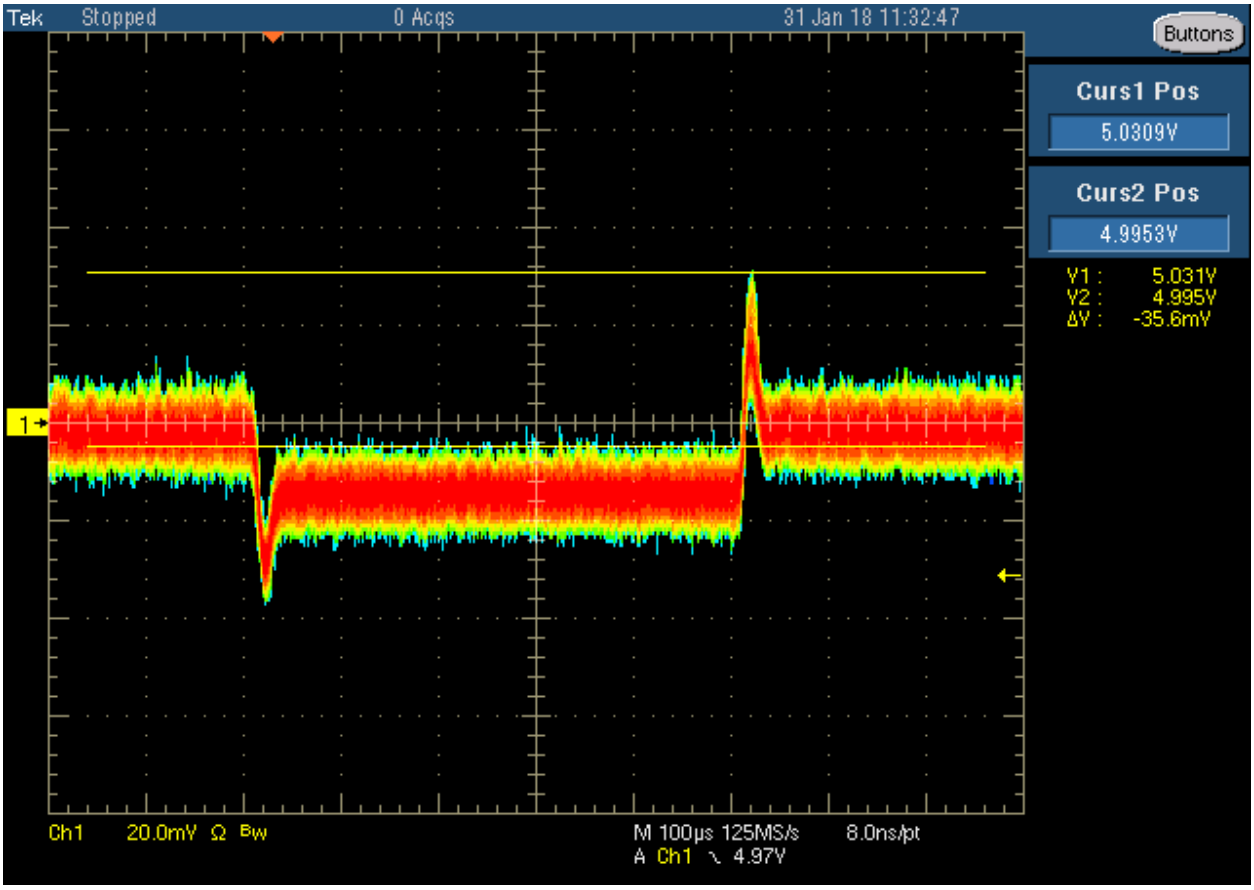


Figure 61 - UTIL_5V0 ac ripple unload

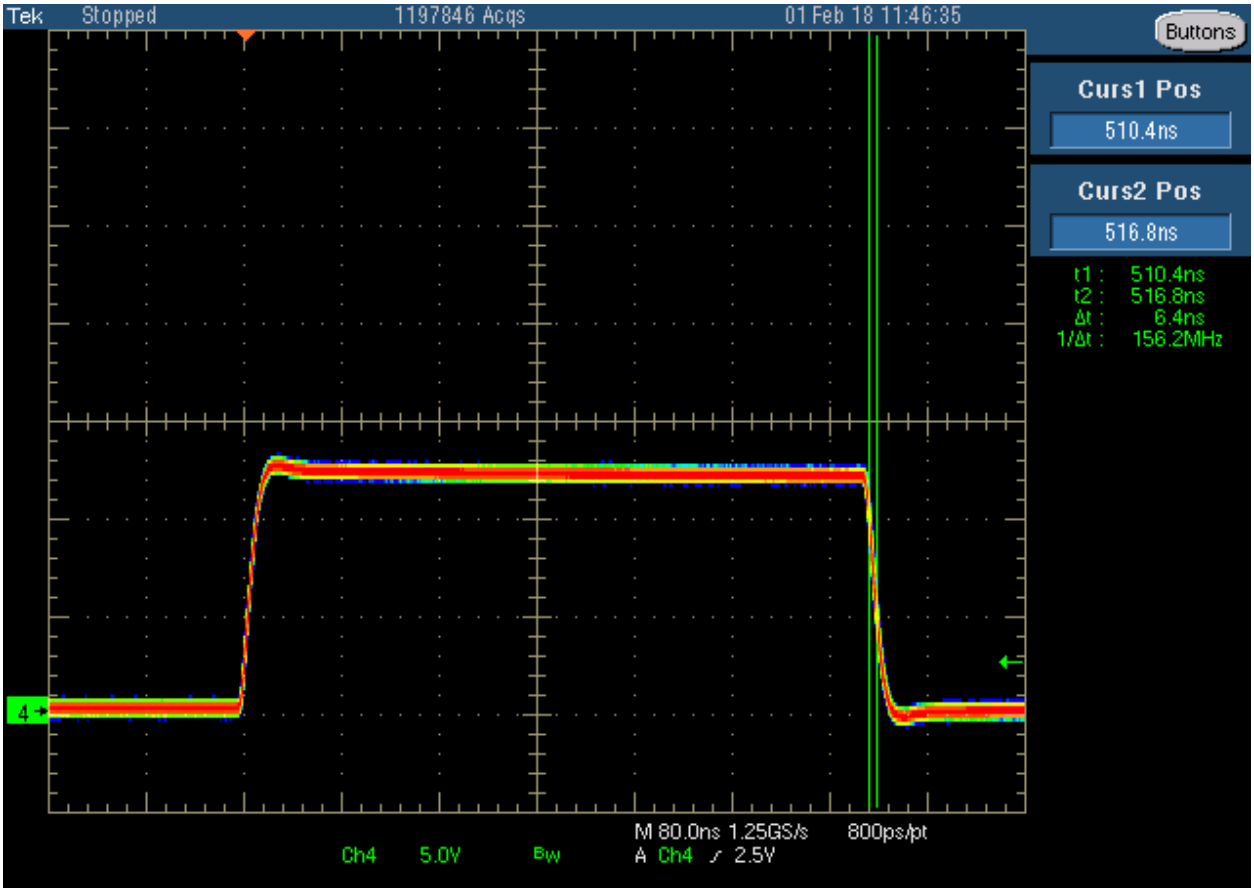


Figure 62 - UTIL_5V0 Jitter, 2.1A

ADC_AVCC

Vin, 1.13V
Vout, 0.925V
Iout(pk), 2.0A
Istep, 0.5A
Iramp, 1A/us

Vout Measurement Location, J82,
Load Test Location, J82

Design Recommendations:

-

Test Needs

- ***DC Ripple – special test equip required***

Table 21 – ADC_AVCC Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.927V	Pass	0A 2.0A	DMM
DC Ripple			0A 2A	Require STE for target spec Reached coax noise floor
Vac(droop)	None measurable to 2A step (<2.0mV)	Pass	1.5A to 2A	
Vac(overshoot)	None measurable to 2A step (<2.0mV)	Pass	1.5A to 2A	

DAC_AVCC

Vin, 1.13V
Vout, 0.925V
Iout(pk), 1.0A
Istep, 0.25A
Iramp, 1A/us

Vout Measurement Location, J82, C131
Load Test Location, J82

Design Recommendations:

-

Test Needs

- ***DC Ripple – special test equip required***

Table 22 – DAC_AVCC Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.93V	Pass	0A 1.0A	DMM
DC Ripple			0A 1A	Require STE for target spec Reached coax noise floor
Vac(droop)	No discernable droop 2mV	Pass	0.75A to 1A 0.5A to 1A	
Vac(overshoot)	No discernable overshoot 2.4mV	Pass	1.0A to 0.75A 1A to 0.5A	

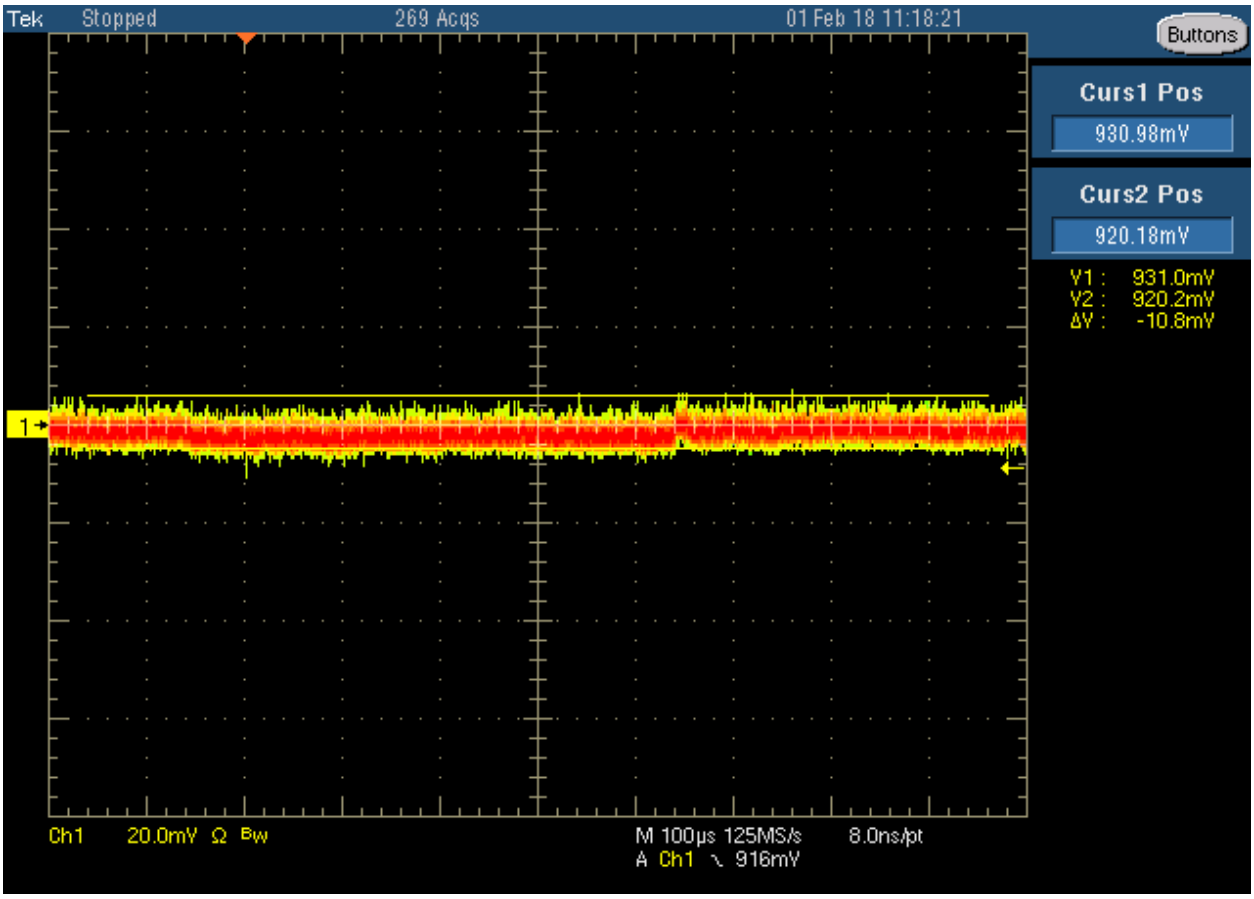


Figure 63 – DAC_AVCC ac ripple

PL_DDR4_VTT

Vin, 12V
Vout, 0.6V
Iout(pk), 3A
Istep, 1.5A
Iramp, 0.5A/us

Vout Measurement Location, J84
Load Test Location, J84
SW Node Measurement Location, L36

Jitter = 7.4ns (3A load)

Design Recommendations:

- **Add BODE resistor**

Test Needs

- ***BODE***
- ***Waveforms from load bypass cap***

Table 23 – PL_DDR4_VTT Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.6V 0.6V	Pass	0A 3A	DMM
DC Ripple	30.0mV 26.8mV	Pass	0A 3A	Active Probe
Vac(droop)	14.0mV	Pass	1.5A to 3.0A	
Vac(overshoot)	10.4mV	Pass	3.0A to 1.5A	

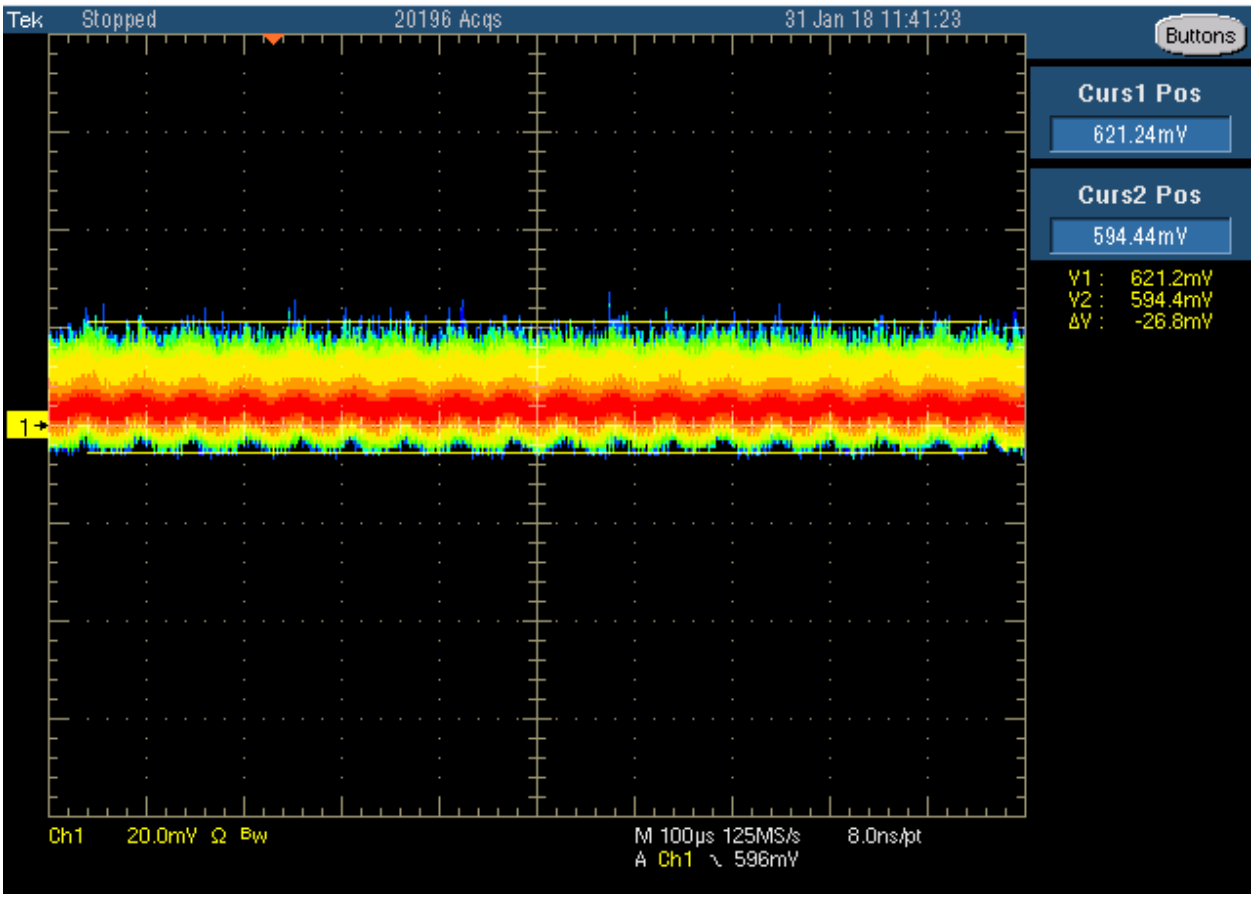


Figure 64 - PL_DDR4_VTT DC Ripple, 3A

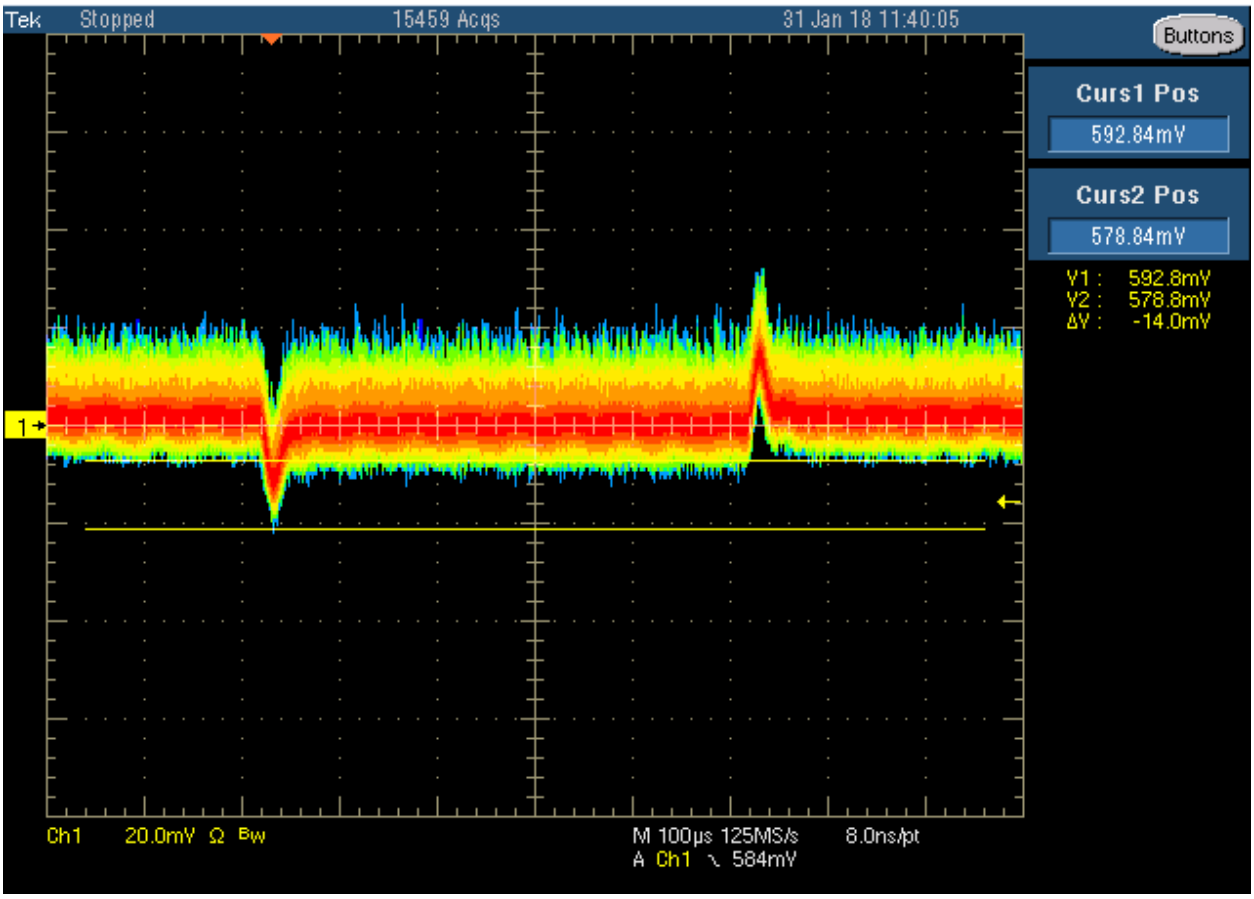


Figure 65 - PL_DDR4_VTT ac ripple load

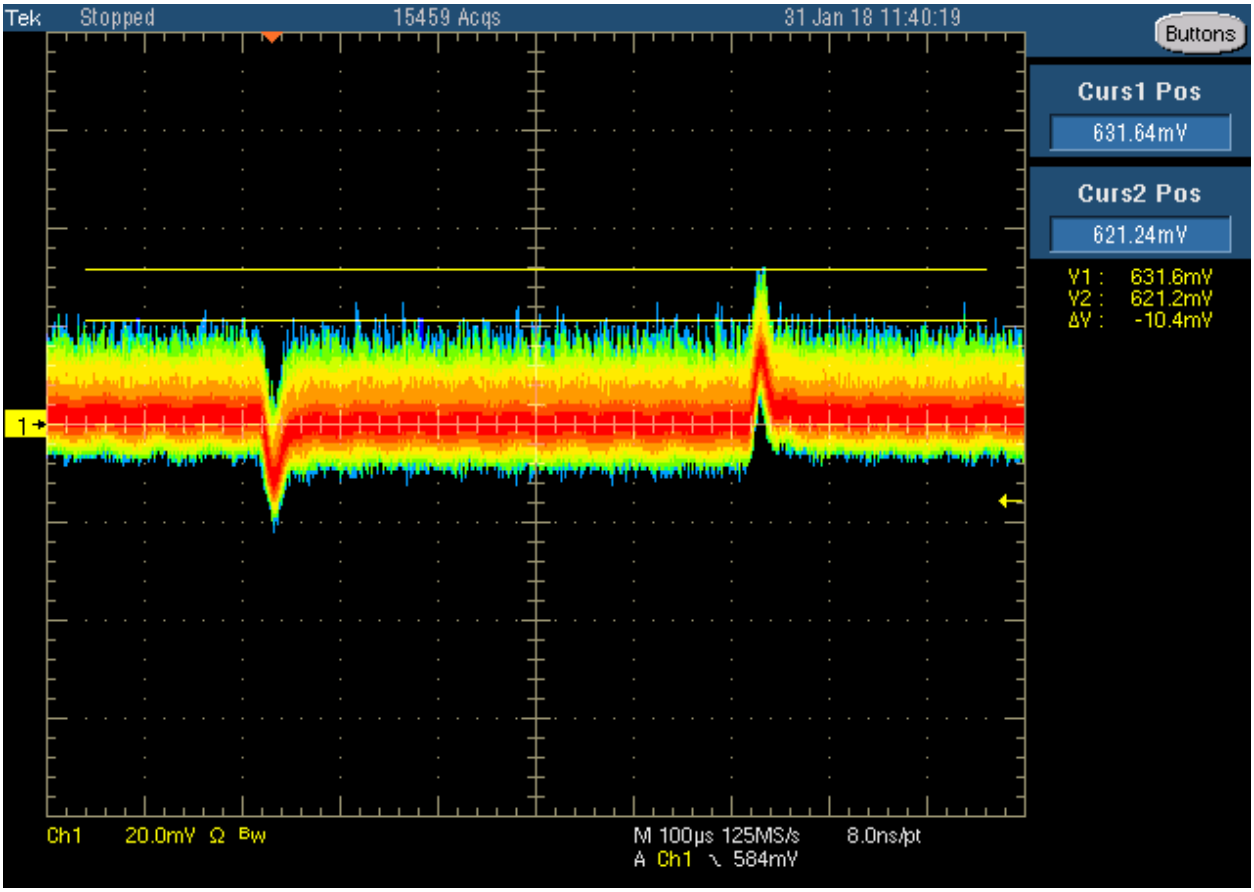


Figure 66 - PL_DDR4_VTT ac ripple release

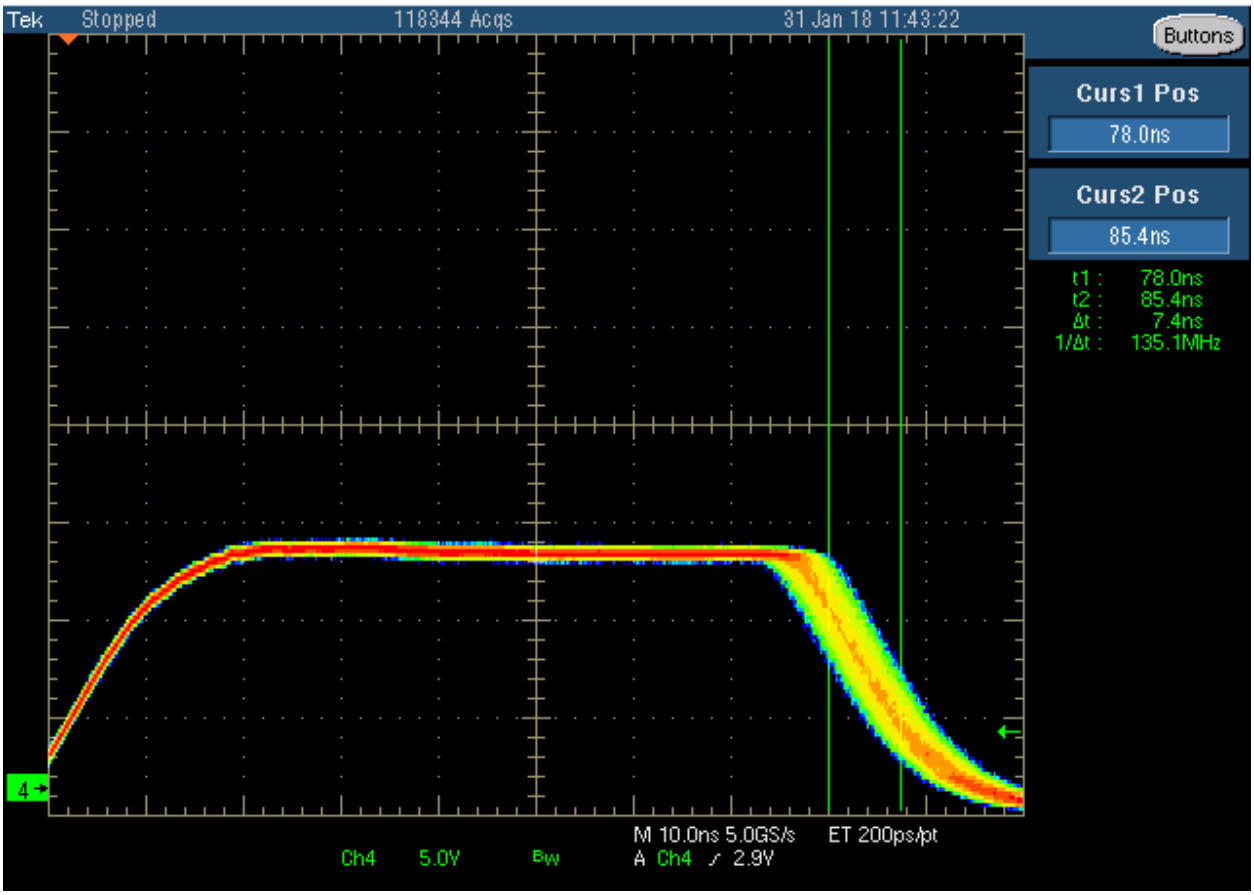


Figure 67 - PL_DDR4_VTT Jitter, 3A

PS_DDR4_VTT

Vin, 12V
Vout, 0.6V
Iout(pk), 3A
Istep, 1.5A
Iramp, 0.5A/us

Vout Measurement Location, J85
Load Test Location, J85
SW Node Measurement Location, L37

Design Recommendations:

- **Add BODE resistor**

Test Needs

- ***BODE***
- ***Jitter***

Table 24 – PS_DDR4_VTT Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.6V 0.599V	Pass	0A 3A	DMM
DC Ripple	12.0mV 12.4mV	Pass	0A 3A	Active Probe
Vac(droop)	8.8mV	Pass	1.5A to 3.0A	
Vac(overshoot)	9.2mV	Pass	3.0A to 1.5A	

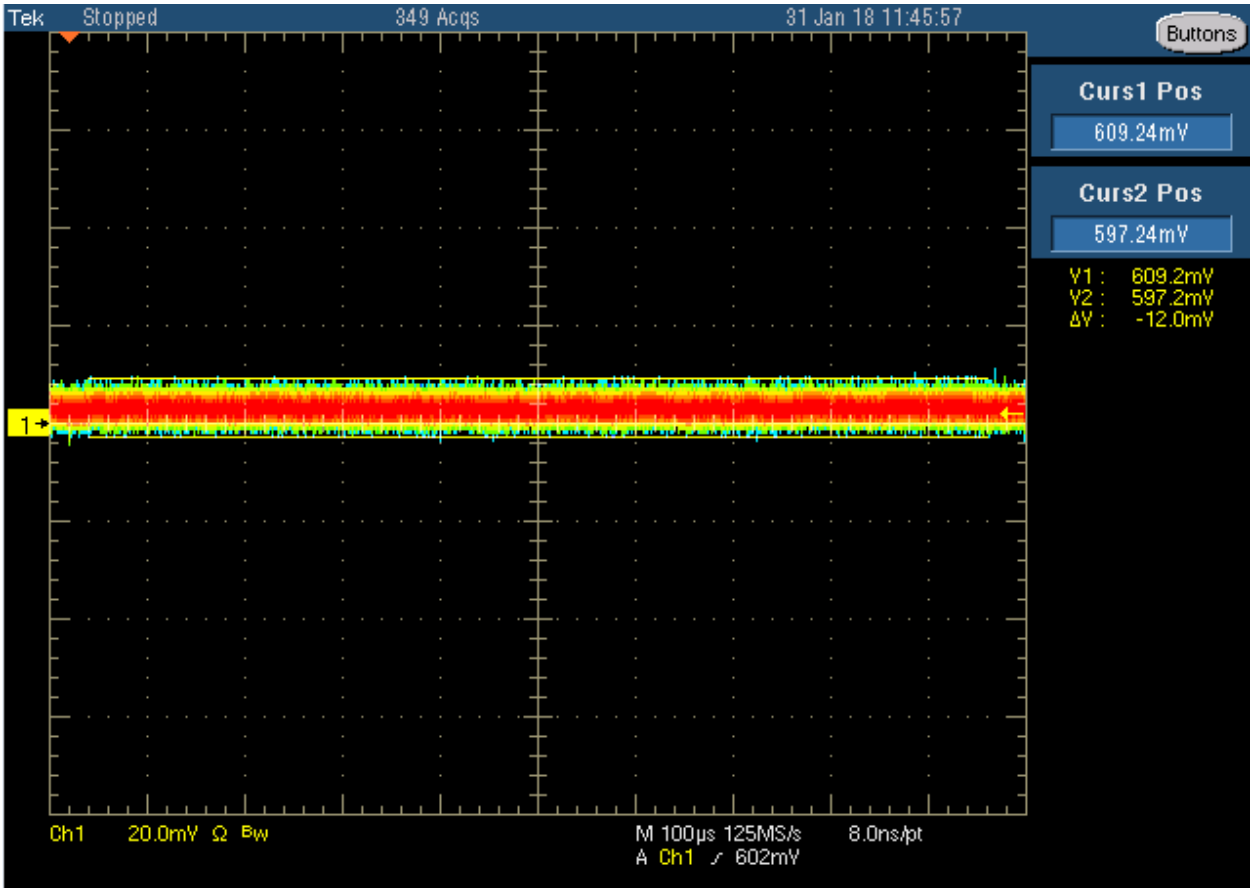


Figure 68 - PS_DDR4_VTT DC Ripple, 3A

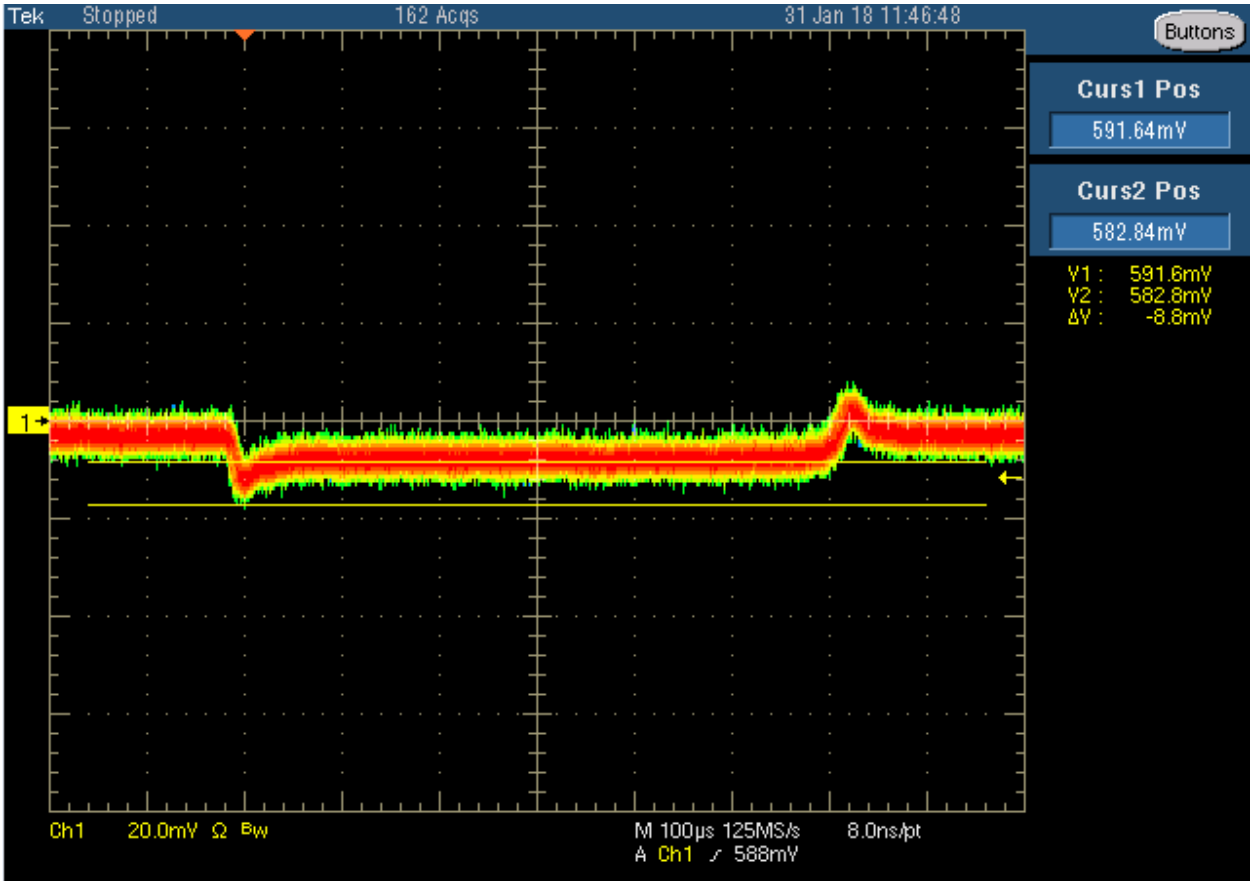


Figure 69 - PS_DDR4_VTT ac ripple load

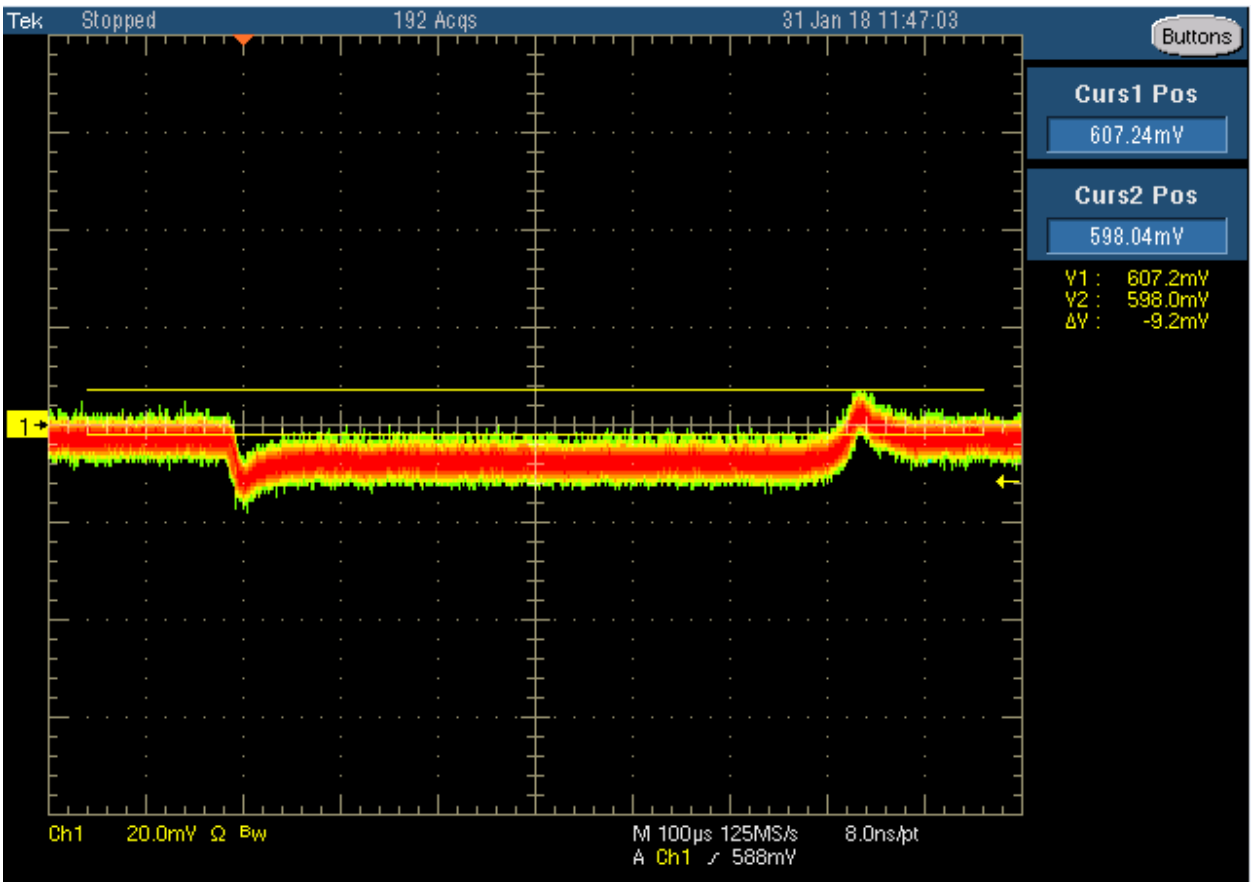


Figure 70 - PS_DDR4_VTT ac ripple release

Figure 71 - PS_DDR4_VTT Jitter, 3A

UTIL_3V5

Vin, 12V
Vout, 3.5V
Iout(pk), 3A
Istep, 1.5A
Iramp, 1A/us

Vout Measurement Location, J93, C832
Load Test Location, J93
SW Node Measurement Location, L71

Design Recommendations:

- **Evaluate DC drop from VR to load**

Test Needs

-

Table 25 – UTIL_3V5 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	3.518V	Pass	0A 3A	DMM
DC Ripple	14.0mV 11.6mV	Pass	0A 3A	Active probe
Vac(droop)	26.4mV	Pass	1.5A to 3.0A	
Vac(overshoot)	29.6mV	Pass	3.0A to 1.5A	

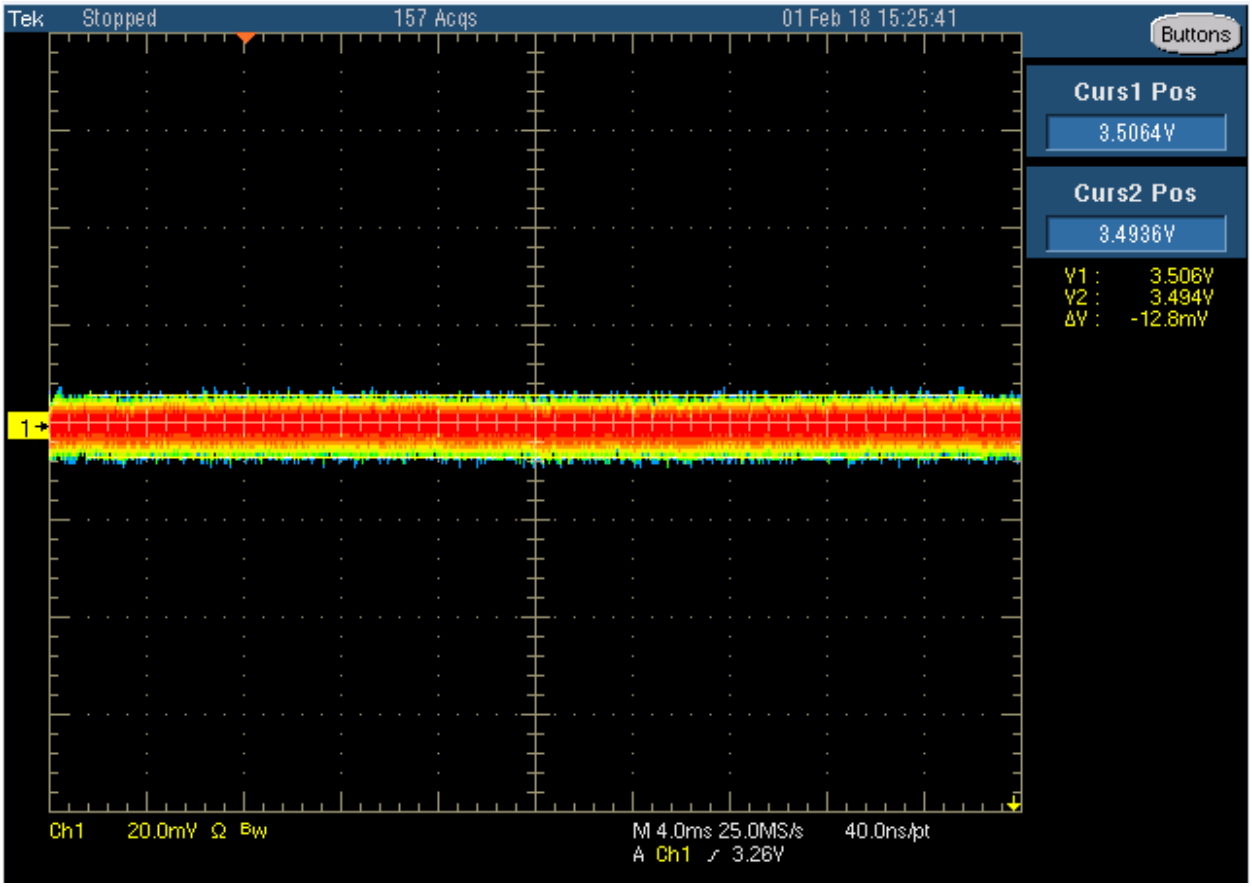


Figure 72 - UTIL_3V5 DC Ripple, 3A

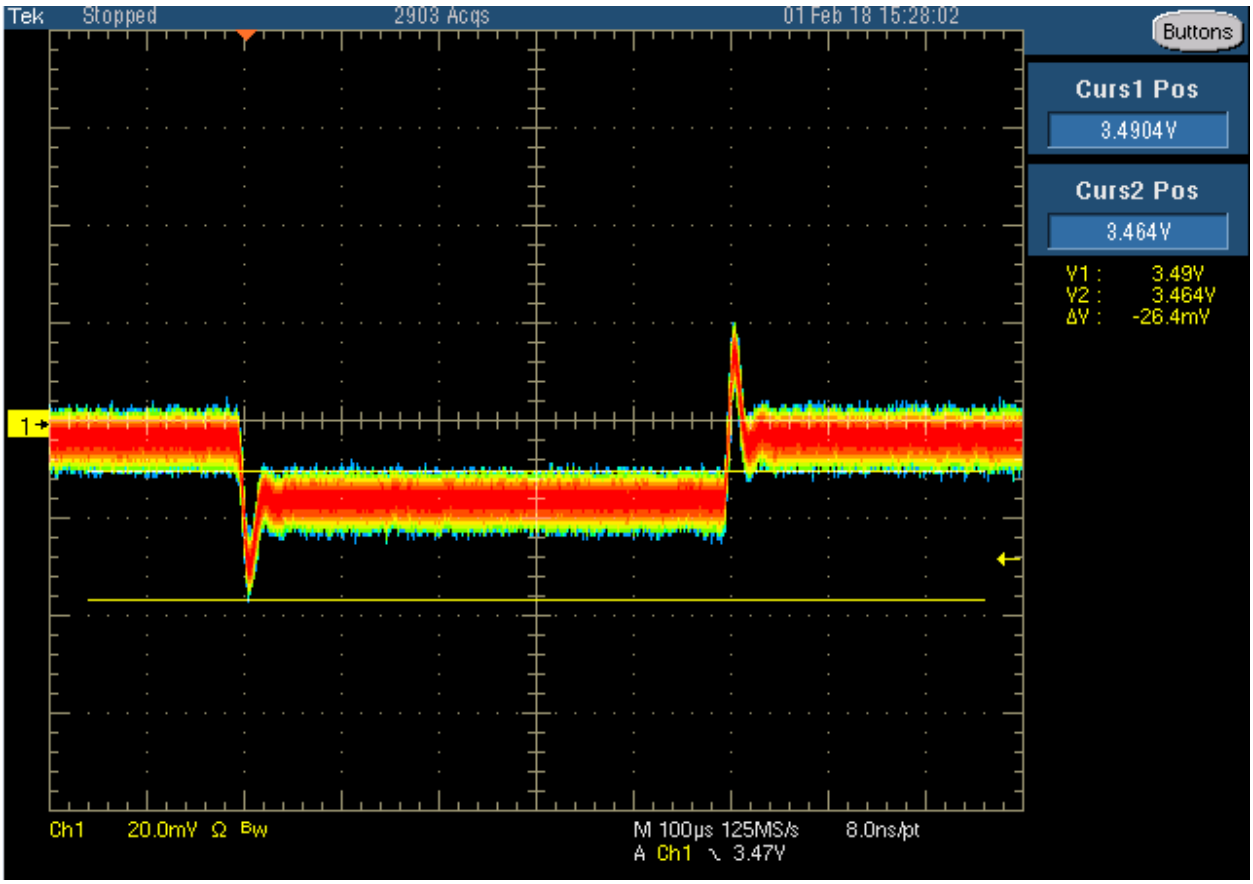


Figure 73 - UTIL_3V5 ac ripple load

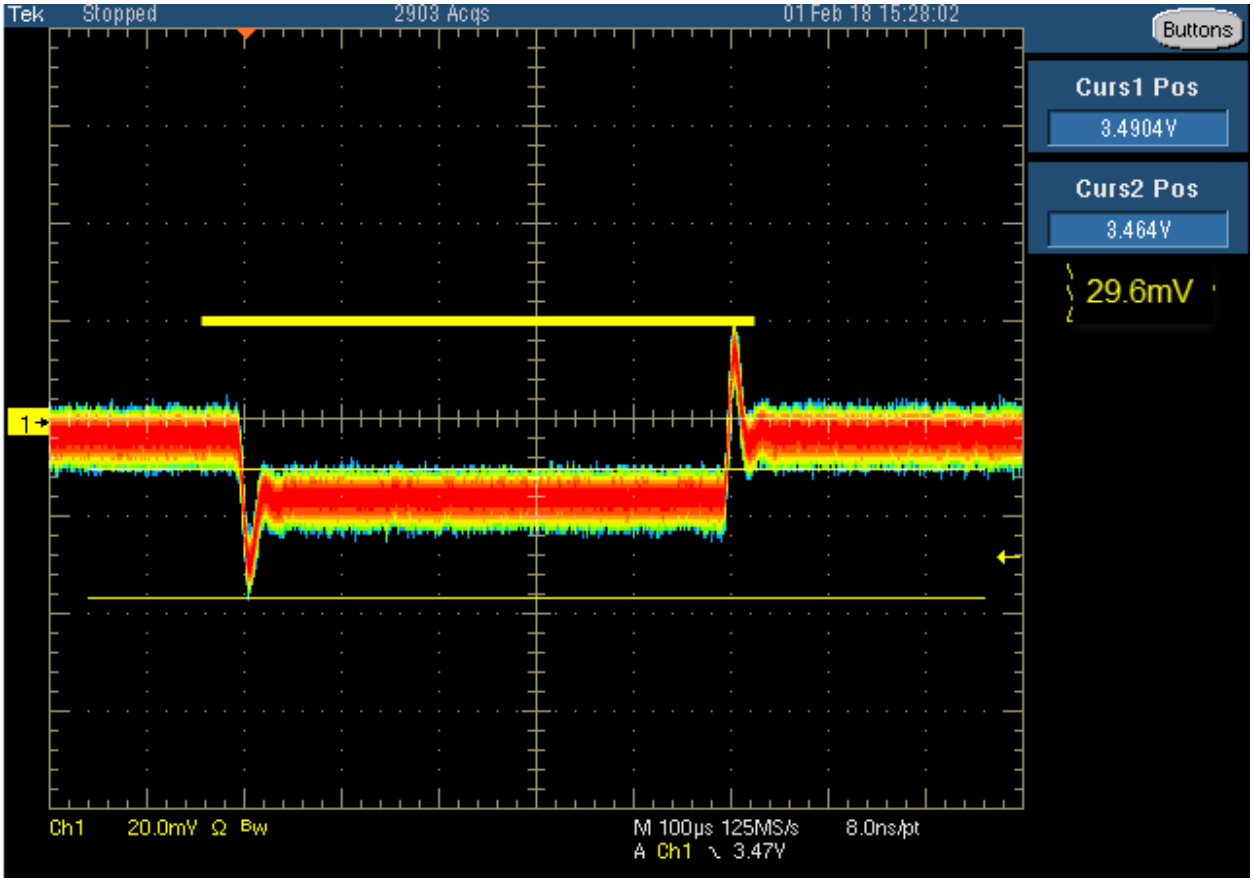


Figure 74 - UTIL_3V5 ac ripple unload

AMS_CLK_VCC3V3

Vin, 12V
Vout, 3.3V
Iout(pk), 3A
Istep, 1.5A
Iramp, 1A/us

Vout Measurement Location, J63, C827, L73, C953, L58
Load Test Location, J63

Design Recommendations:

- **Evaluate Cu and impedance from VR to load to alleviate DC drop**

Test Needs

-

Table 26 – AMS_CLK_VCC3V3 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	3.33V	Pass	0A 3A	DMM
DC Ripple	10.0mV 11.2mV	Pass	0A 3A	Active probe
Vac(droop)	***46.4mV	Pass	1.5A to 3.0A	See slew rate There is no undershoot
Vac(overshoot)	***46.0mV	Pass	3.0A to 1.5A	See slew rate There is minimal VOS, 20mV

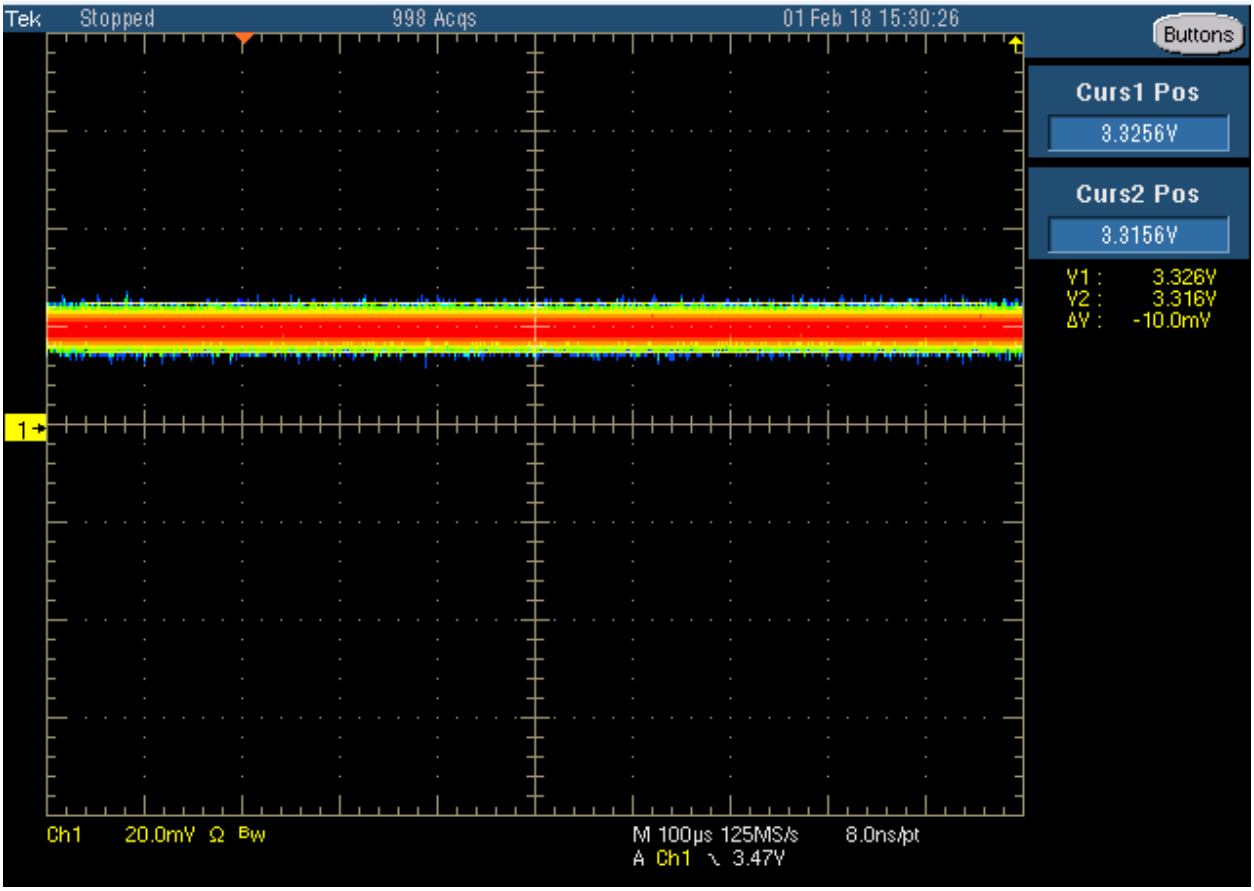


Figure 75 - AMS_CLK_VCC3V3 DC Ripple, 3A

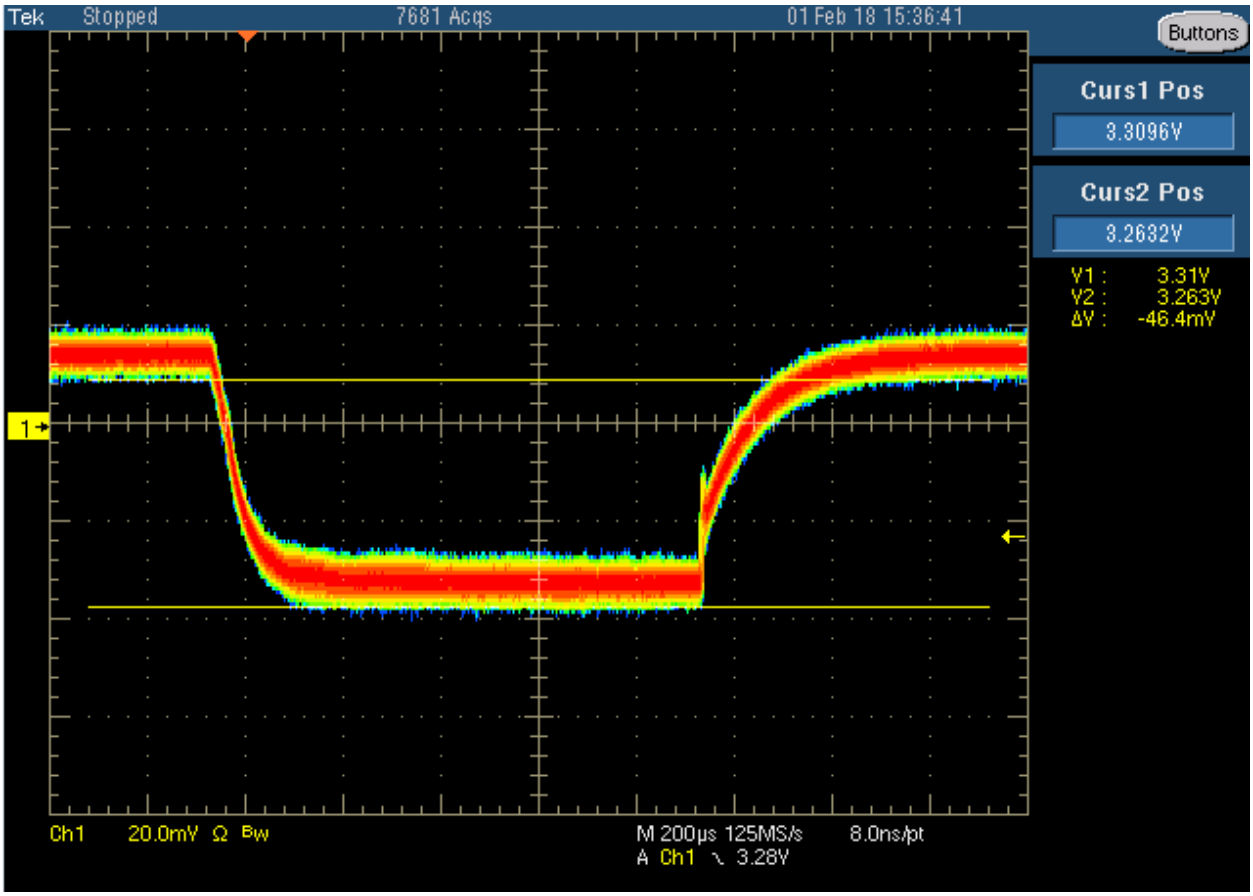


Figure 76 - AMS_CLK_VCC3V3 ac ripple load

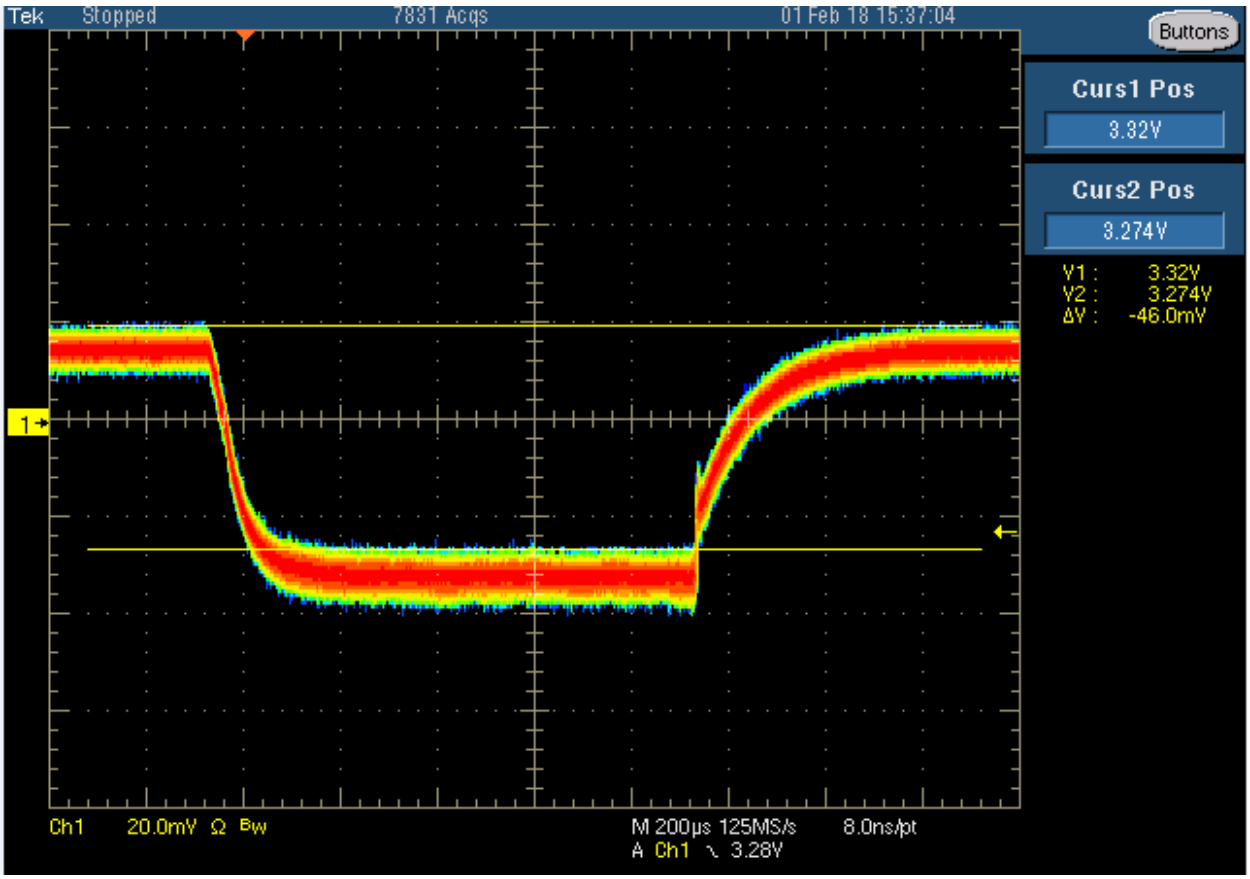


Figure 77 - AMS_CLK_VCC3V3 ac ripple unload