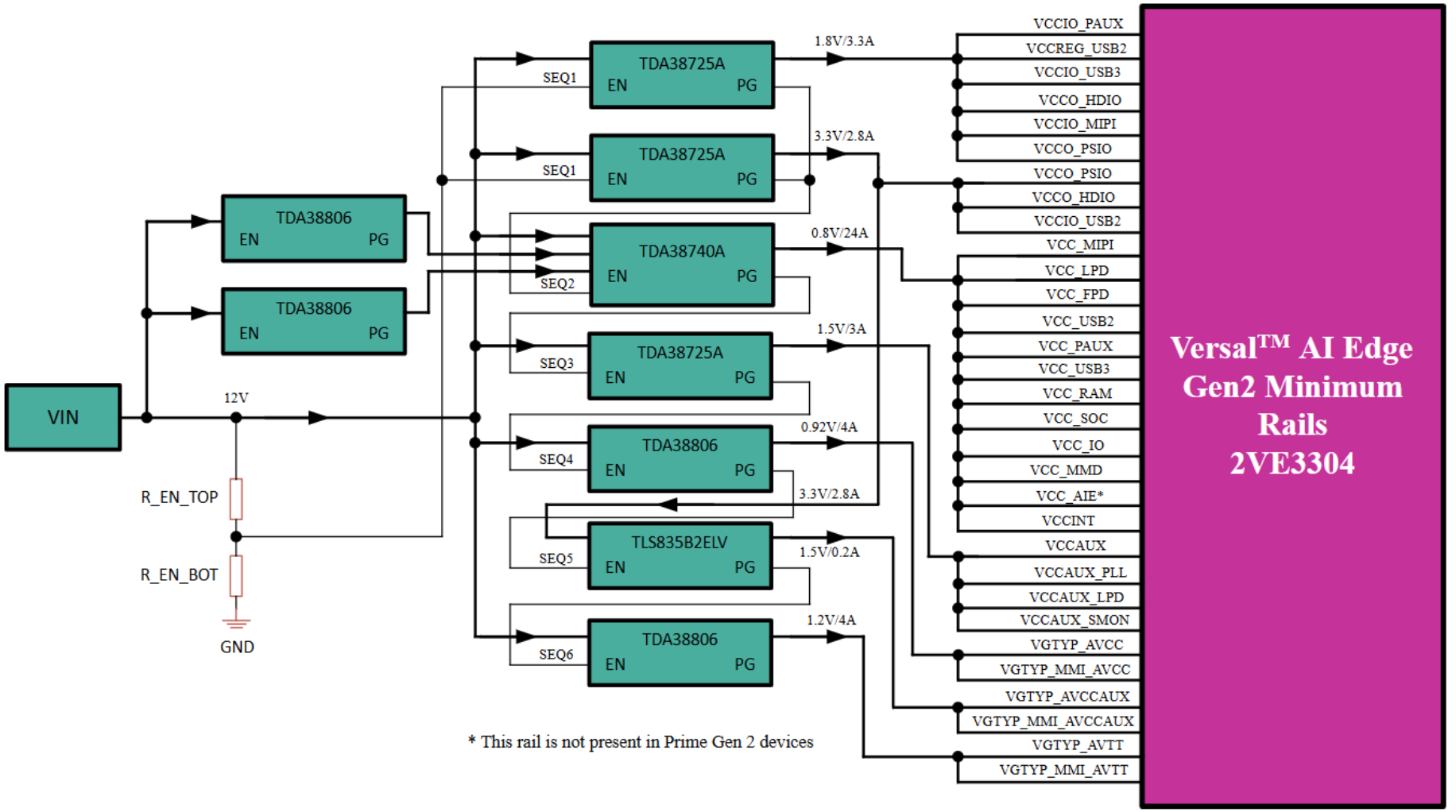
Power tree for Versal™ AI Edge Series Gen 2 and Versal™ Prime Series Gen 2 Minimum Rails

August 2026

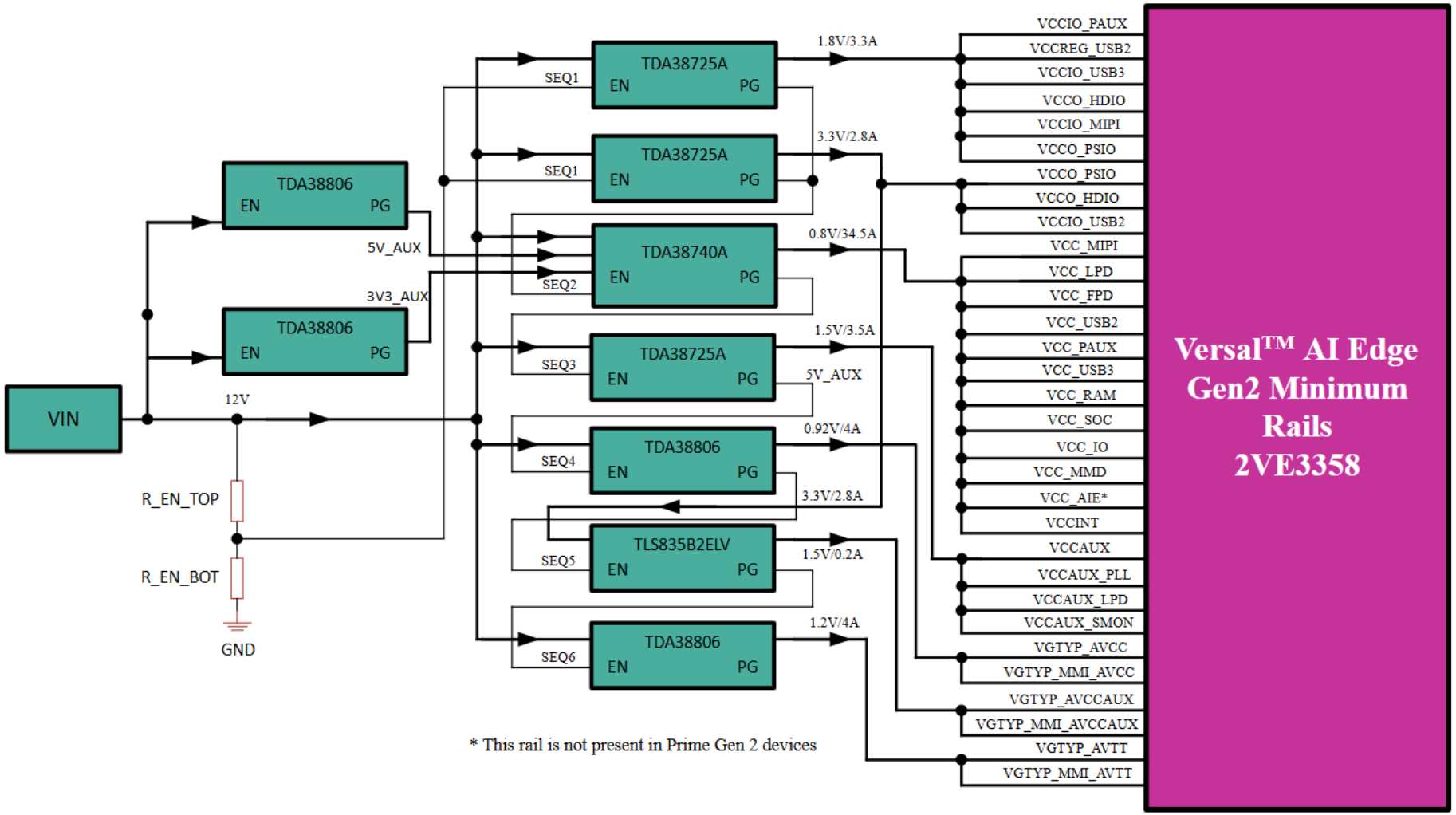
Power estimation for Versal™ AI Edge Series Gen 2 Minimum Rails

							Current (A)					
Sequence	**Rail group**	**Combined rails**	**Nominal voltage (V)**	**DC tolerance**	**AC transient Margin**	**Step load (%)**	**2VE3304**	**2VE3358**	**2VE3504**	**2VE3558**	**2VE3804**	**2VE3858**
2	0V8 (Digital)	VCC_MIPI, VCC_LPD, VCC_FPD, VCC_USB2, VCC_PAUX, VCC_USB3, VCC_RAM, VCC_SOC, VCC_IO, VCC_MMD, VCC_AIE*, VCCINT	0.8	±1%	±17mV	33	24 TDA38740A	34.5 TDA38740A	49.5 XDPE19283 2x TDA21590	60 XDPE19283 2x TDA21590	81.5 XDPE19283 3x TDA21590	92 XDPE19283 3x TDA21590
3	1V5 (Digital)	VCCAUX, VCCAUX_PLL, VCCAUX_LPD, VCCAUX_SMON	1.5	±1%	±2%	100	3 TDA38725A	3.5 TDA38725A	4 TDA38725A	5 TDA38725A	5.5 TDA38725A	6 TDA38725A
4	0V92 (Analog)	VGTYP_AVCC**, VGTYP_MMI_AVCC**	0.92	±1%	±2%	70	4 TDA38806	4 TDA38806	4.5 TDA38806	4.5 TDA38806	5 TDA38806	5 TDA38806
5	1V5 (Analog)	VGTYP_AVCCAUX**, VGTYP_MMI_AVCCAUX**	1.5	±1%	±2%	70	0.2 TLS835B2ELV	0.2 TLS835B2ELV	0.2 TLS835B2ELV	0.2 TLS835B2ELV	0.2 TLS835B2ELV	0.2 TLS835B2ELV
6	1V2 (Analog)	VGTYP_AVTT**, VGTYP_MMI_AVTT**	1.2	±1%	±2%	70	4 TDA38806	4 TDA38806	4.5 TDA38806	4.5 TDA38806	5 TDA38806	5 TDA38806
1	1V8 (Digital)	VCCIO_PAUX, VCCREG_USB2, VCCIO_USB3, VCCO_HDIO, VCCIO_MIPI, VCCO_PSIO	1.8	±1%	±2%	100	3.3 TDA38725A	3.3 TDA38725A	3.8 TDA38725A	3.8 TDA38725A	4.3 TDA38725A	4.3 TDA38725A
1	3V3 (Digital)	VCCO_PSIO, VCCO_HDIO, VCCIO_USB2	3.3	±1%	-50	100	2.8 TDA38725A	2.8 TDA38725A	3.3 TDA38725A	3.3 TDA38725A	3.8 TDA38725A	3.8 TDA38725A

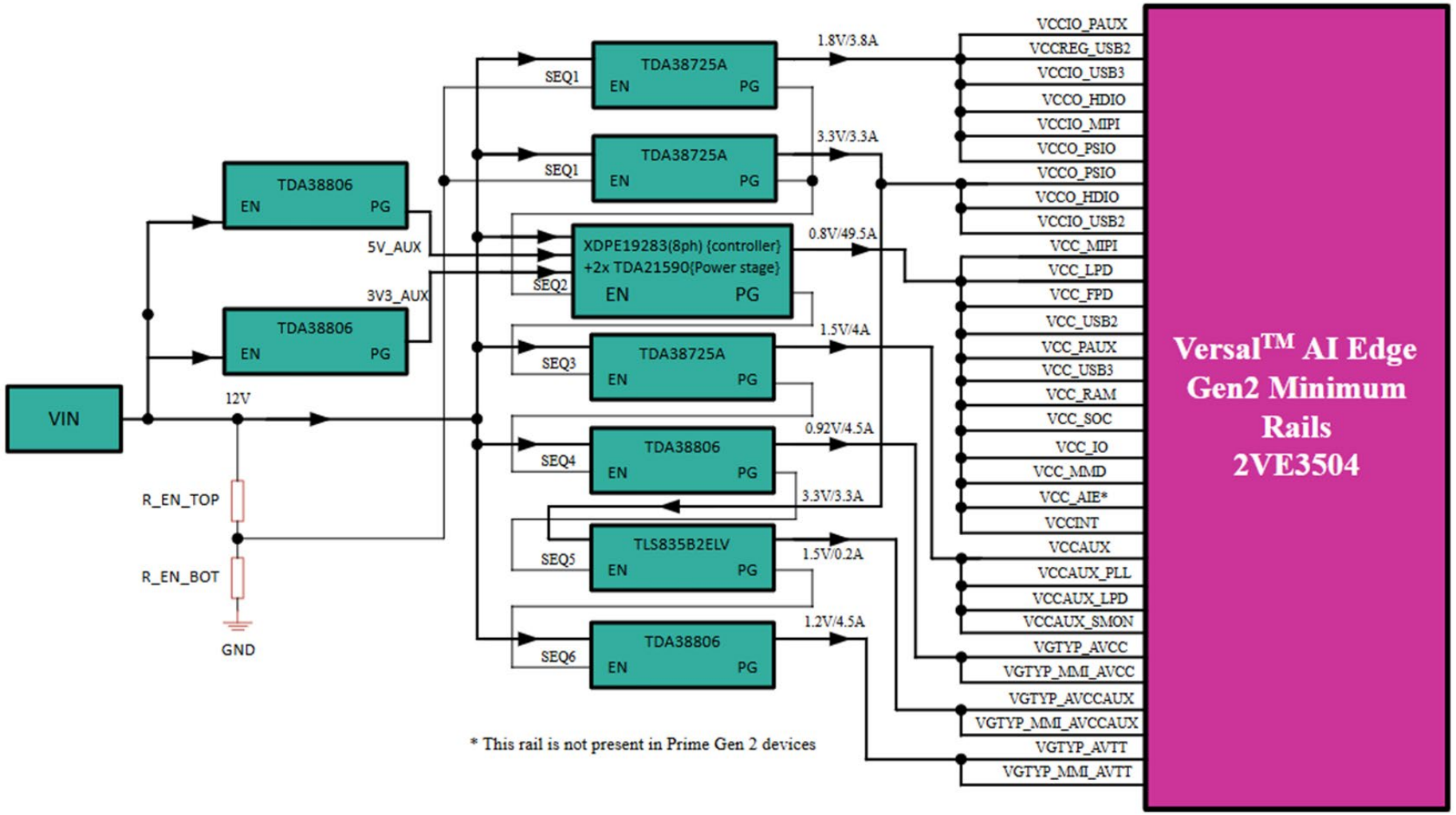
Versal™ AI Edge Series Gen 2 Minimum Rails for 2VE3304



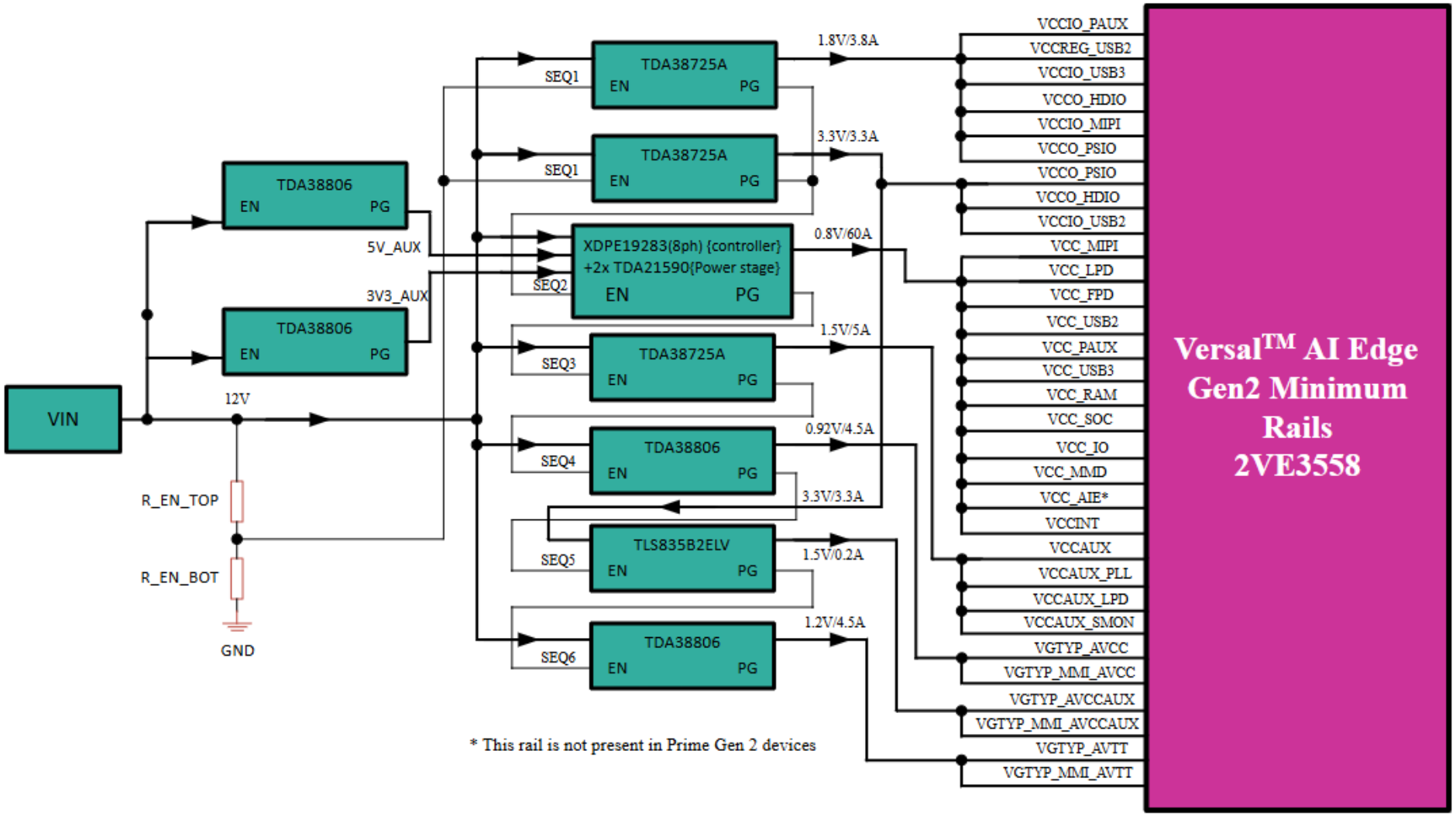
Versal™ AI Edge Series Gen 2 Minimum Rails for 2VE3358



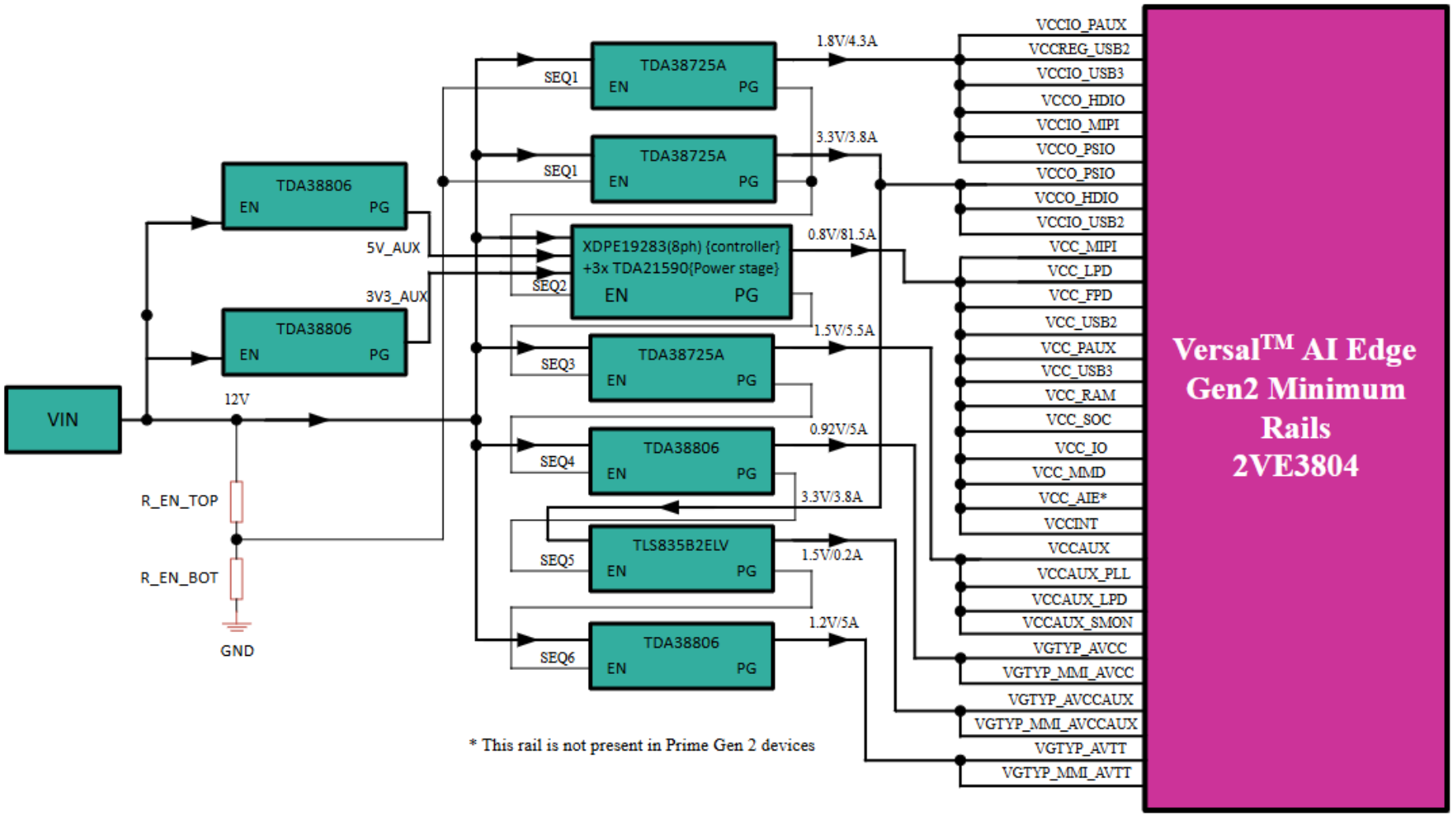
Versal™ AI Edge Series Gen 2 Minimum Rails for 2VE3504



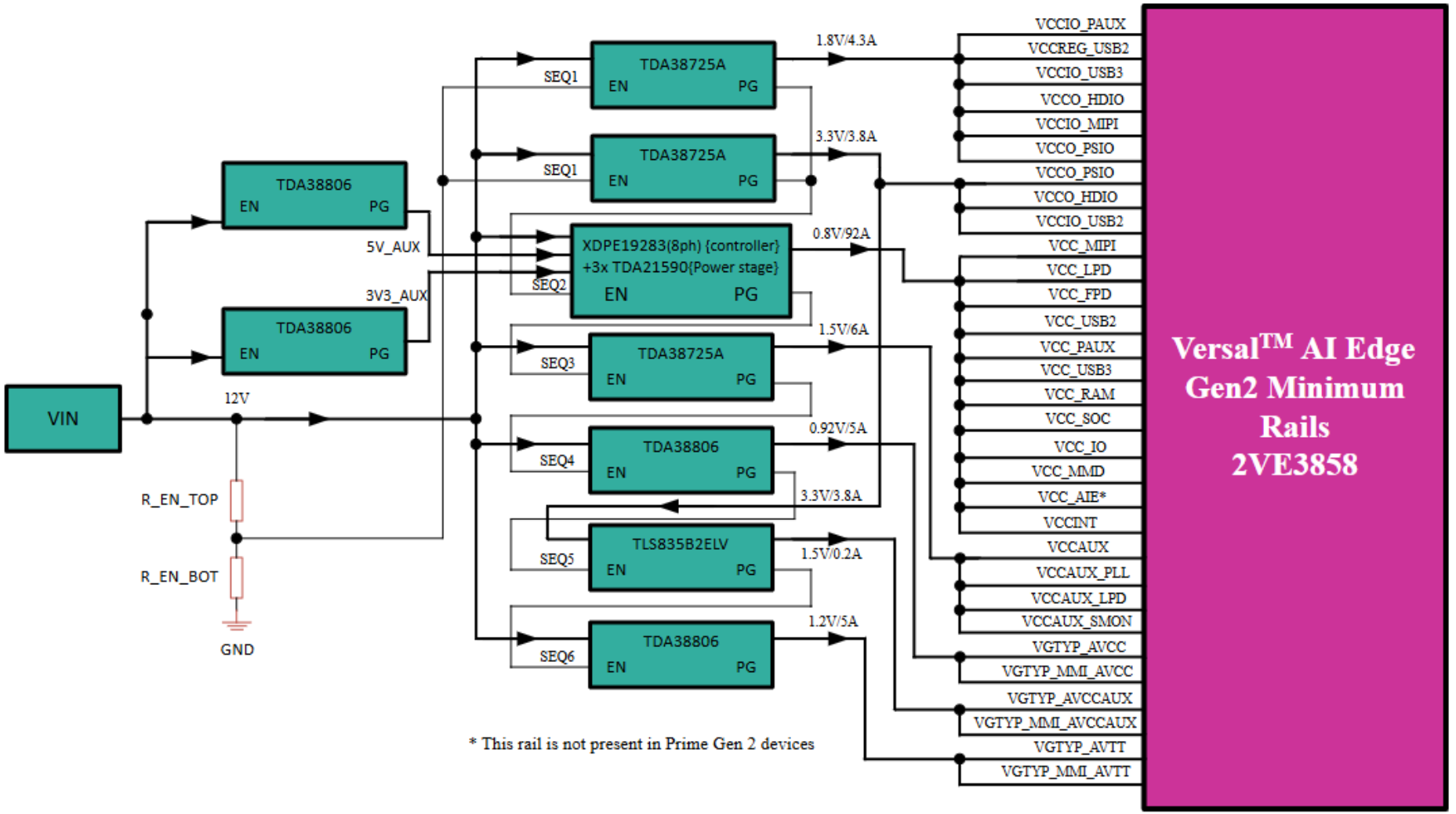
Versal™ AI Edge Series Gen 2 Minimum Rails for 2VE3558



Versal™ AI Edge Series Gen 2 Minimum Rails for 2VE3804



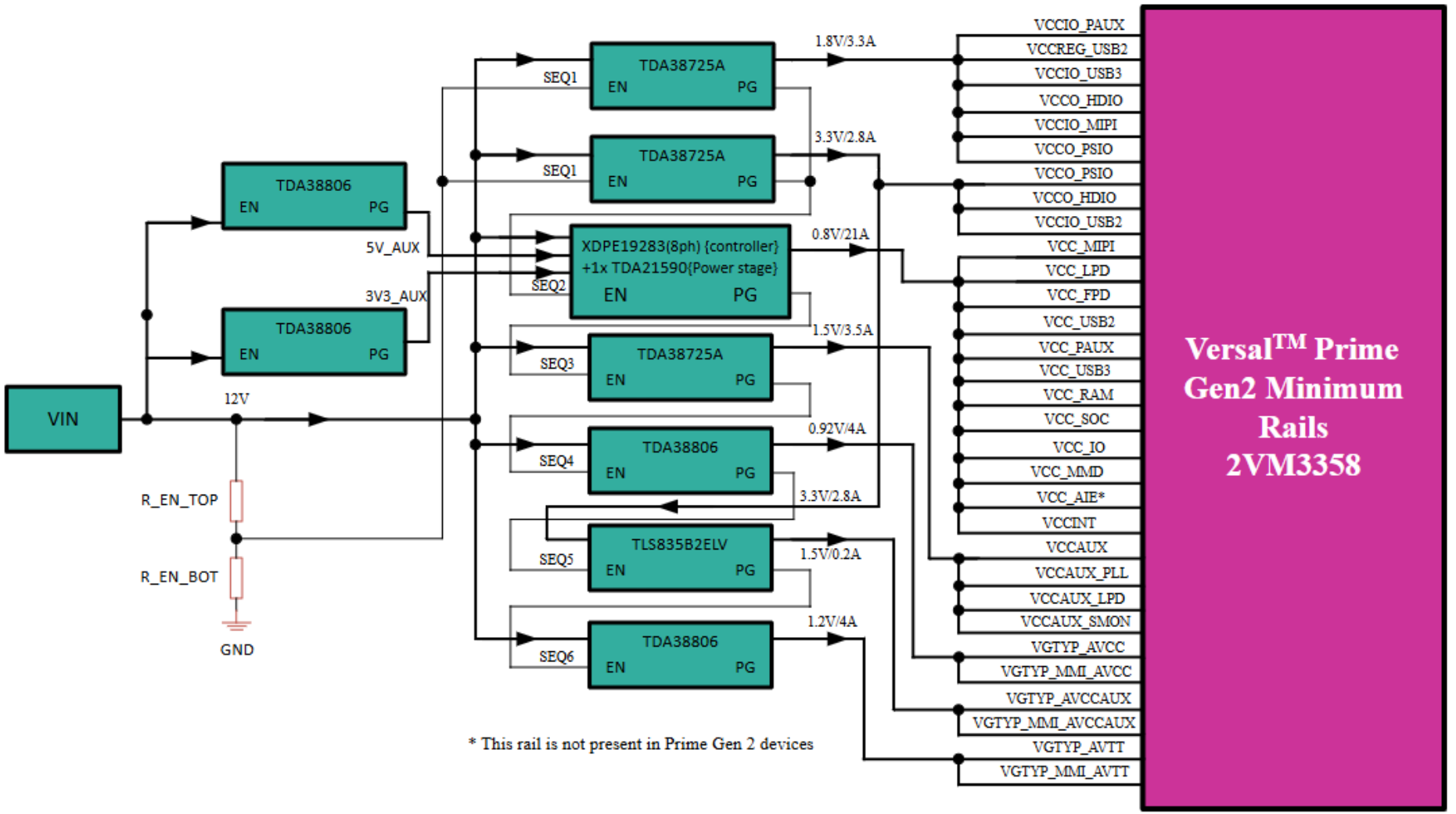
Versal™ AI Edge Series Gen 2 Minimum Rails for 2VE3858



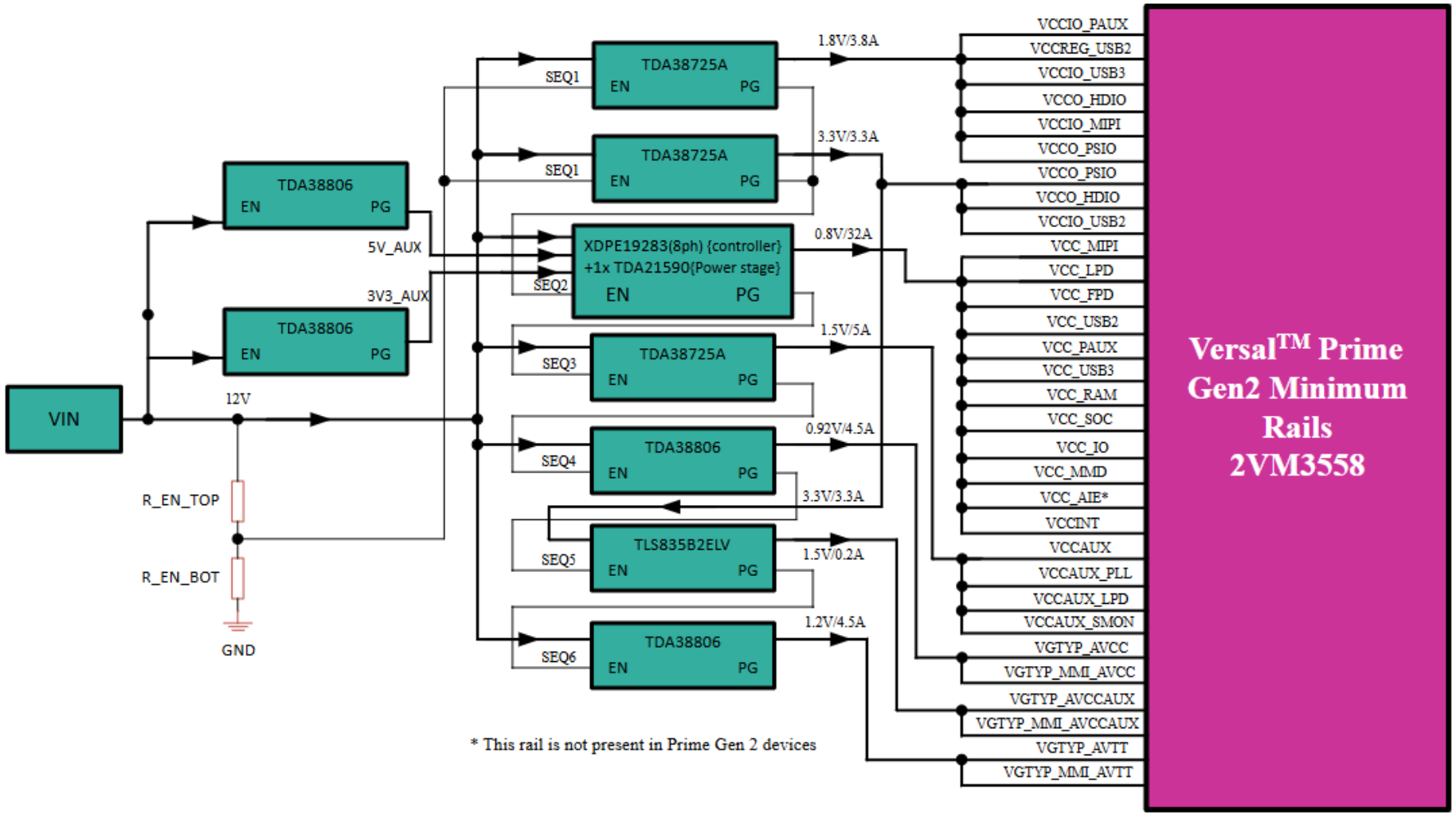
Power estimation for Versal™ Prime Series Gen 2 Minimum Rails

							Current (A)			
Sequence	**Rail group**	**Combined rails**	**Nominal voltage (V)**	**DC tolerance**	**AC transient margin**	**Step load (%)**	**2VM3358**	**2VM3558**	**2VM3654**	**2VM3858**
2	0V8 (Digital)	VCC_MIPI, VCC_LPD, VCC_FPD, VCC_USB2, VCC_PAUX, VCC_USB3, VCC_RAM, VCC_SOC, VCC_IO, VCC_MMD, VCCINT	0.8	±1%	±17mV	33	21 XDPE19283 1x TDA21590A	32 XDPE19283 1x TDA21590A	36 XDPE19283 2x TDA21590A	48 XDPE19283 3x TDA21590A
3	1V5 (Digital)	VCCAUX, VCCAUX_PLL, VCCAUX_LPD, VCCAUX_SMON	1.5	±1%	±2%	100	3.5 TDA38725A	5 TDA38725A	6 TDA38725A	6 TDA38725A
4	0V92 (Analog)	VGTYP_AVCC**, VGTYP_MMI_AVCC**	0.92	±1%	±2%	70	4 TDA38806	4.5 TDA38806	5 TDA38806	5 TDA38806
5	1V5 (Analog)	VGTYP_AVCCAUX**, VGTYP_MMI_AVCCAUX**	1.5	±1%	±2%	70	0.2 TLS835B2ELV	0.2 TLS835B2ELV	0.2 TLS835B2ELV	0.2 TLS835B2ELV
6	1V2 (Analog)	VGTYP_AVTT**, VGTYP_MMI_AVTT**	1.2	±1%	±2%	70	4 TDA38806	4.5 TDA38806	5 TDA38806	5 TDA38806
1	1V8 (Digital)	VCCIO_PAUX, VCCREG_USB2, VCCIO_USB3, VCCO_HDIO, VCCIO_MIPI, VCCO_PSIO	1.8	±1%	±2%	100	3.3 TDA38725A	3.8 TDA38725A	4.3 TDA38725A	4.3 TDA38725A
1	3V3 (Digital)	VCCO_PSIO, VCCO_HDIO, VCCIO_USB2	3.3	±1%	-50	100	2.8 TDA38725A	3.3 TDA38725A	3.5 TDA38725A	3.8 TDA38725A

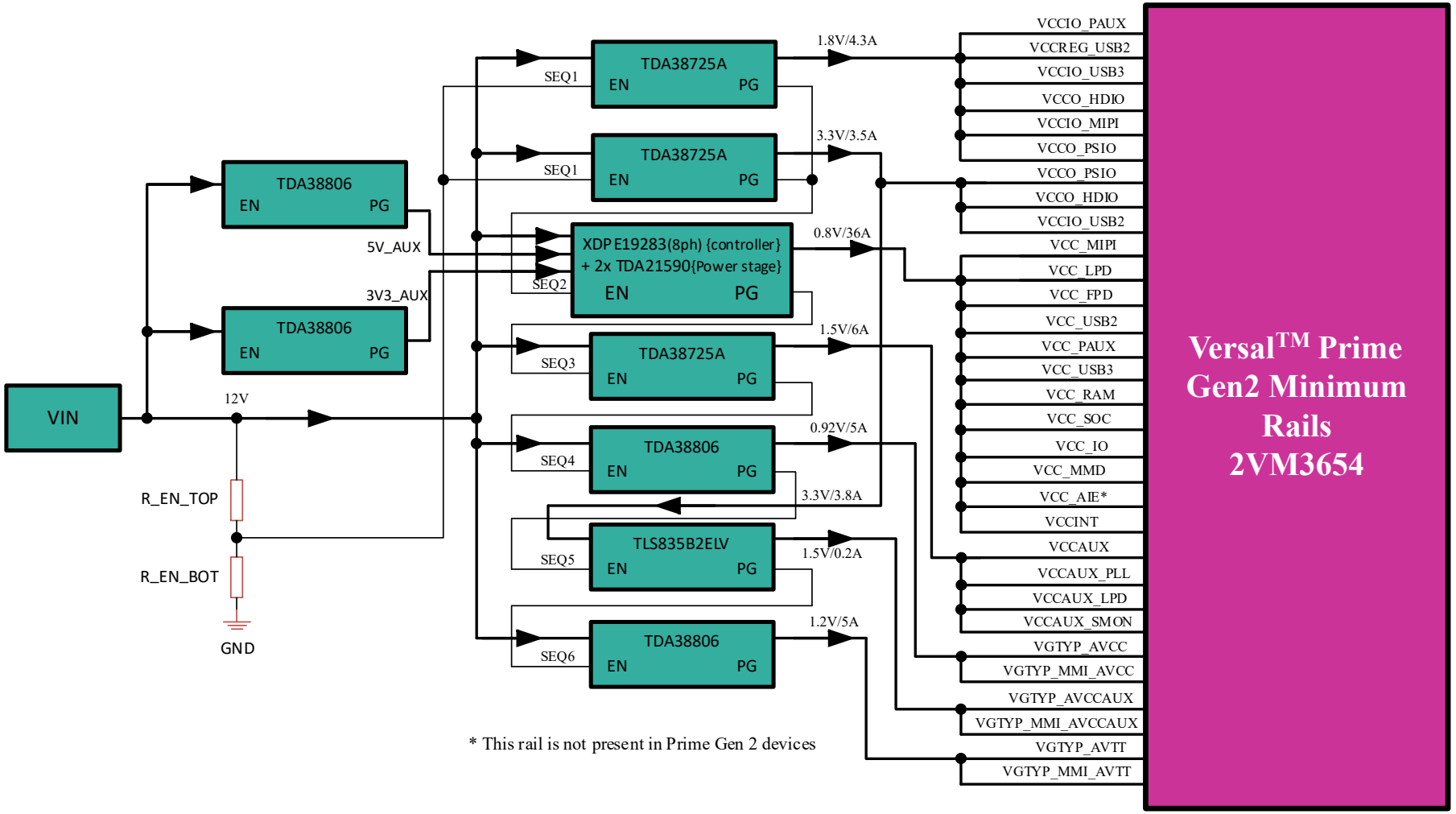
Versal™ Prime Series Gen 2 Minimum Rails for 2VM3358



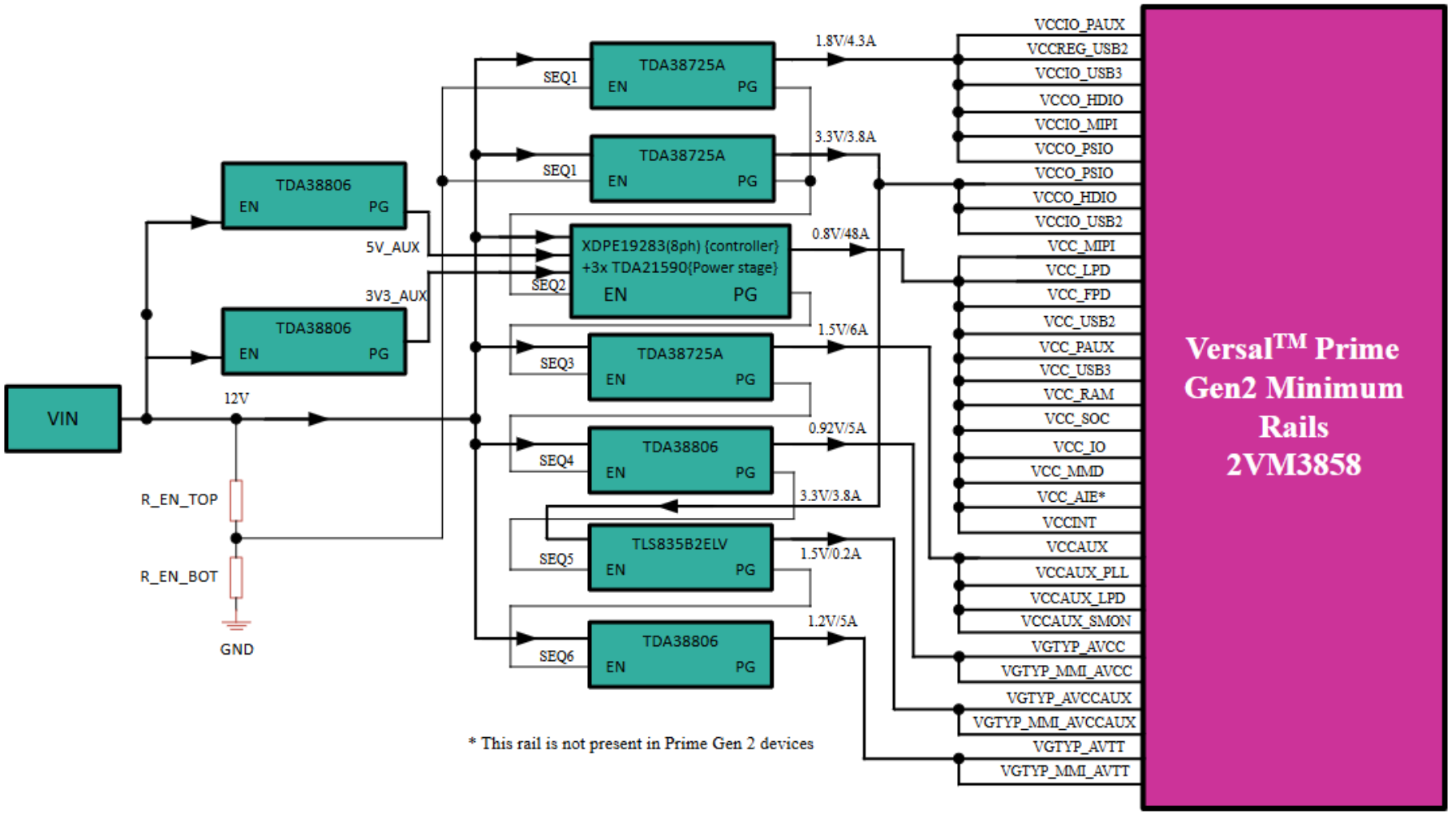
Versal™ Prime Series Gen 2 Minimum Rails for 2VM3558



Versal™ Prime Series Gen 2 Minimum Rails for 2VM3654



Versal™ Prime Series Gen 2 Minimum Rails for 2VM3858




Infineon