KINTEX ULTRASCALE DEVELOPMENT BOARD	
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KINTEX ULTRASCALE DEVELOPMENT BOARD

10/2/2015

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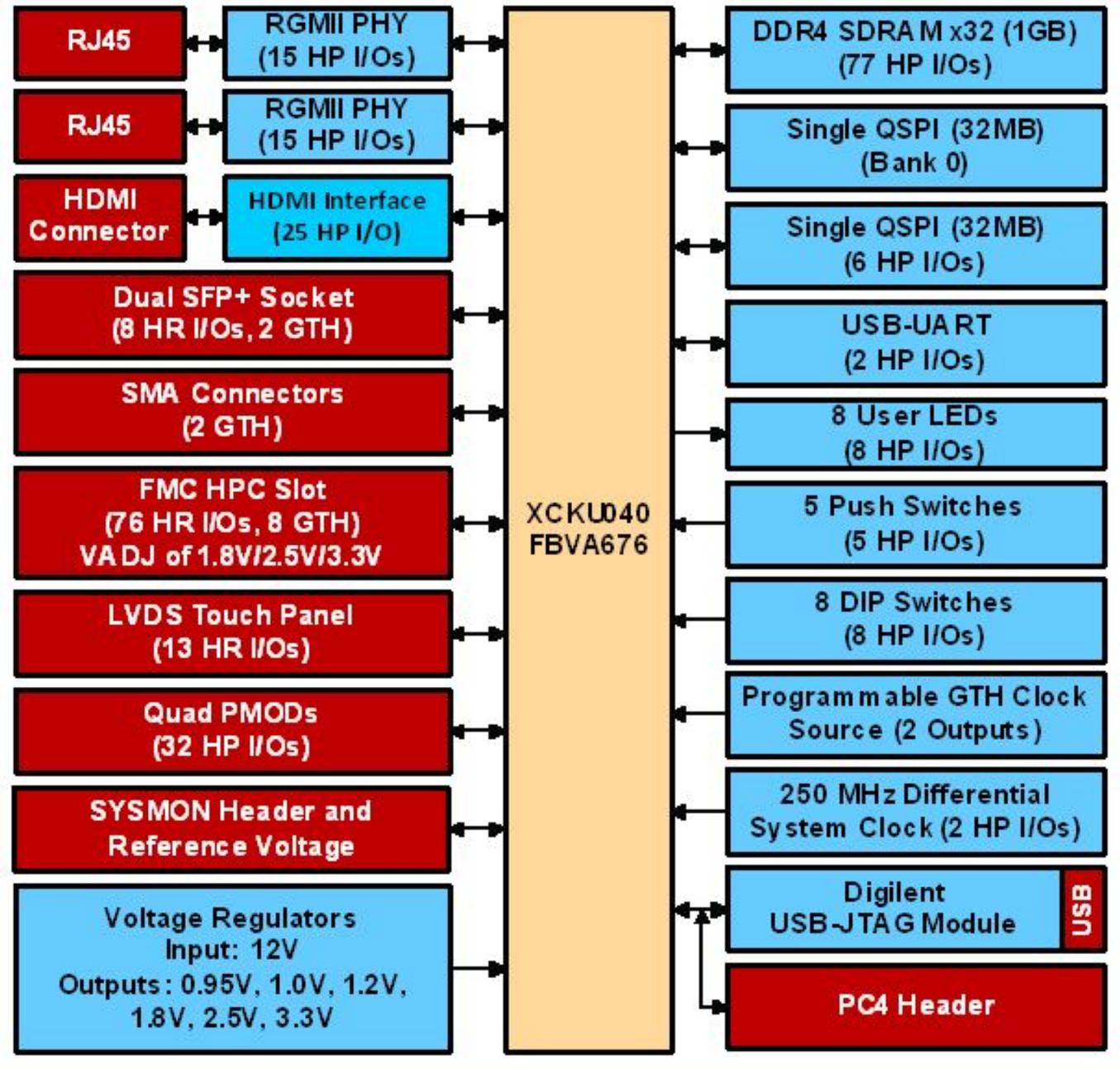
Sheet Title: Cover Sheet			
Size: B	Document Name: Kintex UltraScale Development Board	Variant Description: KU040-DB-PRJ-B-01-00	Rev: B
Date: 10/2/2015	Doc Num: KU040-DB-SCH-B	Sheet: 1 of 14	



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Sheet Title: Block Diagram			
Size: B	Document Name: Kintex UltraScale Development Board	Variant Description: KU040-DB-PRJ-B-01-00	Rev: B
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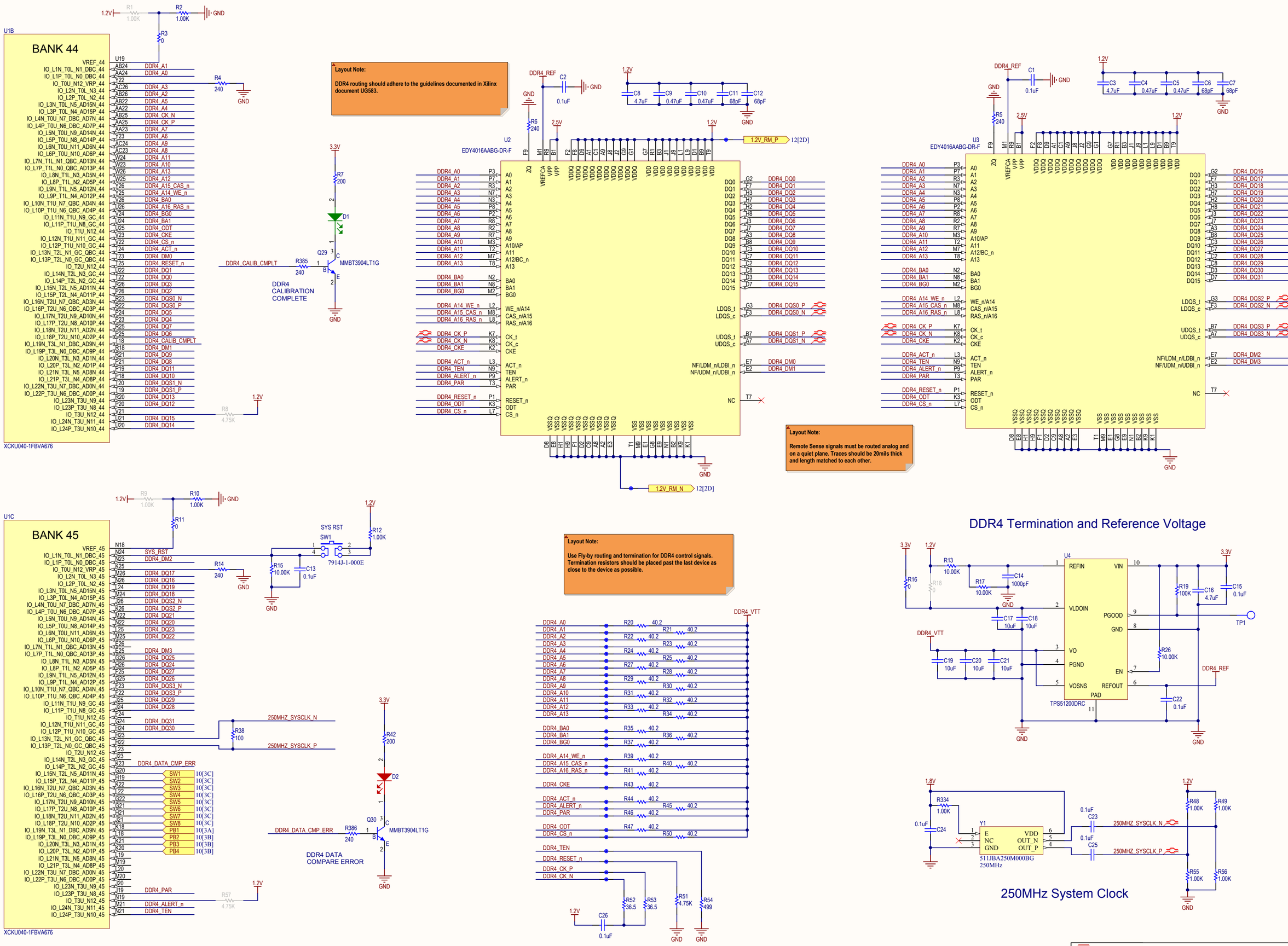
U1B
BANK 44
XCKU040-1FBVA676
U19
R1 1.00K
R2 1.00K
R3 0
R4 240
R8 4.75K
Layout Note:
DDR4 routing should adhere to the guidelines documented in Xilinx document UG583.
DDR4_REF
C2 0.1uF
C8 4.7uF
C9 0.47uF
C10 0.47uF
C11 68pF
C12 68pF
R6 240
U2
EDY4016AABG-DR-F
1.2V_RM_P 12[2D]
1.2V_RM_N 12[2D]
R7 200
D1
Q29 MMBT3904LT1G
R385 240
DDR4_CALIB_CMPLT
DDR4 CALIBRATION COMPLETE
U3
EDY4016AABG-DR-F
C1 0.1uF
C3 4.7uF
C4 0.47uF
C5 0.47uF
C6 68pF
C7 68pF
R5 240
Layout Note:
Remote Sense signals must be routed analog and on a quiet plane. Traces should be 20mils thick and length matched to each other.
U1C
BANK 45
XCKU040-1FBVA676
R9 1.00K
R10 1.00K
R11 0
R14 240
R15 10.00K
C13 0.1uF
SYS RST
SW1
7914J-1-000E
R12 1.00K
R57 4.75K
R38 100
250MHZ_SYSCLK_N
250MHZ_SYSCLK_P
DDR4_DATA_CMP_ERR
R42 200
D2
Q30 MMBT3904LT1G
R386 240
DDR4 DATA COMPARE ERROR
Layout Note:
Use Fly-by routing and termination for DDR4 control signals. Termination resistors should be placed past the last device as close to the device as possible.
DDR4_VTT
R20 40.2
R21 40.2
R22 40.2
R23 40.2
R24 40.2
R25 40.2
R27 40.2
R28 40.2
R29 40.2
R30 40.2
R31 40.2
R32 40.2
R33 40.2
R34 40.2
R35 40.2
R36 40.2
R37 40.2
R39 40.2
R40 40.2
R41 40.2
R43 40.2
R44 40.2
R45 40.2
R46 40.2
R47 40.2
R50 40.2
R52 36.5
R53 36.5
R51 4.75K
R54 499
C26 0.1uF
DDR4 Termination and Reference Voltage
U4
TPS51200DRC
R13 10.00K
R16 0
R17 10.00K
R18 0
C14 1000pF
C17 10uF
C18 10uF
C19 10uF
C20 10uF
C21 10uF
R19 100K
C16 4.7uF
C15 0.1uF
R26 10.00K
C22 0.1uF
TP1
250MHz System Clock
R334 1.00K
C24 0.1uF
Y1
511JBA250M000BG
250MHz
C23 0.1uF
C25 0.1uF
R48 1.00K
R49 1.00K
R55 1.00K
R56 1.00K
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Sheet Title: DDR4
Size: B
Document Name: Kintex UltraScale Development Board
Variant Description: KU040-DB-PRJ-B-01-00
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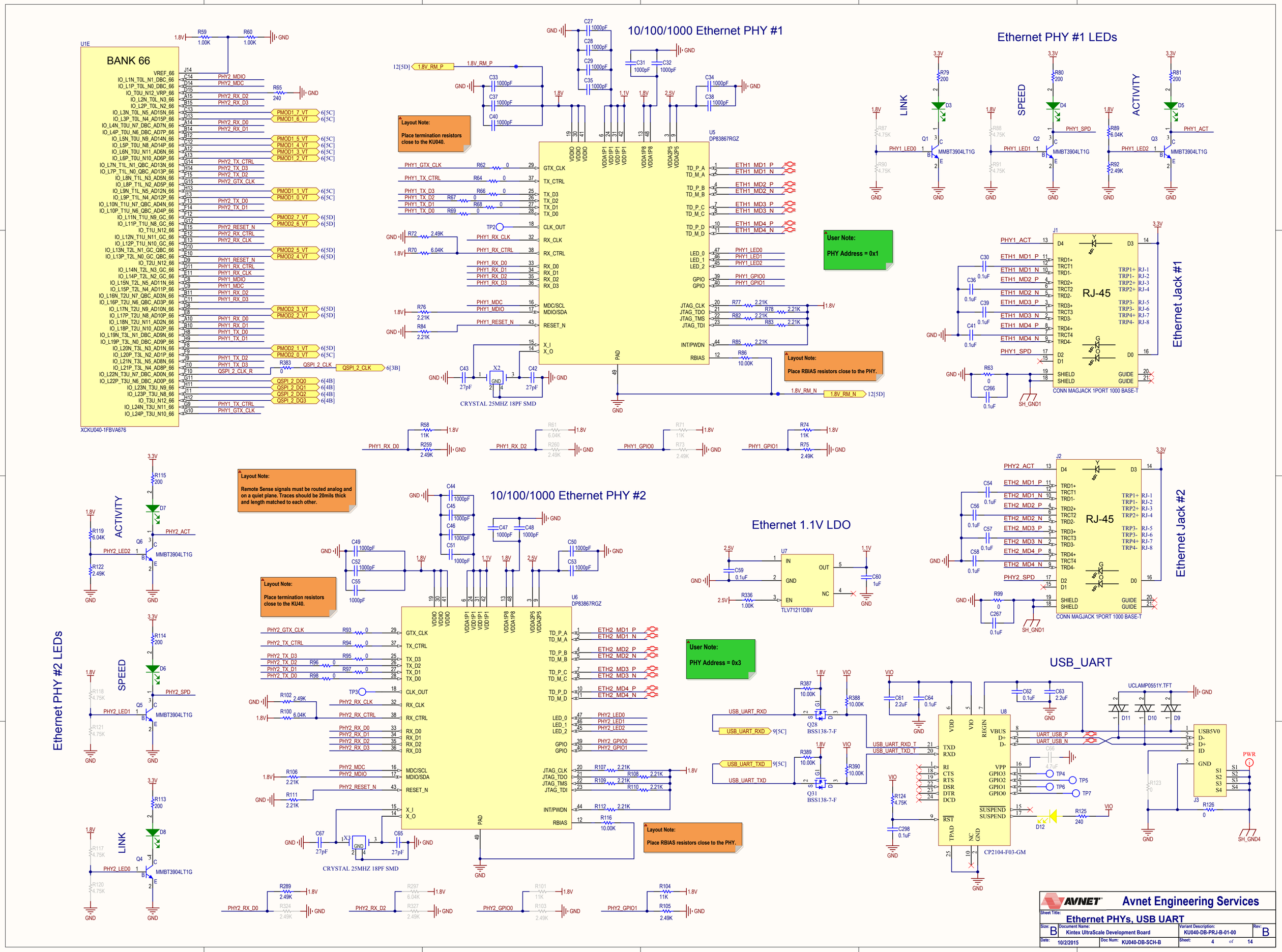

10/100/1000 Ethernet PHY #1
Ethernet PHY #1 LEDs
BANK 66
U1E
XCKU040-1FBVA676
U5
DP83867RGZ
Layout Note:
Place termination resistors close to the KU040.
User Note:
PHY Address = 0x1
Layout Note:
Place RBIAS resistors close to the PHY.
CRYSTAL 25MHZ 18PF SMD
LINK
SPEED
ACTIVITY
MMBT3904LT1G
RJ-45
Ethernet Jack #1
CONN MAGJACK 1PORT 1000 BASE-T
Layout Note:
Remote Sense signals must be routed analog and on a quiet plane. Traces should be 20mils thick and length matched to each other.
10/100/1000 Ethernet PHY #2
Ethernet 1.1V LDO
U7
TLV71211DBV
Ethernet Jack #2
Ethernet PHY #2 LEDs
U6
DP83867RGZ
User Note:
PHY Address = 0x3
USB_UART
U8
CP2104-F03-GM
UCLAMP0551Y.TFT
USB5V0
Q28
BSS138-7-F
Q31
BSS138-7-F
Q4
Q5
Q6
Q3
Q2
Q1
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Sheet Title:
Ethernet PHYs, USB UART
Size: B
Document Name: Kintex UltraScale Development Board
Variant Description: KU040-DB-PRJ-B-01-00
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Date: 10/2/2015
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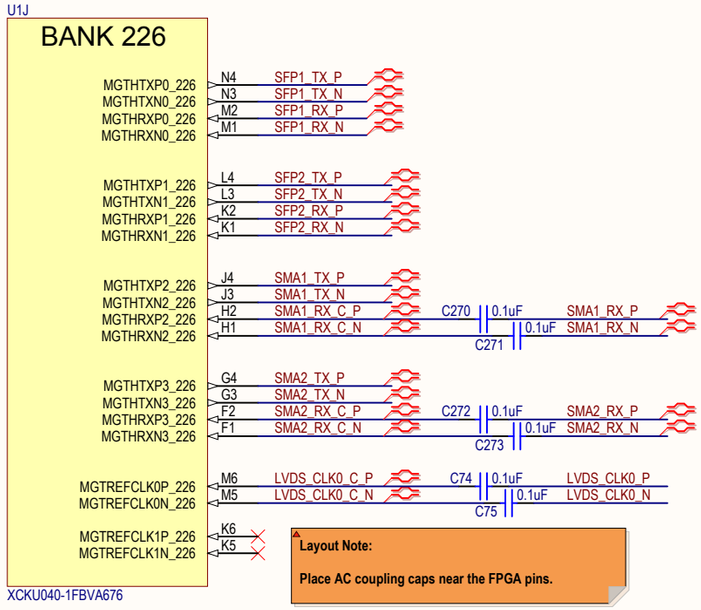
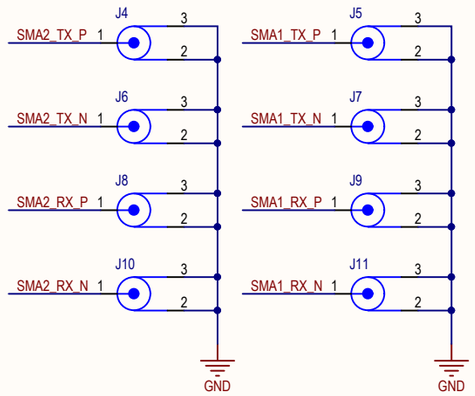
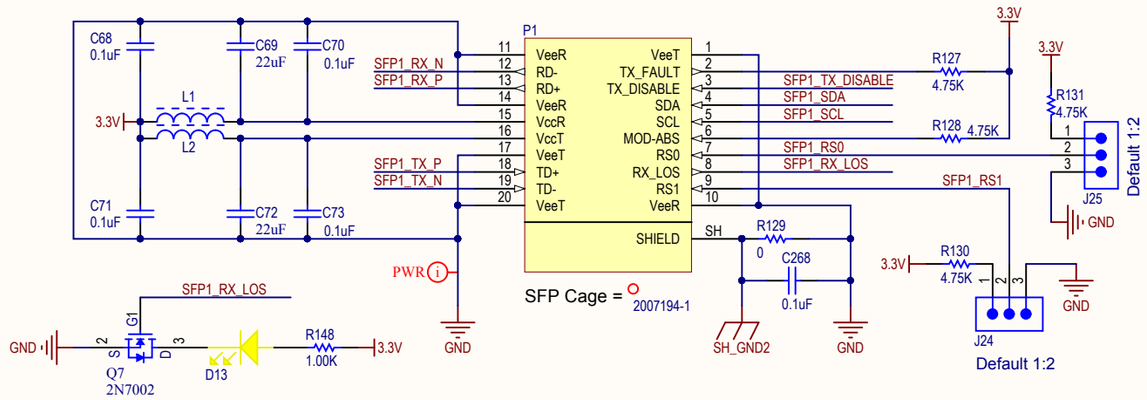


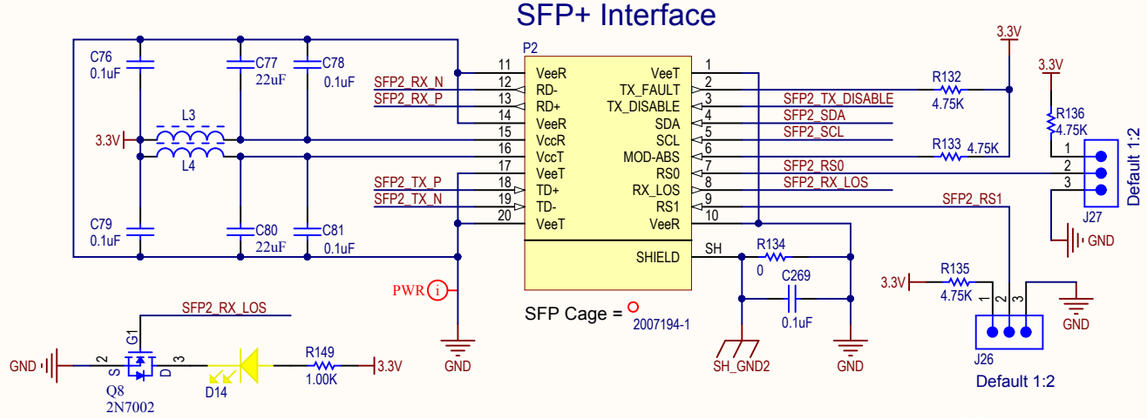
GTH SMA CONNECTORS

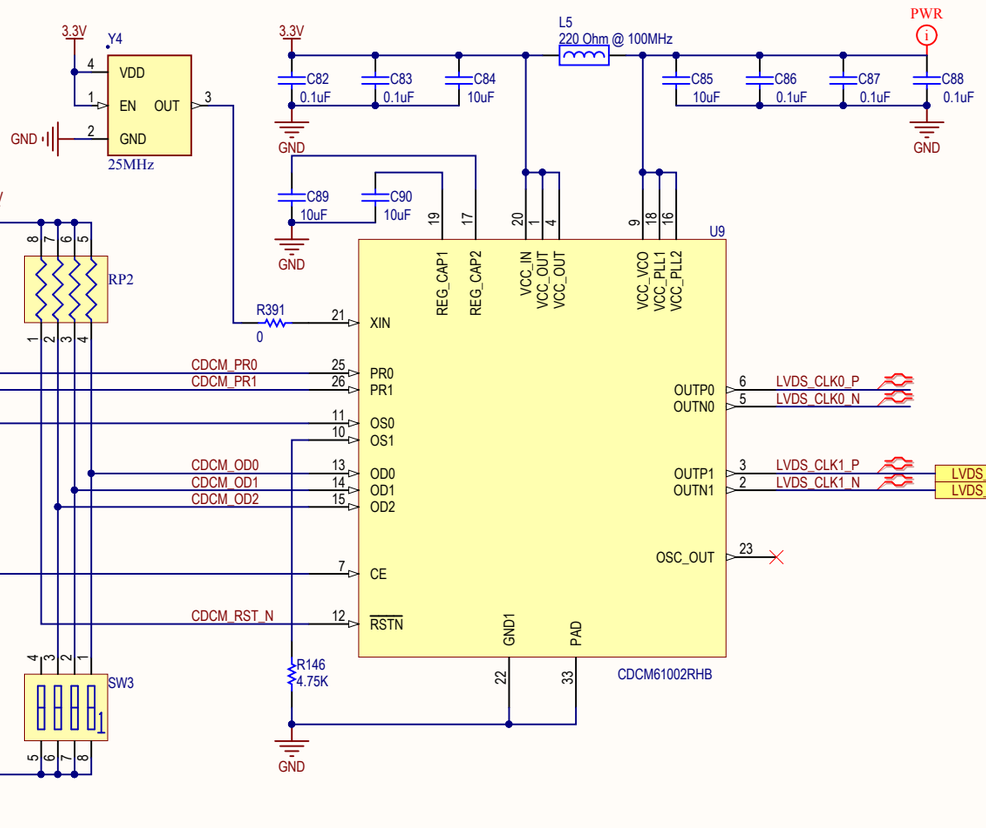


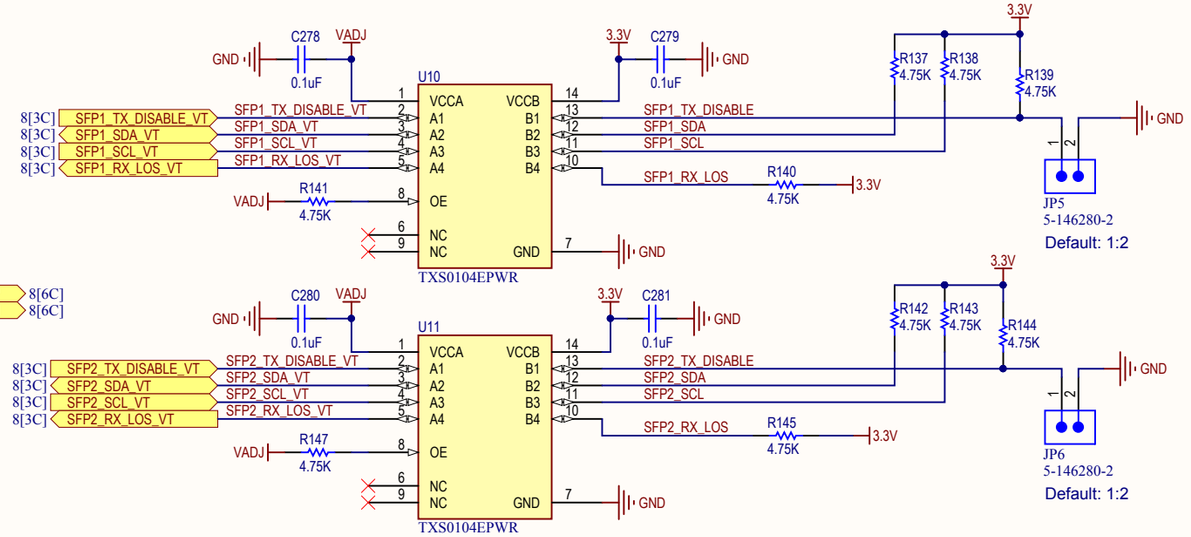
SFP+ Interface



SFP+ Interface







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Sheet Title: SFP+, LVDS Clock			
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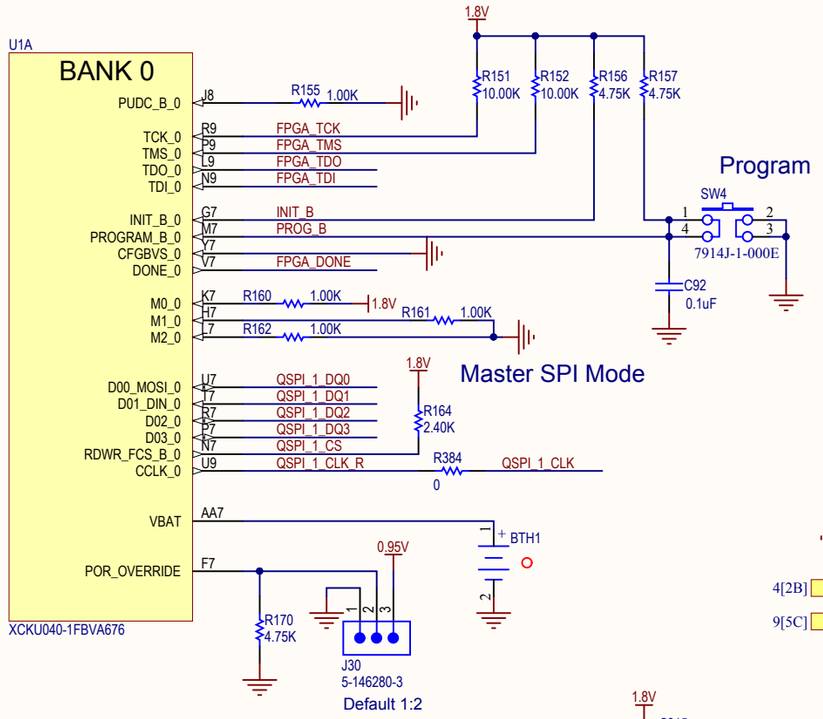
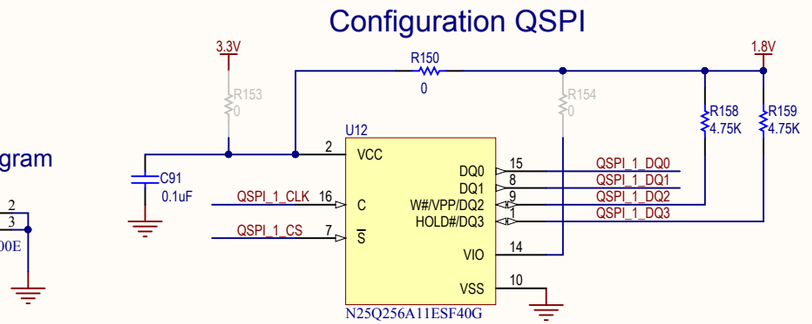
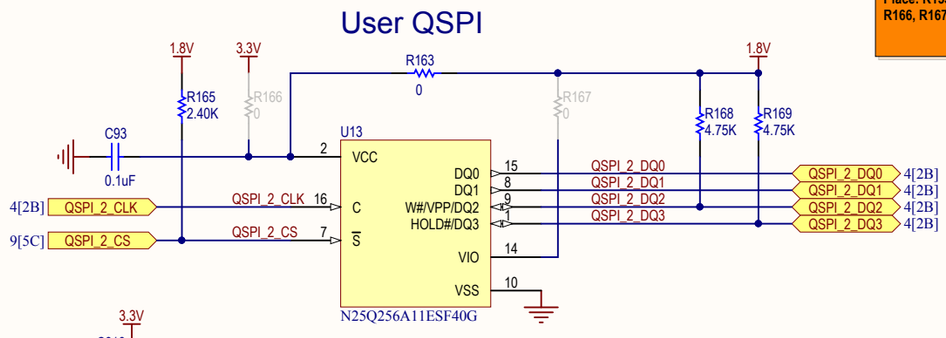






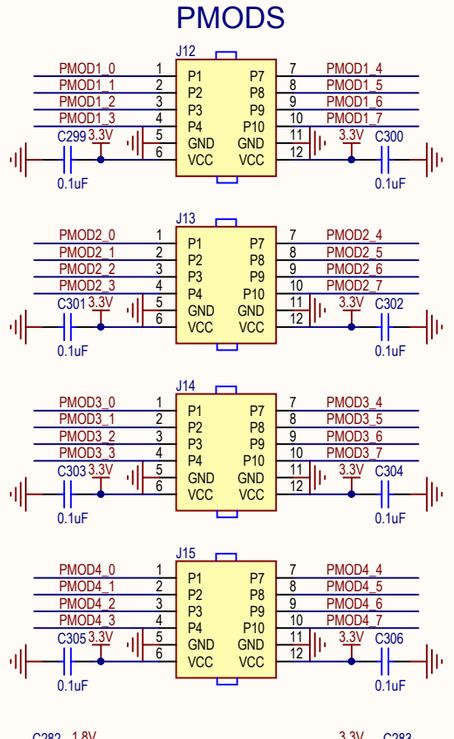
Assembly Note:

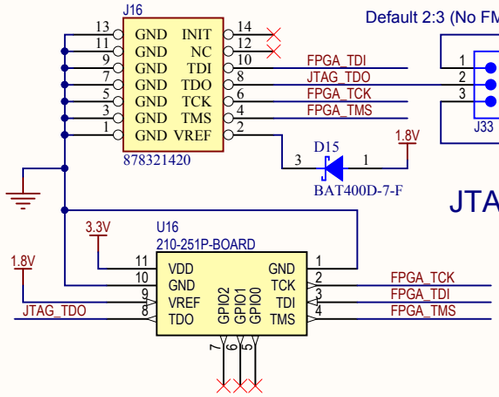
QSPI IC land patterns designed to accommodate Micron (shown) or Spansion QSPI device S25FL128SAGMFIR0.

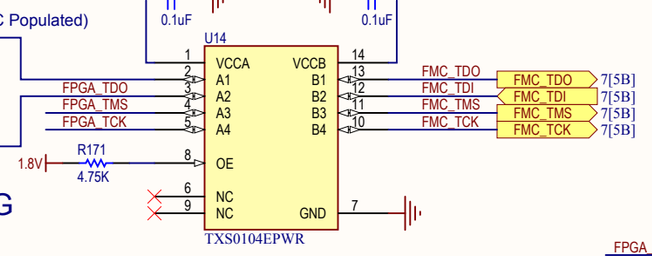
To Implement Spansion QSPI:

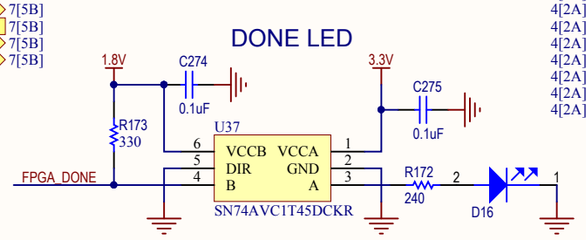
DNP: R150, R163

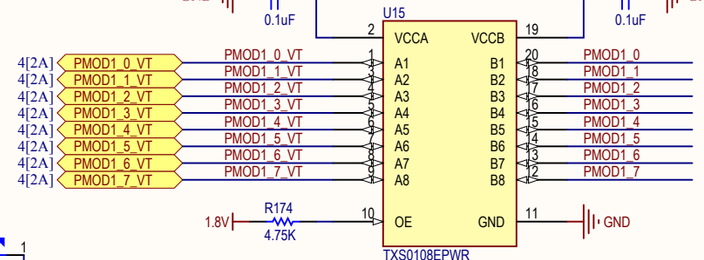
Place: R153, R154, R166, R167

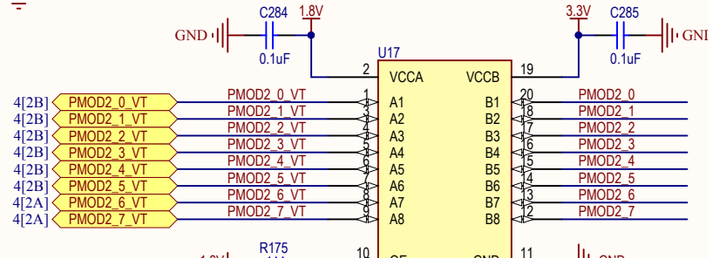




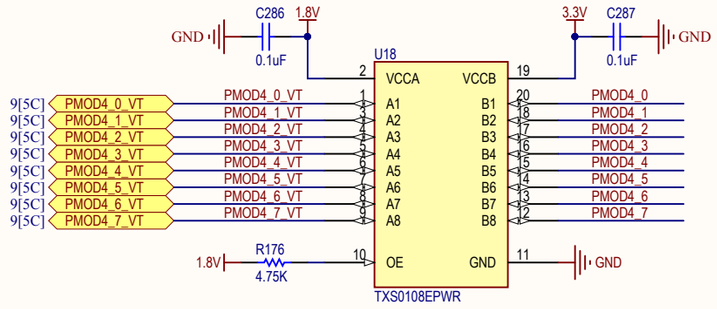


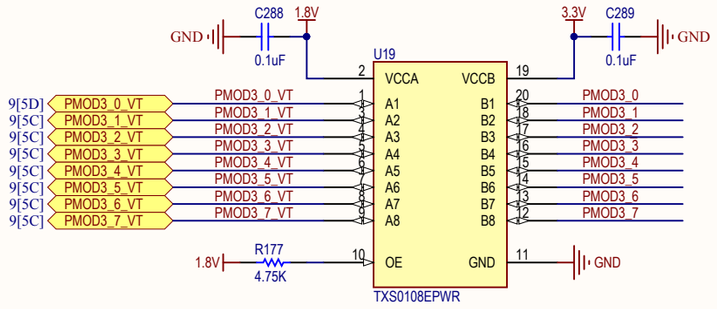






PMOD VOLTAGE TRANSLATION





Sheet Title:	QSPI, JTAG, PMODS
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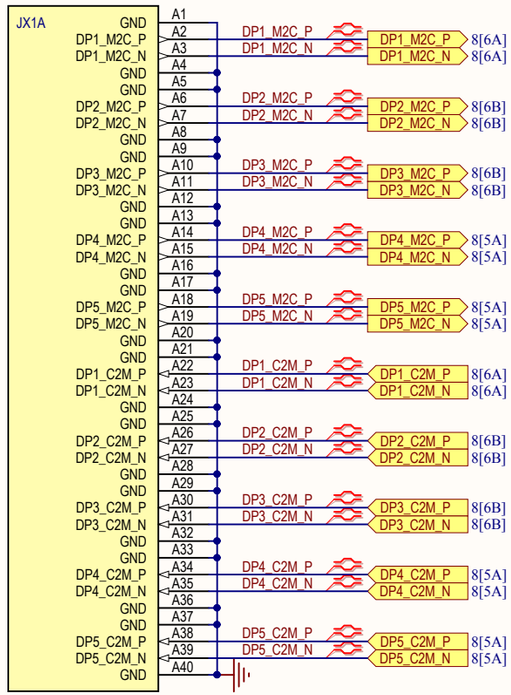

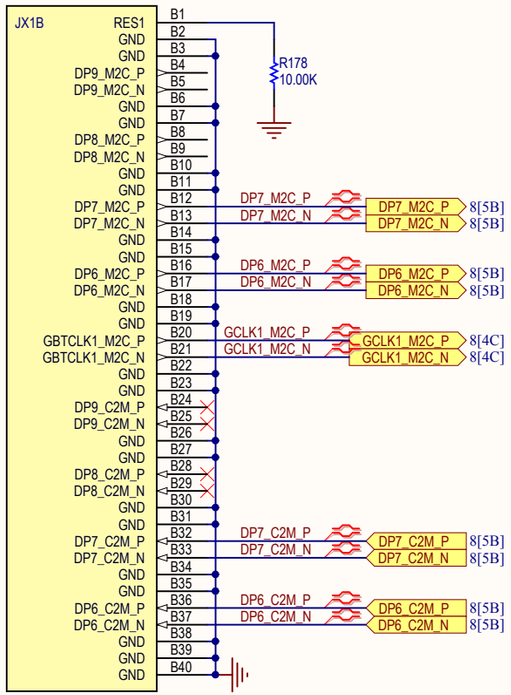

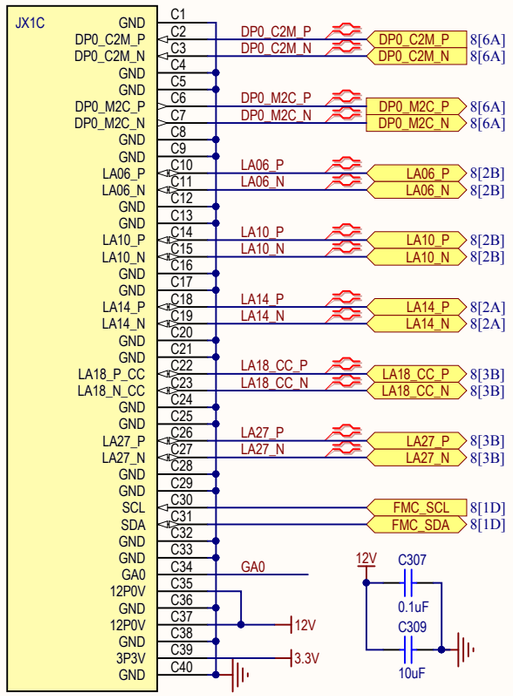

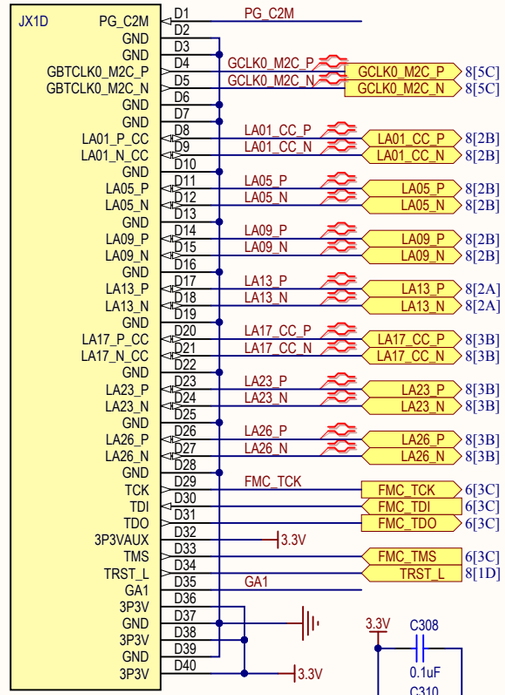

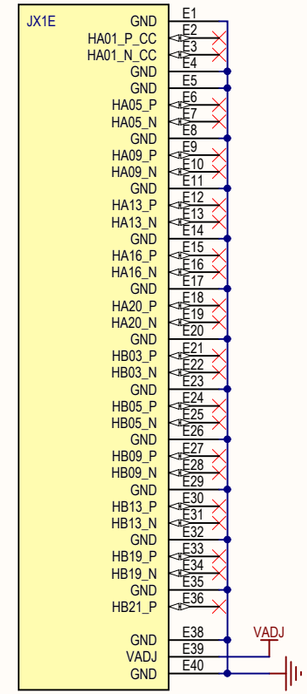

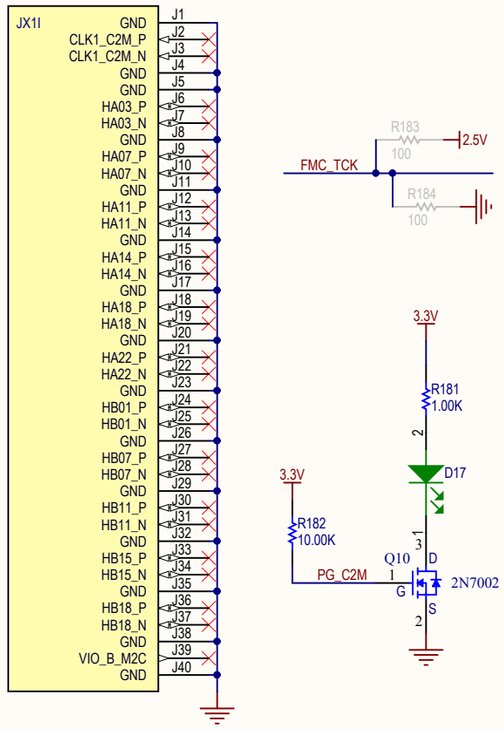

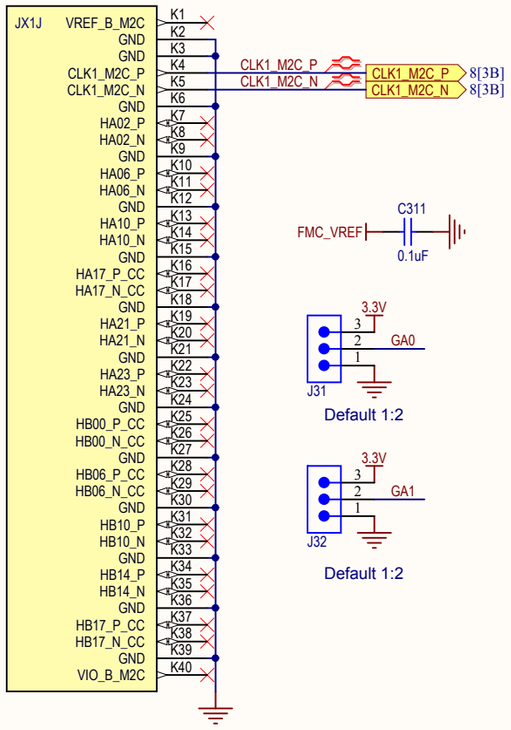

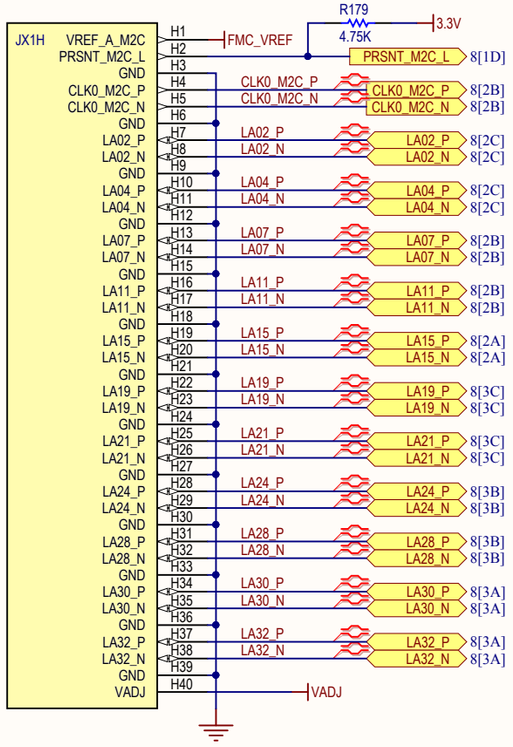

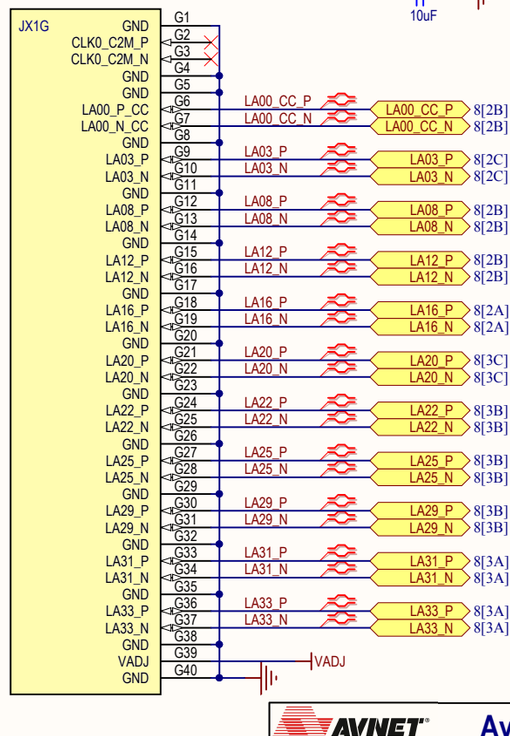

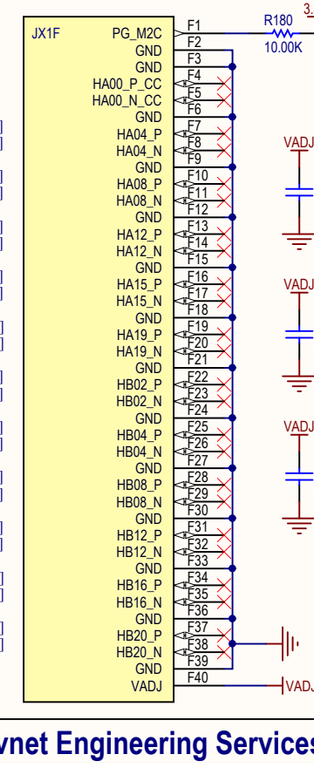

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Sheet Title: FMC FPC Connector			
Size: B	Document Name: Kintex UltraScale Development Board	Variant Description: KU040-DB-PRJ-B-01-00	Rev: B
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FMC GTH BANKS

Layout Note:
BANK 225 - Trace length from MGTAVTTRCAL pin and MGTRREF_R pin to 100 ohm resistor must be equal in length.

U1F — BANK 64

FMC_VREF — R185 4.75K — V14

VREF_64			
IO_L1N_T0L_N1_DBC_64	AF15	LA16_N	LA16_N 7[5C]
IO_L1P_T0L_N0_DBC_64	AE16	LA16_P	LA16_P 7[5C]
IO_T0U_N12_64	AE13	PWR_TMON_IO	
IO_L2N_T0L_N3_64	AF13	LA15_N	LA15_N 7[4C]
IO_L2P_T0L_N2_64	AF14	LA15_P	LA15_P 7[4C]
IO_L3N_T0L_N5_AD15N_64	AE15	LA14_N	LA14_N 7[4A]
IO_L3P_T0L_N4_AD15P_64	AD15	LA14_P	LA14_P 7[4A]
IO_L4N_T0U_N7_DBC_AD7N_64	AF12	LA13_N	LA13_N 7[5A]
IO_L4P_T0U_N6_DBC_AD7P_64	AE12	LA13_P	LA13_P 7[5A]
IO_L5N_T0U_N9_AD14N_64	AC13	LA12_N	LA12_N 7[5C]
IO_L5P_T0U_N8_AD14P_64	AC14	LA12_P	LA12_P 7[5C]
IO_L6N_T0U_N11_AD6N_64	AD13	LA11_N	LA11_N 7[4C]
IO_L6P_T0U_N10_AD6P_64	AD14	LA11_P	LA11_P 7[4C]
IO_L7N_T1L_N1_QBC_AD13N_64	AB15	LA10_N	LA10_N 7[4A]
IO_L7P_T1L_N0_QBC_AD13P_64	AA15	LA10_P	LA10_P 7[4A]
IO_L8N_T1L_N3_AD5N_64	Y15	LA09_N	LA09_N 7[5A]
IO_L8P_T1L_N2_AD5P_64	W15	LA09_P	LA09_P 7[5A]
IO_L9N_T1L_N5_AD12N_64	AB14	LA08_N	LA08_N 7[5C]
IO_L9P_T1L_N4_AD12P_64	AA14	LA08_P	LA08_P 7[5C]
IO_L10N_T1U_N7_QBC_AD4N_64	W13	LA07_N	LA07_N 7[4C]
IO_L10P_T1U_N6_QBC_AD4P_64	W14	LA07_P	LA07_P 7[4C]
IO_L11N_T1U_N9_GC_64	AA12	LA06_N	LA06_N 7[4A]
IO_L11P_T1U_N8_GC_64	AA13	LA06_P	LA06_P 7[4A]
IO_T1U_N12_64	Y13	PWR_SCL_IO	
IO_L12N_T1U_N11_GC_64	AB11	LA00_CC_N	LA00_CC_N 7[5C]
IO_L12P_T1U_N10_GC_64	AB12	LA00_CC_P	LA00_CC_P 7[5C]
IO_L13N_T2L_N1_GC_QBC_64	AC11	CLK0_M2C_N	CLK0_M2C_N 7[4C]
IO_L13P_T2L_N0_GC_QBC_64	AC12	CLK0_M2C_P	CLK0_M2C_P 7[4C]
IO_T2U_N12_64	AD10	PWR_SDA_IO	
IO_L14N_T2L_N3_GC_64	AE11	LA01_CC_N	LA01_CC_N 7[5A]
IO_L14P_T2L_N2_GC_64	AD11	LA01_CC_P	LA01_CC_P 7[5A]
IO_L15N_T2L_N5_AD11N_64	AD9	LA05_N	LA05_N 7[5A]
IO_L15P_T2L_N4_AD11P_64	AC9	LA05_P	LA05_P 7[5A]
IO_L16N_T2U_N7_QBC_AD3N_64	AF10	LA04_N	LA04_N 7[4C]
IO_L16P_T2U_N6_QBC_AD3P_64	AE10	LA04_P	LA04_P 7[4C]
IO_L17N_T2U_N9_AD10N_64	AD8	LA03_N	LA03_N 7[5C]
IO_L17P_T2U_N8_AD10P_64	AC8	LA03_P	LA03_P 7[5C]
IO_L18N_T2U_N11_AD2N_64	AB9	LA02_N	LA02_N 7[4C]
IO_L18P_T2U_N10_AD2P_64	AB10	LA02_P	LA02_P 7[4C]
IO_L19N_T3L_N1_DBC_AD9N_64	AA9	TP_D0_N	
IO_L19P_T3L_N0_DBC_AD9P_64	AA10	TP_D0_P	
IO_L20N_T3L_N3_AD1N_64	Y10	TP_D1_N	
IO_L20P_T3L_N2_AD1P_64	Y11	TP_D1_P	
IO_L21N_T3L_N5_AD8N_64	AA8	TP_D2_N	
IO_L21P_T3L_N4_AD8P_64	Y8	TP_D2_P	
IO_L22N_T3U_N7_DBC_AD0N_64	V11	TP_D3_N	
IO_L22P_T3U_N6_DBC_AD0P_64	V12	TP_D3_P	
IO_L23N_T3U_N9_64	W8	CLK_N	
IO_L23P_T3U_N8_64	W9	CLK_P	
IO_T3U_N12_64	Y12	TP_SCL_VT	
IO_L24N_T3U_N11_64	W10	TP_SDA_VT	
IO_L24P_T3U_N10_64	W11	TP_IRQ_N_VT	

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U1G — BANK 65

FMC_VREF — R186 4.75K — V17

VREF_65			
IO_L1N_T0L_N1_DBC_RS1_65	AD16	LA33_N	LA33_N 7[5D]
IO_L1P_T0L_N0_DBC_RS0_65	AC16	LA33_P	LA33_P 7[5D]
IO_T0U_N12_A28_65	AB16		
IO_L2N_T0L_N3_FWE_FCS2_B_65	AC17	LA32_N	LA32_N 7[4D]
IO_L2P_T0L_N2_FOE_B_65	AB17	LA32_P	LA32_P 7[4D]
IO_L3N_T0L_N5_AD15N_A27_65	AE18	LA31_N	LA31_N 7[5D]
IO_L3P_T0L_N4_AD15P_A26_65	AE17	LA31_P	LA31_P 7[5D]
IO_L4N_T0U_N7_DBC_AD7N_A25_65	AF20	LA30_N	LA30_N 7[4D]
IO_L4P_T0U_N6_DBC_AD7P_A24_65	AF19	LA30_P	LA30_P 7[4D]
IO_L5N_T0U_N9_AD14N_A23_65	AD18	LA29_N	LA29_N 7[5D]
IO_L5P_T0U_N8_AD14P_A22_65	AC18	LA29_P	LA29_P 7[5D]
IO_L6N_T0U_N11_AD6N_A21_65	AE18	LA28_N	LA28_N 7[4D]
IO_L6P_T0U_N10_AD6P_A20_65	AF17	LA28_P	LA28_P 7[4D]
IO_L7N_T1L_N1_QBC_AD13N_A19_65	Y16	LA27_N	LA27_N 7[4B]
IO_L7P_T1L_N0_QBC_AD13P_A18_65	W16	LA27_P	LA27_P 7[4B]
IO_L8N_T1L_N3_AD5N_A17_65	Y21	LA26_N	LA26_N 7[5B]
IO_L8P_T1L_N2_AD5P_A16_65	W21	LA26_P	LA26_P 7[5B]
IO_L9N_T1L_N5_AD12N_A15_D31_65	W19	LA25_N	LA25_N 7[5D]
IO_L9P_T1L_N4_AD12P_A14_D30_65	W18	LA25_P	LA25_P 7[5C]
IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65	V19	LA24_N	LA24_N 7[4D]
IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65	V18	LA24_P	LA24_P 7[4D]
IO_L11N_T1U_N9_GC_A11_D27_65	Y18	LA23_N	LA23_N 7[5B]
IO_L11P_T1U_N8_GC_A10_D26_65	Y17	LA23_P	LA23_P 7[5B]
IO_T1U_N12_PERSTN1_65	AA17		
IO_L12N_T1U_N11_GC_A09_D25_65	Y20	LA17_CC_N	LA17_CC_N 7[5A]
IO_L12P_T1U_N10_GC_A08_D24_65	W20	LA17_CC_P	LA17_CC_P 7[5A]
IO_L13N_T2L_N1_GC_QBC_A07_D23_65	AA20	CLK1_M2C_N	CLK1_M2C_N 7[3C]
IO_L13P_T2L_N0_GC_QBC_A06_D22_65	AA19	CLK1_M2C_P	CLK1_M2C_P 7[3C]
IO_T2U_N12_CSI_ADV_B_65	AA18		
IO_L14N_T2L_N3_GC_A05_D21_65	AB20	LA18_CC_N	LA18_CC_N 7[4B]
IO_L14P_T2L_N2_GC_A04_D20_65	AB19	LA18_CC_P	LA18_CC_P 7[4B]
IO_L15N_T2L_N5_AD11N_A03_D19_65	AD19	LA22_N	LA22_N 7[5C]
IO_L15P_T2L_N4_AD11P_A02_D18_65	AC19	LA22_P	LA22_P 7[5C]
IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65	AE21	LA21_N	LA21_N 7[4C]
IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65	AE20	LA21_P	LA21_P 7[4C]
IO_L17N_T2U_N9_AD10N_D15_65	AC21	LA20_N	LA20_N 7[5C]
IO_L17P_T2U_N8_AD10P_D14_65	AB21	LA20_P	LA20_P 7[5C]
IO_L18N_T2U_N11_AD2N_D13_65	AD21	LA19_N	LA19_N 7[4C]
IO_L18P_T2U_N10_AD2P_D12_65	AD20	LA19_P	LA19_P 7[4C]
IO_L19N_T3L_N1_DBC_AD9N_D11_65	AF22	TRST_L_VT	
IO_L19P_T3L_N0_DBC_AD9P_D10_65	AE22	FMC_SDA_VT	
IO_L20N_T3L_N3_AD1N_D09_65	AF25	FMC_SCL_VT	
IO_L20P_T3L_N2_AD1P_D08_65	AE25	PRSNT_M2C_L_VT	
IO_L21N_T3L_N5_AD8N_D07_65	AF24	SFP1_TX_DISABLE_VT	SFP1_TX_DISABLE_VT 5[4C]
IO_L21P_T3L_N4_AD8P_D06_65	AF23	SFP1_SDA_VT	SFP1_SDA_VT 5[4C]
IO_L22N_T3U_N7_DBC_AD0N_D05_65	AE26	SFP1_SCL_VT	SFP1_SCL_VT 5[4C]
IO_L22P_T3U_N6_DBC_AD0P_D04_65	AD26	SFP1_RX_LOS_VT	SFP1_RX_LOS_VT 5[4C]
IO_L23N_T3U_N9_I2C_SDA_65	AE23	SFP2_TX_DISABLE_VT	SFP2_TX_DISABLE_VT 5[4D]
IO_L23P_T3U_N8_I2C_SCLK_65	AD23	SFP2_SDA_VT	SFP2_SDA_VT 5[4D]
IO_T3U_N12_PERSTN0_65	AC22	SFP2_SCL_VT	SFP2_SCL_VT 5[4D]
IO_L24N_T3U_N11_DOUT_CSO_B_65	AD25	SFP2_RX_LOS_VT	SFP2_RX_LOS_VT 5[4D]
IO_L24P_T3U_N10_EMCCLK_65	AD24		

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U1H — BANK 224

MGTHTXP0_224	AF6	DP4_C2M_P	DP4_C2M_P 7[2B]
MGTHTXN0_224	AF5	DP4_C2M_N	DP4_C2M_N 7[2B]
MGTHRXP0_224	AF2	DP4_M2C_P	DP4_M2C_P 7[2A]
MGTHRXN0_224	AF1	DP4_M2C_N	DP4_M2C_N 7[2A]
MGTHTXP1_224	AD6	DP5_C2M_P	DP5_C2M_P 7[2B]
MGTHTXN1_224	AD5	DP5_C2M_N	DP5_C2M_N 7[2B]
MGTHRXP1_224	AE4	DP5_M2C_P	DP5_M2C_P 7[2A]
MGTHRXN1_224	AE3	DP5_M2C_N	DP5_M2C_N 7[2A]
MGTHTXP2_224	AC4	DP6_C2M_P	DP6_C2M_P 7[3B]
MGTHTXN2_224	AC3	DP6_C2M_N	DP6_C2M_N 7[3B]
MGTHRXP2_224	AD2	DP6_M2C_P	DP6_M2C_P 7[3A]
MGTHRXN2_224	AD1	DP6_M2C_N	DP6_M2C_N 7[3A]
MGTHTXP3_224	AB6	DP7_C2M_P	DP7_C2M_P 7[3B]
MGTHTXN3_224	AB5	DP7_C2M_N	DP7_C2M_N 7[3B]
MGTHRXP3_224	AB2	DP7_M2C_P	DP7_M2C_P 7[3A]
MGTHRXN3_224	AB1	DP7_M2C_N	DP7_M2C_N 7[3A]
MGTREFCLK0P_224	Y6	GCLK1_M2C_C_P	
MGTREFCLK0N_224	Y5	GCLK1_M2C_C_N	
MGTREFCLK1P_224	V6		
MGTREFCLK1N_224	V5		

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U1I — BANK 225

MGTHTXP0_225	AA4	DP0_C2M_P	DP0_C2M_P 7[4A]
MGTHTXN0_225	AA3	DP0_C2M_N	DP0_C2M_N 7[4A]
MGTHRXP0_225	Y2	DP0_M2C_P	DP0_M2C_P 7[4A]
MGTHRXN0_225	Y1	DP0_M2C_N	DP0_M2C_N 7[4A]
MGTHTXP1_225	W4	DP1_C2M_P	DP1_C2M_P 7[2B]
MGTHTXN1_225	W3	DP1_C2M_N	DP1_C2M_N 7[2B]
MGTHRXP1_225	V2	DP1_M2C_P	DP1_M2C_P 7[2A]
MGTHRXN1_225	V1	DP1_M2C_N	DP1_M2C_N 7[2A]
MGTHTXP2_225	U4	DP2_C2M_P	DP2_C2M_P 7[2B]
MGTHTXN2_225	U3	DP2_C2M_N	DP2_C2M_N 7[2B]
MGTHRXP2_225	T2	DP2_M2C_P	DP2_M2C_P 7[2A]
MGTHRXN2_225	T1	DP2_M2C_N	DP2_M2C_N 7[2A]
MGTHTXP3_225	R4	DP3_C2M_P	DP3_C2M_P 7[2B]
MGTHTXN3_225	R3	DP3_C2M_N	DP3_C2M_N 7[2B]
MGTHRXP3_225	P2	DP3_M2C_P	DP3_M2C_P 7[2A]
MGTHRXN3_225	P1	DP3_M2C_N	DP3_M2C_N 7[2A]
MGTREFCLK0P_225	T6	GCLK0_M2C_C_P	
MGTREFCLK0N_225	T5	GCLK0_M2C_C_N	
MGTREFCLK1P_225	P6	LVDS_CLK1_C_P	
MGTREFCLK1N_225	P5	LVDS_CLK1_C_N	
MGTAVTTRCAL_R	AF8	MGT_AVTT	
MGTRREF_R	AF7	R195 100	

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GCLK1_M2C_C_P — C95 0.1uF — GCLK1_M2C_P 7[3A]
GCLK1_M2C_C_N — C97 0.1uF — GCLK1_M2C_N 7[3A]
GCLK0_M2C_C_P — C94 0.1uF — GCLK0_M2C_P 7[5A]
GCLK0_M2C_C_N — C96 0.1uF — GCLK0_M2C_N 7[5A]
LVDS_CLK1_C_P — C98 0.1uF — LVDS_CLK1_P 5[3C]
LVDS_CLK1_C_N — C99 0.1uF — LVDS_CLK1_N 5[3C]

LVDS Touch Panel Interface

User Note:
VADJ must be set to 2.5V when the LVDS Touch Panel is used

C290 0.1uF — 3.3V
C291 0.1uF — VADJ
R187 4.75K — R188 4.75K — R189 4.75K
R191 4.75K — VADJ
R192 0 — 3.3V

U20 — TXS0104EPWR

TP_SCL_VT	2	A1	B1 — 13 — TP_SCL
TP_SDA_VT	3	A2	B2 — 12 — TP_SDA
TP_IRQ_N_VT	4	A3	B3 — 11 — CLK_P
	5	A4	B4 — 10 — CLK_N
	8	OE	
	1	VCCA	VCCB — 14
	6	NC	
	9	NC	
	7	GND	

P3 — INDUSTRIAL

TP_D0_P	1
TP_D0_N	2
TP_D1_P	3
TP_D1_N	4
TP_D2_P	5
TP_D2_N	6
TP_D3_P	7
TP_D3_N	8
TP_SCL	9
TP_SDA	10
CLK_P	11
CLK_N	12
TP_IRQ_N	13
	14
	15
	16
SH	17
SH	18
SH	19
SH	20
SH	21
SH	22
SH	23
SH	24

U21 — TXS0104EPWR

C295 0.1uF — 3.3V
C293 0.1uF — VADJ
R194 4.75K — VADJ

7[5B] TRST_L	13	B1	A1 — 2 — TRST_L_VT
7[4B] FMC_SDA	12	B2	A2 — 3 — FMC_SDA_VT
7[4B] FMC_SCL	11	B3	A3 — 4 — FMC_SCL_VT
7[4B] PRSNT_M2C_L	10	B4	A4 — 5 — PRSNT_M2C_L_VT
	8	OE	
	14	VCCB	VCCA — 1
	6	NC	
	9	NC	
	7	GND	

U35 — TXS0104EPWR

C294 0.1uF — VADJ
C292 0.1uF — 3.3V
R190 2.00K — R193 2.00K — R333 2.00K
R272 4.75K — VADJ

PWR_SCL_IO	2	A1	B1 — 13 — PWRSCL — PWRSCL 12[6B]
PWR_SDA_IO	3	A2	B2 — 12 — PWRSDA — PWRSDA 12[6B]
PWR_TMON_IO	4	A3	B3 — 11 — PWRTMON — PWRTMON 12[6B]
	5	A4	B4 — 10
	8	OE	
	1	VCCA	VCCB — 14
	6	NC	
	9	NC	
	7	GND	

Layout Note:
DisplayPort routing should adhere to the following guidelines:
1. Diff pair lengths matched to within 10 mils
2. Vias should be avoided on all diff pairs
3. All trace angles should be > 135°
4. All pairs should use symetric routing within the pair
5. Do not route traces of plane splits or anti-pads
6. Target impedence is 100 ohm differential

AVNET — Avnet Engineering Services

Sheet Title: Bank 64, Bank 65, LVDS Touch Panel			
Size: B	Document Name: Kintex UltraScale Development Board	Variant Description: KU040-DB-PRJ-B-01-00	Rev: B
Date: 10/2/2015	Doc Num: KU040-DB-SCH-B	Sheet: 8 of 14	

Layout Note:

Place termination resistors close to the KU40.

Layout Note:

HDMI signal routing should adhere to the following guidelines:

1. Differential Target impedence is 100 ohm
2. Single Ended Target Impedence is 50 ohm
2. Length match traces within a pair to 10 mils
3. Length match pair to pair within 20 mils
4. Routing without vias is preferred
5. Route signals within a pair symmetrically
6. Do not route over plane splits or anti-pads
7. Stub length shall not exceed 1000 mils

U22 ADV7511KSTZ

HDMI_MVDD HDMI_PLVDD HDMI_AVDD HDMI_DVDD

R196 27.4K 3.3V

D18 BAS521,115

D19 PESD0402-140

HDMI_D23 R199 0
HDMI_D22 R200 0
HDMI_D21 R201 0
HDMI_D20 R202 0
HDMI_D19 R203 0
HDMI_D18 R205 0
HDMI_D17 R207 0
HDMI_D16 R209 0
HDMI_D15 R211 0
HDMI_D14 R213 0
HDMI_D13 R214 0
HDMI_D12 R215 0
HDMI_D11 R217 0
HDMI_D10 R218 0
HDMI_D9 R219 0
HDMI_D8 R220 0

HDMI_DE HDMI_CLK HDMI_VSYNC HDMI_HSYNC

TX2+ HDMI_TX2_P
TX2- HDMI_TX2_N
TX1+ HDMI_TX1_P
TX1- HDMI_TX1_N
TX0+ HDMI_TX0_P
TX0- HDMI_TX0_N
TXC+ HDMI_TXC_P
TXC- HDMI_TXC_N

CEC HDMI_CEC_CLK R204 49.9
DDCSCL R206 2.00K HDMI_5V
DDCSDA R208 2.00K HDMI_5V
HEAC+ C100 1uF R210 49.9 HDMI_DVDD
HEAC- R212 49.9 C101 1uF
HPD

SPDIF HDMI_SPDIF
SPDIF_OUT HDMI_SPDIFOUT
MCLK
I2S0 I2S1 I2S2 I2S3
SCLK
LRCLK

I2C Address 0111001 R/W

SDA HDMI_SDA
SCL HDMI_SCL
INT HDMI_INT
R_EXT R223 887
PD

R216 10.00K
3.3V D23 R221 240
Q11 2N7002

R222 2.00K 1.8V

J17 HDMI

D2+ D2S D2- D1+ D1S D1- D0+ D0S D0- CLK+ CLKS CLK- CEC RES SCL SDA DDC/CECG 5V0 HPD
S1 S3 S2 S4

PWR HDMI_5V

D20 D21 D22

L6 220 Ohm @ 100MHz
C102 0.1uF
SH_GND5

1.8V R197 1.00K R198 1.00K GND

U1D

BANK 46

J18		
HDMI_D23	A25	IO_L1N_T0L_N1_DBC_46
HDMI_D22	A24	IO_L1P_T0L_N0_DBC_46
HDMI_D21	E23	IO_T0U_N12_VRP_46
HDMI_D20	D26	IO_L2N_T0L_N3_46
HDMI_D19	D25	IO_L2P_T0L_N2_46
HDMI_D18	B25	IO_L3N_T0L_N5_AD15N_46
HDMI_D17	B24	IO_L3P_T0L_N4_AD15P_46
HDMI_D16	C23	IO_L4N_T0U_N7_DBC_AD7N_46
HDMI_D15	D23	IO_L4P_T0U_N6_DBC_AD7P_46
HDMI_D14	C24	IO_L5N_T0U_N9_AD14N_46
HDMI_D13	D24	IO_L5P_T0U_N8_AD14P_46
HDMI_D12	B26	IO_L6N_T0U_N11_AD6N_46
HDMI_D11	C26	IO_L6P_T0U_N10_AD6P_46
HDMI_D10	A23	IO_L7N_T1L_N1_QBC_AD13N_46
HDMI_D9	A22	IO_L7P_T1L_N0_QBC_AD13P_46
HDMI_D8	A20	IO_L8N_T1L_N3_AD5N_46
HDMI_SPDIF	B20	IO_L8P_T1L_N2_AD5P_46
HDMI_DE	B22	IO_L9N_T1L_N5_AD12N_46
HDMI_CLK	B21	IO_L9P_T1L_N4_AD12P_46
HDMI_VSYNC	C22	IO_L10N_T1U_N7_QBC_AD4N_46
HDMI_HSYNC	C21	IO_L10P_T1U_N6_QBC_AD4P_46
HDMI_INT	E21	IO_L11N_T1U_N9_GC_46
HDMI_SPDIFOUT_VT	E20	IO_L11P_T1U_N8_GC_46
HDMI_SDA_VT	E22	IO_T1U_N12_46
HDMI_SCL_VT	D21	IO_L12N_T1U_N11_GC_46
	D20	IO_L12P_T1U_N10_GC_46
4[4D] USB_UART_TXD	C19	IO_L13N_T2L_N1_GC_QBC_46
4[4D] USB_UART_RXD	D19	IO_L13P_T2L_N0_GC_QBC_46
6[3B] QSPI_2_CS	D16	IO_T2U_N12_46
10[1A] LED0	C18	IO_L14N_T2L_N3_GC_46
6[1D] PMOD4_7_VT	D18	IO_L14P_T2L_N2_GC_46
6[1D] PMOD4_6_VT	A18	IO_L15N_T2L_N5_AD11N_46
6[1D] PMOD4_5_VT	A17	IO_L15P_T2L_N4_AD11P_46
6[1D] PMOD4_4_VT	A19	IO_L16N_T2U_N7_QBC_AD3N_46
6[1D] PMOD4_3_VT	B19	IO_L16P_T2U_N6_QBC_AD3P_46
6[1D] PMOD4_2_VT	B16	IO_L17N_T2U_N9_AD10N_46
6[1D] PMOD4_1_VT	C16	IO_L17P_T2U_N8_AD10P_46
6[1D] PMOD4_0_VT	B17	IO_L18N_T2U_N11_AD2N_46
6[3D] PMOD3_7_VT	C17	IO_L18P_T2U_N10_AD2P_46
6[3D] PMOD3_6_VT	F20	IO_L19N_T3L_N1_DBC_AD9N_46
6[3D] PMOD3_5_VT	G19	IO_L19P_T3L_N0_DBC_AD9P_46
6[3D] PMOD3_4_VT	F17	IO_L20N_T3L_N3_AD1N_46
6[3D] PMOD3_3_VT	G17	IO_L20P_T3L_N2_AD1P_46
6[3D] PMOD3_2_VT	F19	IO_L21N_T3L_N5_AD8N_46
6[3D] PMOD3_1_VT	F18	IO_L21P_T3L_N4_AD8P_46
6[3D] PMOD3_0_VT	G16	IO_L22N_T3U_N7_DBC_AD0N_46
10[1B] LED1	H16	IO_L22P_T3U_N6_DBC_AD0P_46
10[1B] LED2	E18	IO_L23N_T3U_N9_46
10[1B] LED3	E17	IO_L23P_T3U_N8_46
10[1C] LED4	E16	IO_T3U_N12_46
10[1C] LED5	H18	IO_L24N_T3U_N11_46
10[1C] LED6	H17	IO_L24P_T3U_N10_46
10[1C] LED7		

XCKU040-1FBVA676

3.3V C297 0.1uF 1.8V
U25 TXS0104EPWR
VCCA VCCB A1 A2 A3 A4 B1 B2 B3 B4 OE NC NC GND
HDMI_SPDIFOUT_VT HDMI_SDA_VT HDMI_SCL_VT
HDMI_SPDIFOUT HDMI_SDA HDMI_SCL
R226 4.75K 1.8V
3.3V C296 0.1uF
R224 4.75K R225 4.75K 3.3V

12V C105 1uF
U24 LP2981AIM5-5.0/NOPB
VIN VOUT EN NC GND
HDMI_5V C104 10uF

3.3V C103 0.1uF
U23 DSC1001AI2-012.0000T
VCC INH OUT GND PAD
HDMI_CEC_CLK

HDMI_MVDD L7 1.8V 220 Ohm @ 100MHz PWR HDMI_DVDD
C106 10uF C107 0.1uF C108 0.1uF C109 0.1uF C110 0.1uF C111 0.1uF

L8 3.3V 220 Ohm @ 100MHz PWR
C112 10uF C113 0.1uF

HDMI_AVDD L9 1.8V 220 Ohm @ 100MHz PWR
C114 10uF C115 0.1uF C116 0.1uF C117 0.1uF C118 0.1uF C119 0.1uF

HDMI_PLVDD L10 1.8V 220 Ohm @ 100MHz PWR
C120 10uF C121 0.1uF C122 0.1uF

Sheet Title:	HDMI
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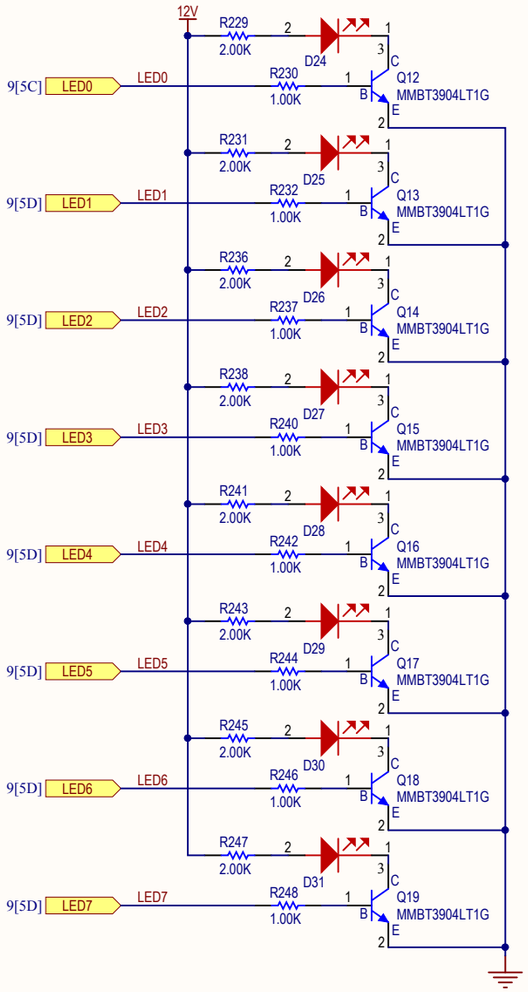
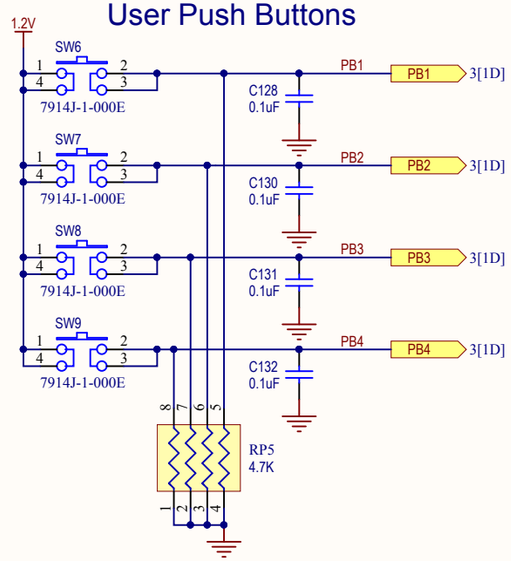
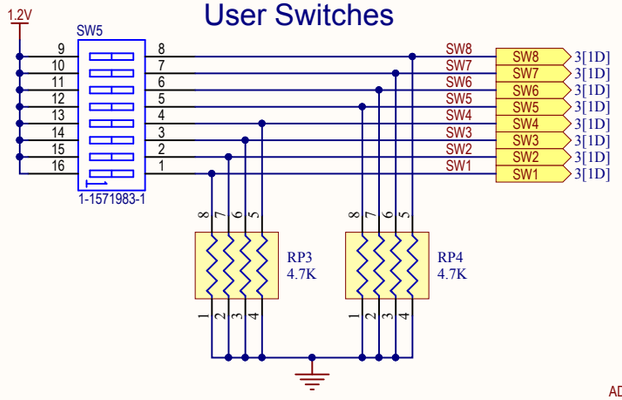
User LEDs

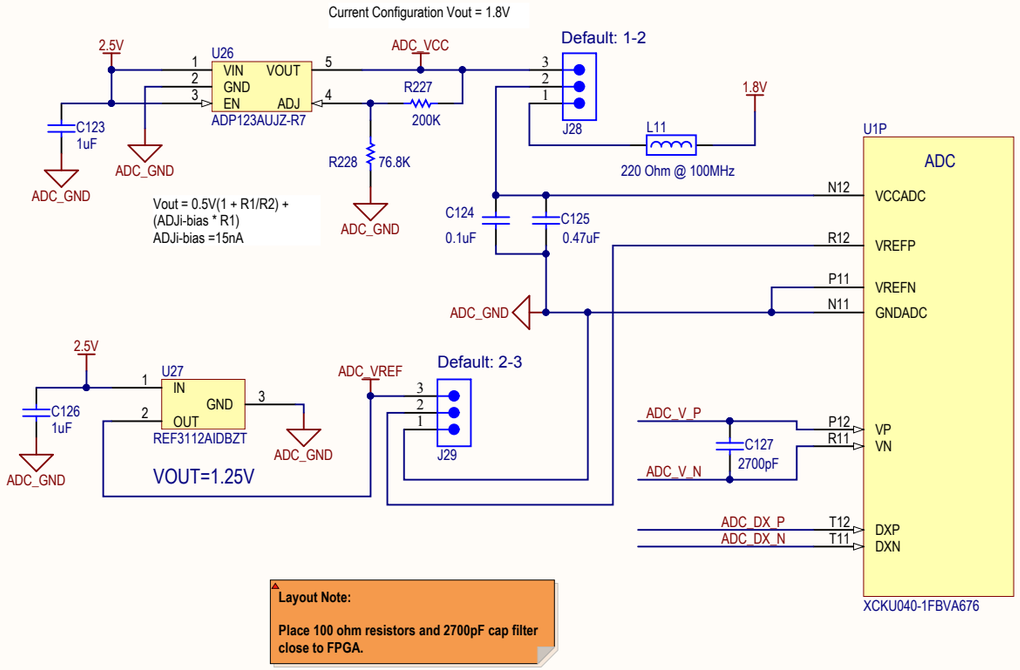


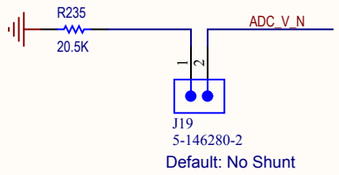
User Push Buttons

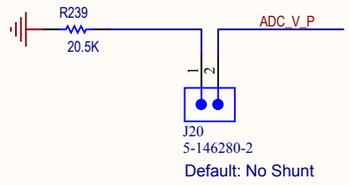


User Switches

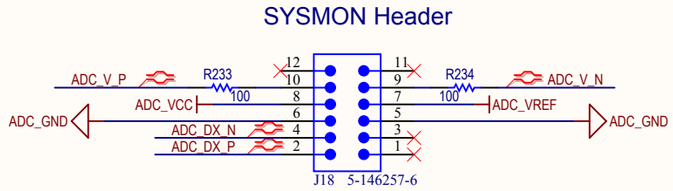


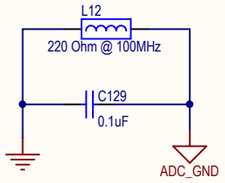






SYSMON Header





Sheet Title:	SYSMON, LEDs, Switches, Push Buttons
Size: B	Document Name: Kintex UltraScale Development Board
Variant Description:	KU040-DB-PRJ-B-01-00
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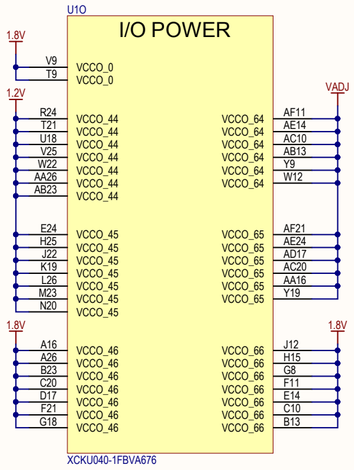
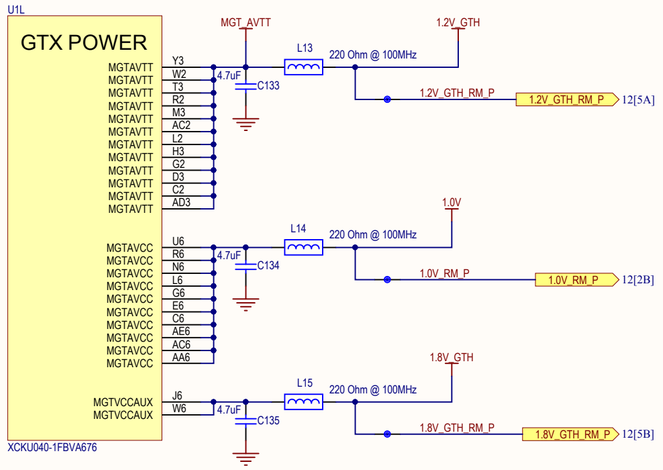
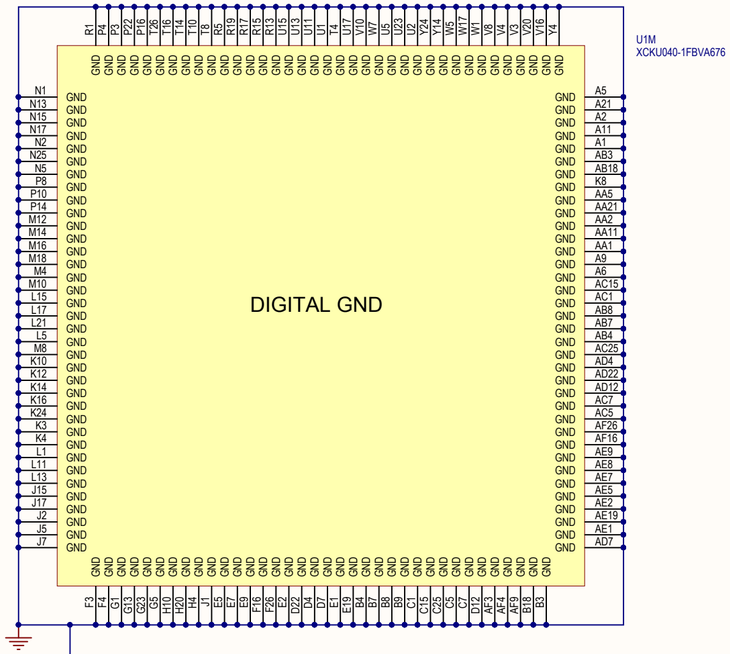
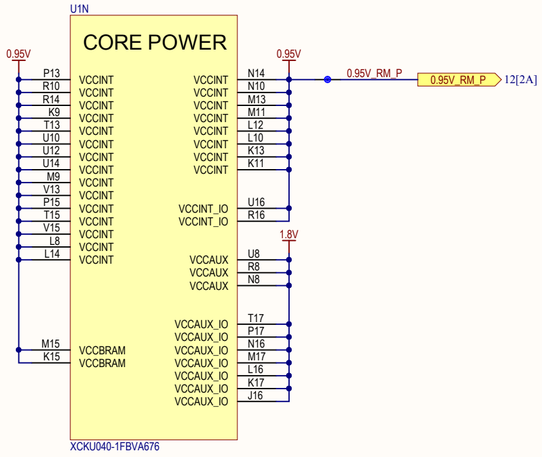
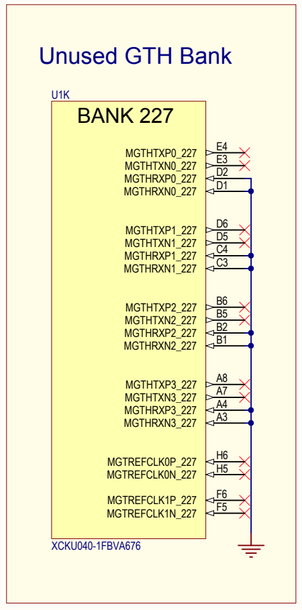










VCCO_64/VCCO_65

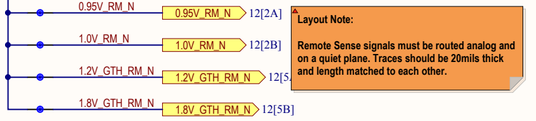


VCCO_46/VCCO_66

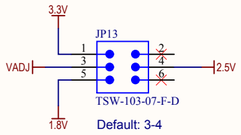


VCCO_0/VCCO_44/VCCO_45



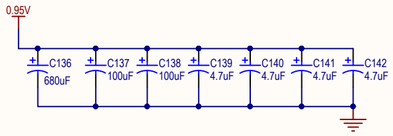


VADJ SEL

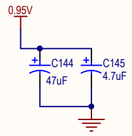




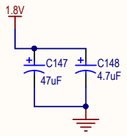
VCCINT/VCCINT_IO



VCCBRAM



VCCAUX/VCCAUXIO



AVNET — Avnet Engineering Services			
Sheet Title: Device Power			
Size: B	Document Name: Kintex UltraScale Development Board	Variant Description: KU040-DB-PRJ-B-01-00	Rev: B
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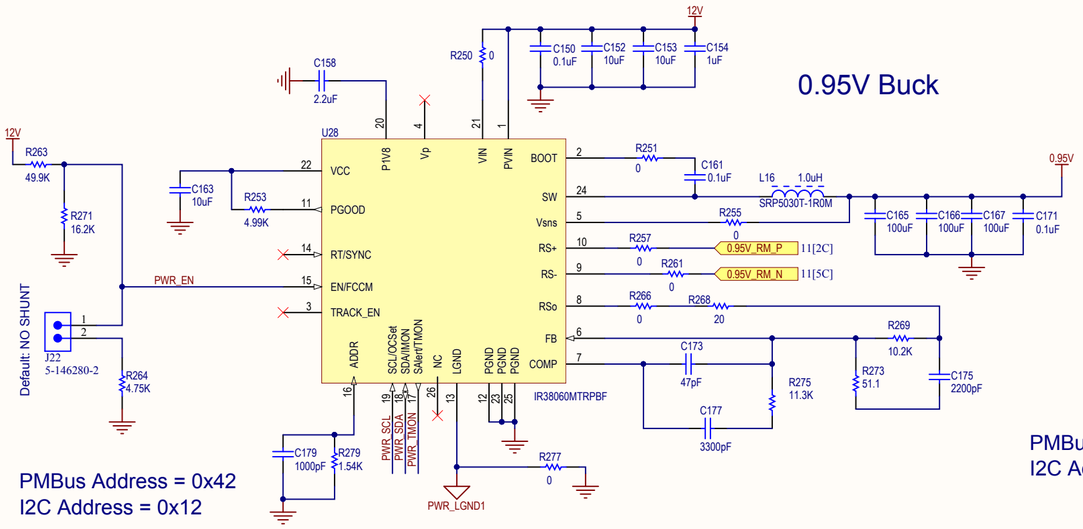
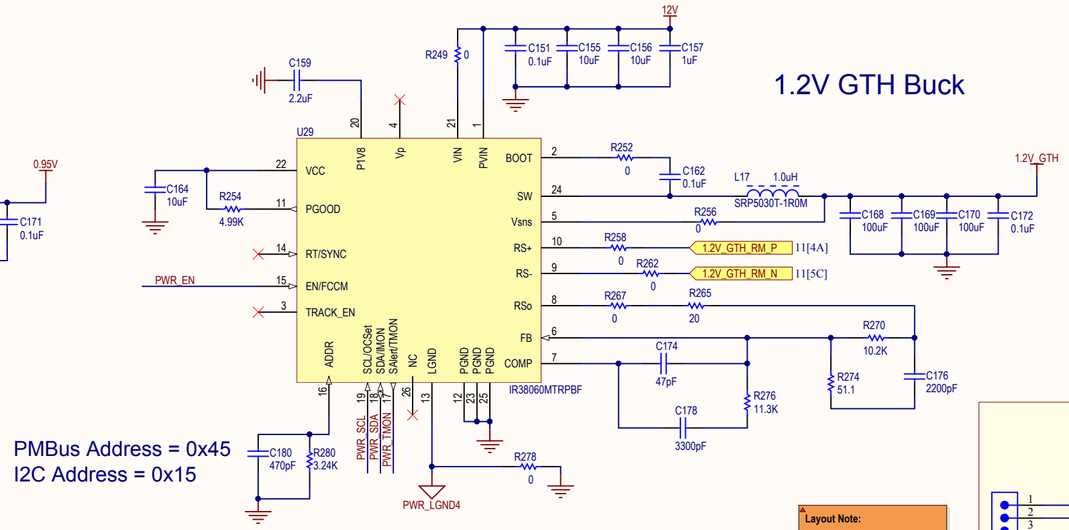
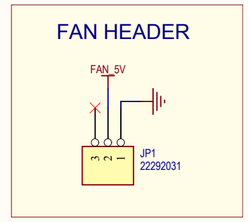
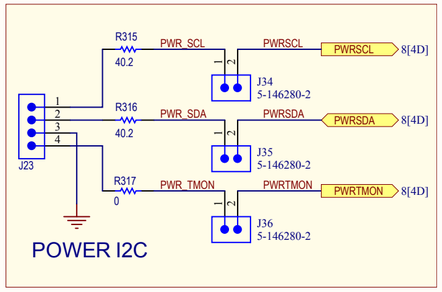






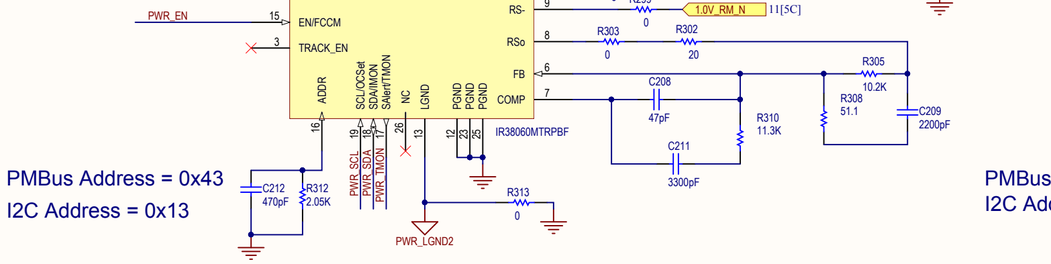


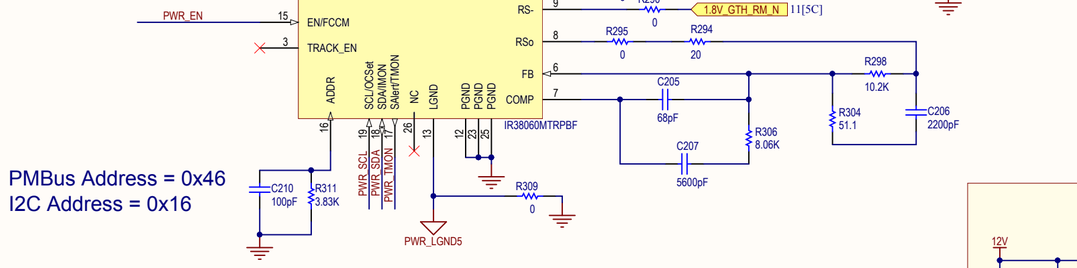
Layout Note:

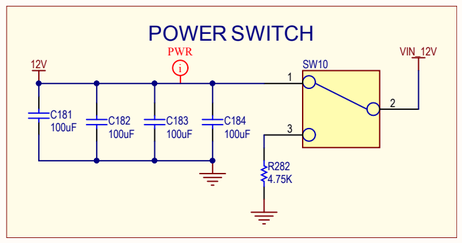
Jumpers J34/J35/J36 should be placed as close as possible to J23.

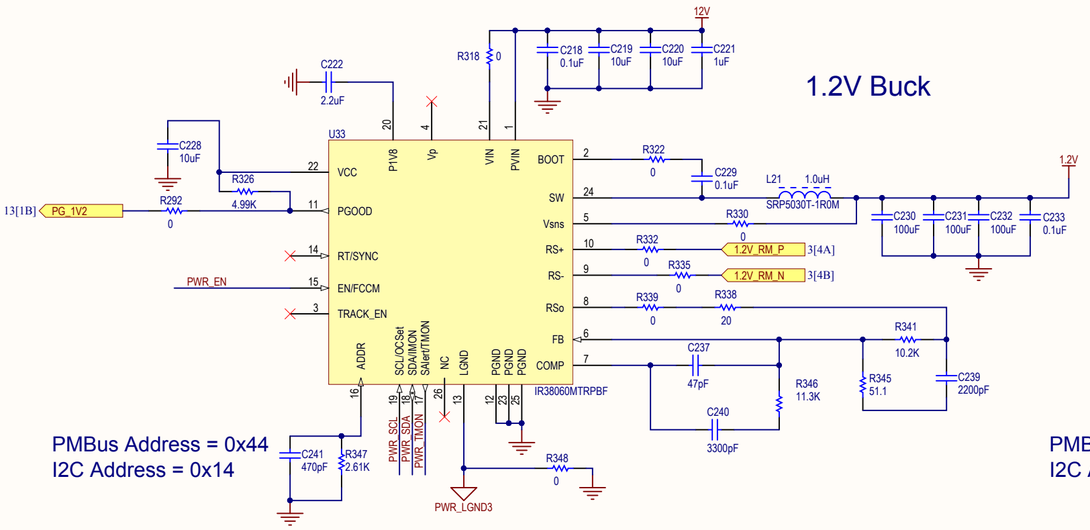
User Note:

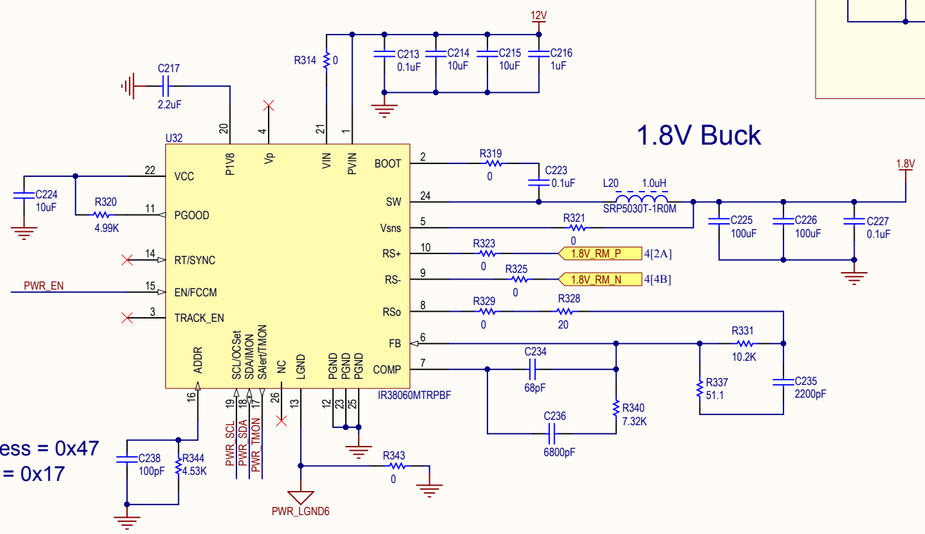
Remove J34-J35-J36 when Programming the IR Devices via the IR Programming Cable

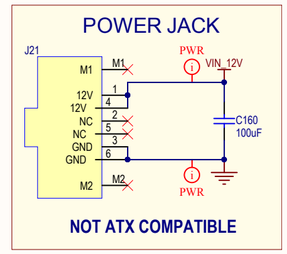












Sheet Title:	IR Main Power Supplies
Size: B	Document Name: Kintex UltraScale Development Board
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2.5V and 3.3V Dual Buck

Layout Note:
Place 3 each near the VIN pins for each rail.

12V
C243 10uF
C244 10uF
C245 10uF
C246 10uF
C247 10uF
C248 10uF

R352 5.36K
R353 95.3
C242 2200pF
R354 5.36K
R355 0
R361 1.33K
PWR_LGND7
C249 390pF
R359 1.33K
C250 15nF
R360 1.33K
PWR_LGND7

3.3V
R362 49.9K

U34
Vsns1 (1)
FB1 (31)
COMP1 (30)
29 PGOOD1
2 EN1
7 RT/SYNC
5 GND
3 VIN
4 VCC/LDO_OUT
6 SEQ
8 EN2
12 PGOOD2
26 PVIN1
27 PVIN1
23 PGND1
24 PGND1
25 PGND1
28 BOOT1
21 SW1
22 SW1
19 SW2
20 SW2
13 BOOT2
14 PVIN2
15 PVIN2
16 PGND2
17 PGND2
18 PGND2
Vsns2 (9)
FB2 (10)
COMP2 (11)
IR3892MTRPBF

12V
C251 0.1uF
C253 0.1uF
L22 1.0uH SRP5030T-1R0M
2.5V
C254 22uF
C255 22uF
L23 1.0uH SRP5030T-1R0M
3.3V
C259 22uF
C260 22uF
C258 0.1uF
C262 0.1uF

12[1D] PG_1V2
C252 10000pF
R366 39.2K
PWR_LGND7
12V
C256 1uF
C257 2.2uF
C261 10000pF
PWR_LGND7
3.3V
R370 49.9K

R375 0
PWR_LGND7
R376 953
PWR_LGND7
C263 0.022uF
C264 470pF
R377 1.24K
R378 95.3
C265 2200pF
R379 5.36K
R380 0
R381 953
PWR_LGND7
R382 5.36K

R300 0
12V
FZT849TA Q9
FAN_5V
R342 1.33K
C276 0.1uF
R301 10.00K
C277 4.7uF
TL431AIDBZR U36
R307 10.00K

Power Rail LEDs

12V
R349 10.00K
D32
0.95V
R356 1.00K
CQ20 MMBT3904LT1G
0.95V

12V
R350 10.00K
D33
1.0V
R357 1.00K
CQ21 MMBT3904LT1G
1.0V

12V
R351 10.00K
D34
1.2V
R358 1.00K
CQ22 MMBT3904LT1G
1.2V

12V
R363 10.00K
D35
1.2V_GTH
R367 1.00K
CQ23 MMBT3904LT1G
1.2V_GTH

12V
R364 10.00K
D36
1.8V_GTH
R368 1.00K
CQ24 MMBT3904LT1G
1.8V_GTH

12V
R365 10.00K
D37
1.8V
R369 1.00K
CQ25 MMBT3904LT1G
1.8V

12V
R371 10.00K
D38
2.5V
R373 1.00K
CQ26 MMBT3904LT1G
2.5V

12V
R372 10.00K
D39
3.3V
R374 1.00K
CQ27 MMBT3904LT1G
3.3V

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Sheet Title: IR Dual Power Supply			
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Revision Notes:

KU040 DB Revision: B
Initial Product Release

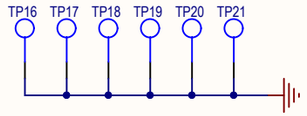
Mechanicals:

PCB1

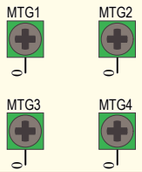


PCB
KU040-DB-PCB-B

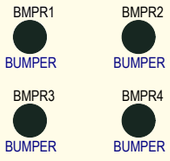
GND TEST POINTS



Mounting Holes



Bumper Standoffs



Assembly:

Label1
BD-XXXX-XXXXX-G
Label, Product

Label_ESD1



Label, ESD

Label2

XXXXXXX
Label, Serial Number

ESD1



ESD Bag

SH1



SH2



SH3



SH4



SH6



SH7



SH8



SH9



SH10



SH11



SH12



SH13



SH14



SH15



SH16



SH17



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Sheet Title: **Back Page**			
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