40 W adapter board powered by 950 V CoolMOS™ P7 SJ MOSFET

Quasi-resonant snubberless flyback converter solution for high efficiency adapter designs

EVAL_40W_FLY_P7_950V

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GD10000720

Table of contents

1 General description

2 Efficiency results

3 PCB layout

4 Evaluation board features

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2 Efficiency results

3 PCB layout

4 Evaluation board features

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General description

Introduction

This 40 W adapter reference board is intended to be a form, fit and function test platform for low cost charger applications to show the state-of-art 950 V CoolMOS™ P7 superjunction (SJ) MOSFET (IPA95R450P7). The board is designed to fit a very small form factor while maintaining high efficiency, low standby power and various modes of protection for a highly reliable system. The 950 V CoolMOS™ P7 has a higher breakdown voltage allowing use in applications which require a high input voltage or gives increased design flexibility to reduce losses in the snubber network.

The board shows how to use the 950 V CoolMOS™ P7 in a snubberless flyback converter with up to 40 W of output power. By eliminating the snubber network the cost of the snubber can be removed while increasing efficiency and eliminating the PCB hotspot caused by the snubber network. This gives additional design flexibility to increase power density or reduce system costs.

Summary of features:

- Input voltage: 90 – 265 V_{AC}
- Output voltage: 19 V_{DC}
- Output current max.: 2.10 A
- Efficiency: ~90.5% (at 230 V_{AC}, 100% load)
- Efficiency: ~88.6% (at 90 V_{AC}, 100% load)



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General description

Schematic

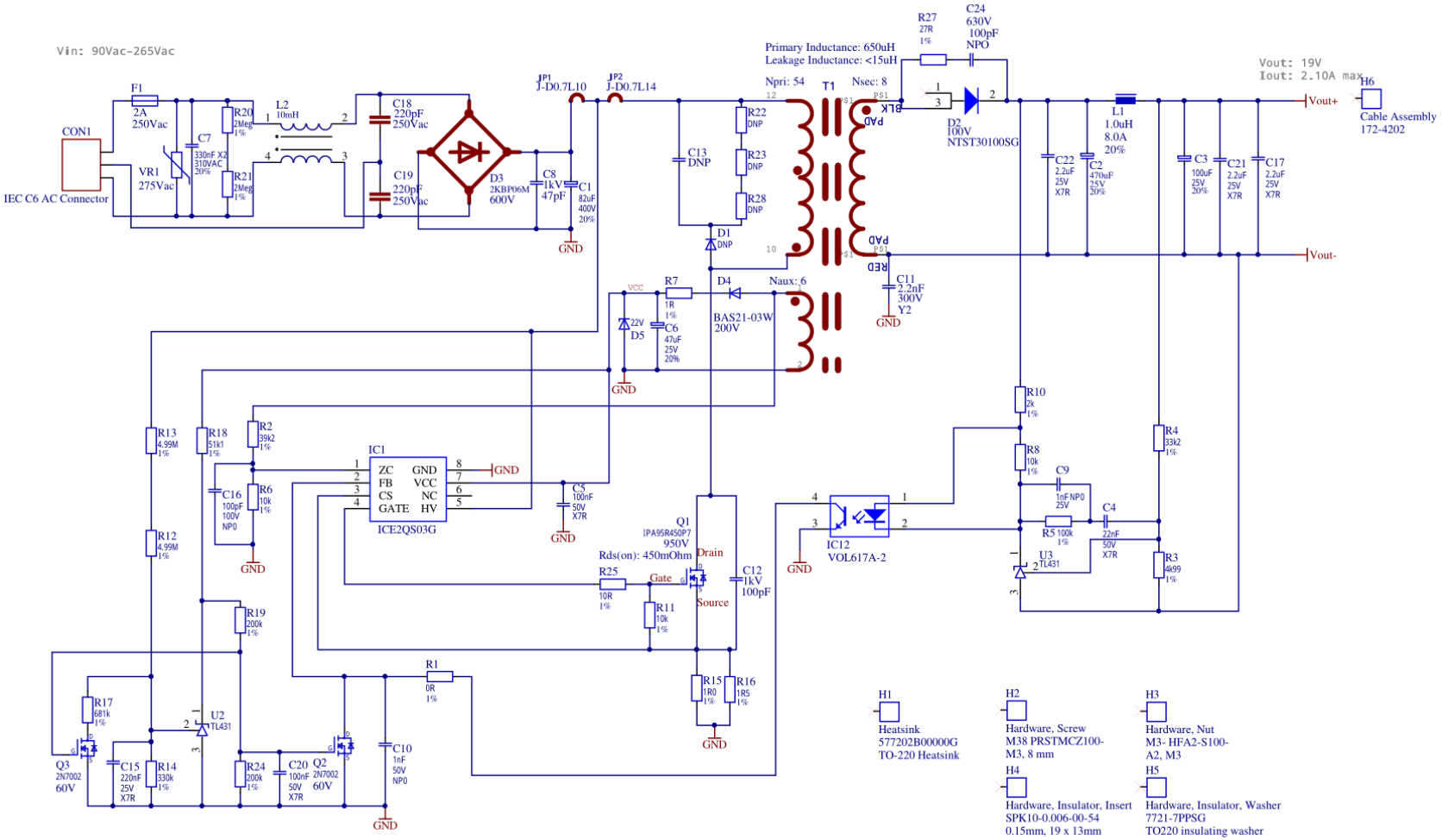

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Table of contents

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2 Efficiency results

3 PCB layout

4 Evaluation board features

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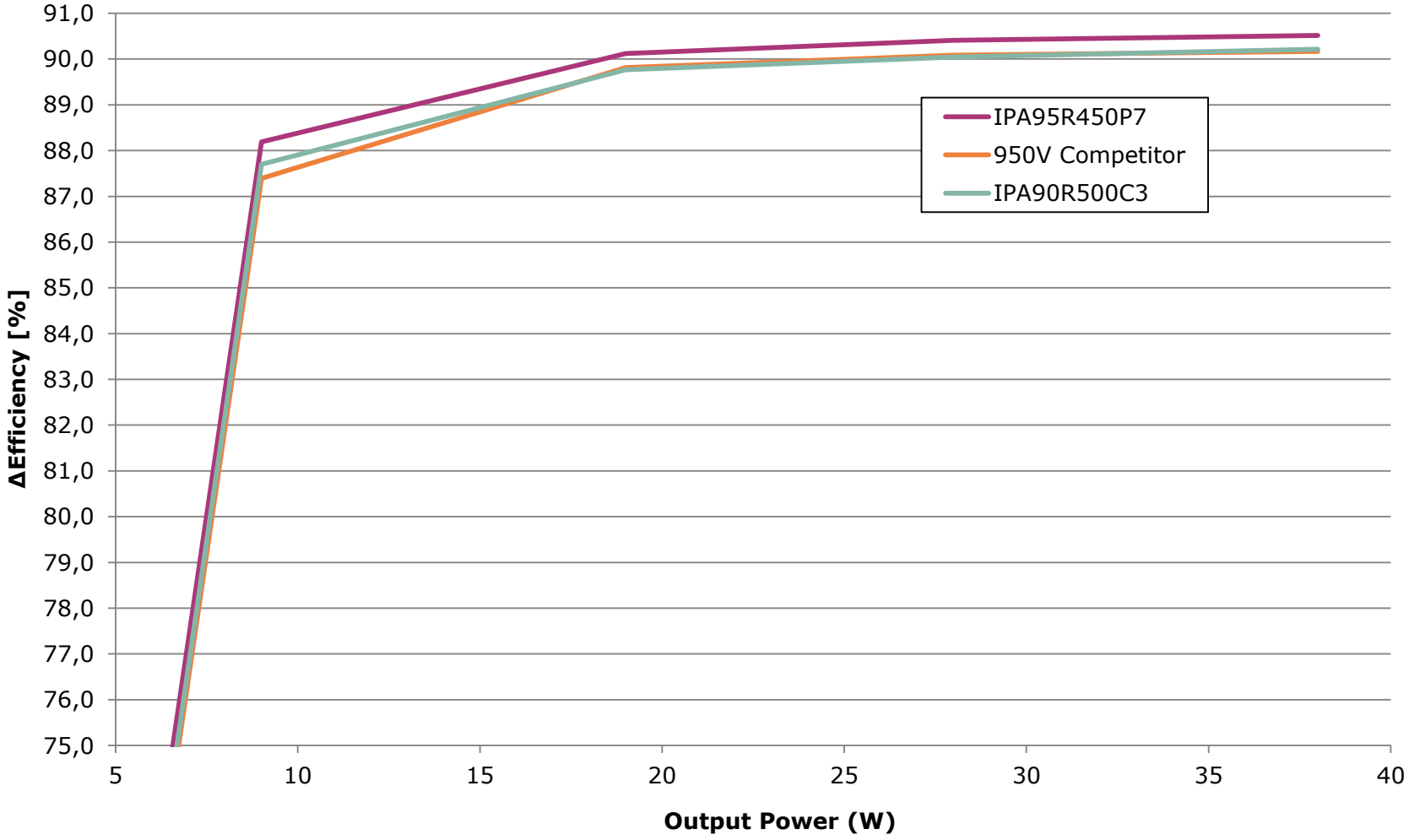
Efficiency results

Absolute efficiency of the 40 W adapter at 230 V_{AC}



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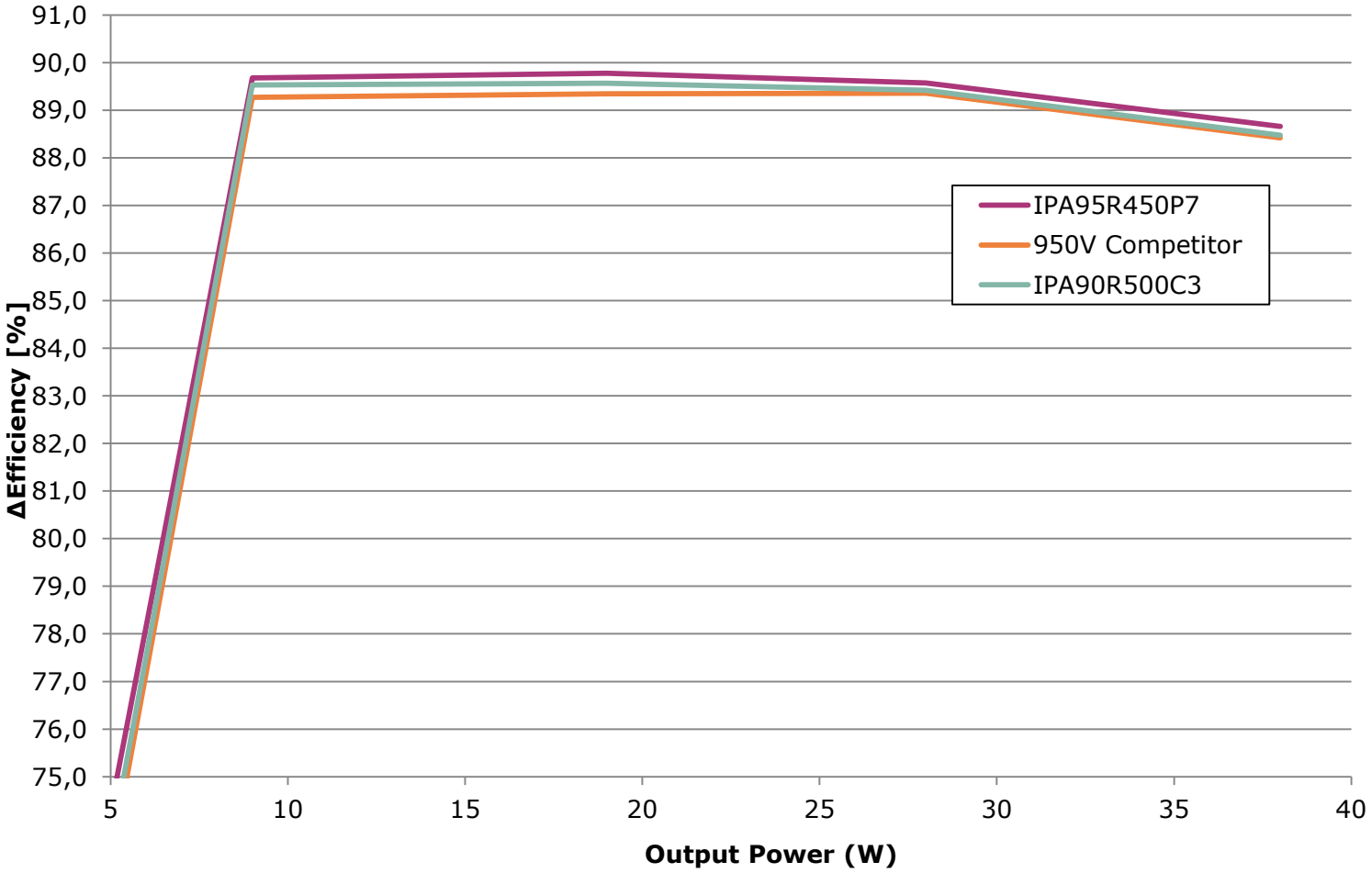
Efficiency results

Absolute efficiency of the 40 W adapter at 90 V_{AC}



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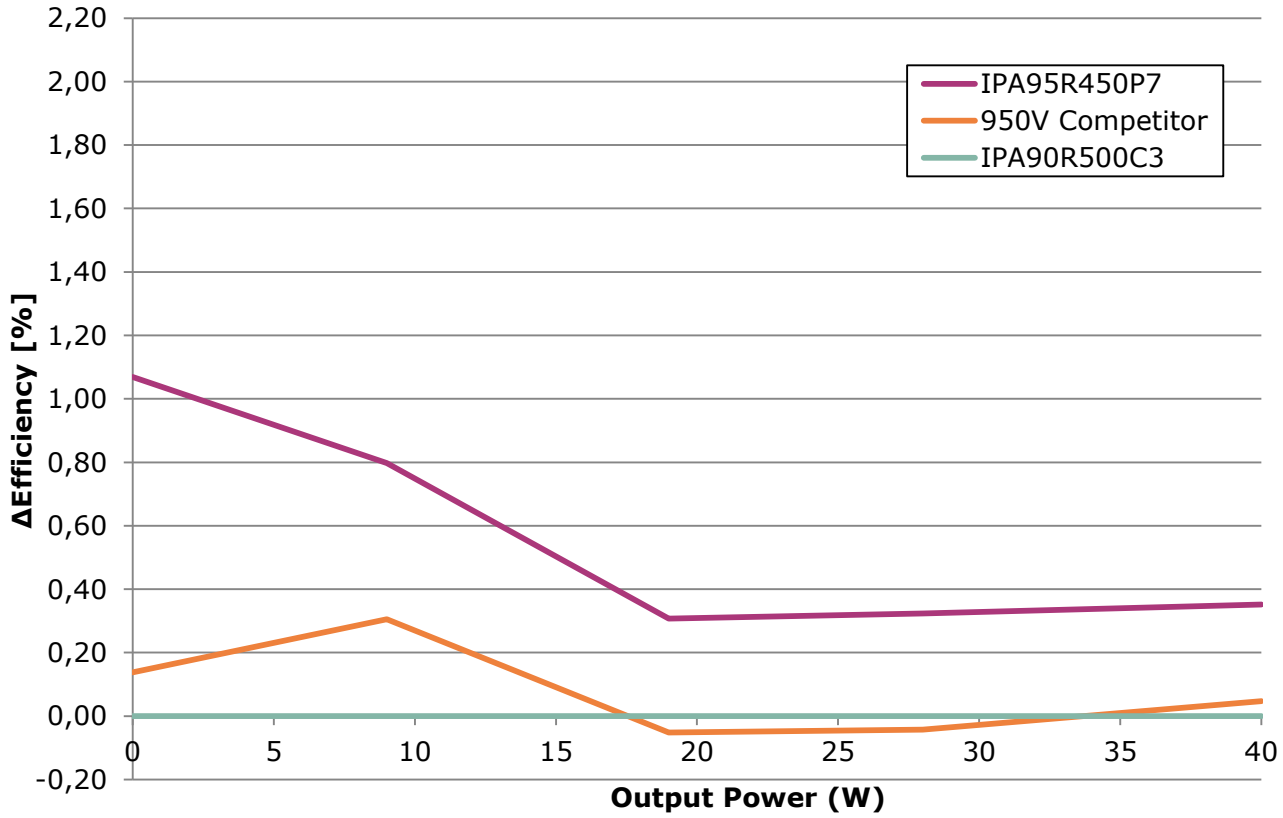
Efficiency results

Efficiency graph of the 40 W adapter at 230 VAC showing the C3 and competitor's devices referenced to the P7 MOSFET.



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Efficiency results

Efficiency of the 40 W adapter at 90 V_{AC} showing the C3 and competitor's devices referenced to the P7 MOSFET.

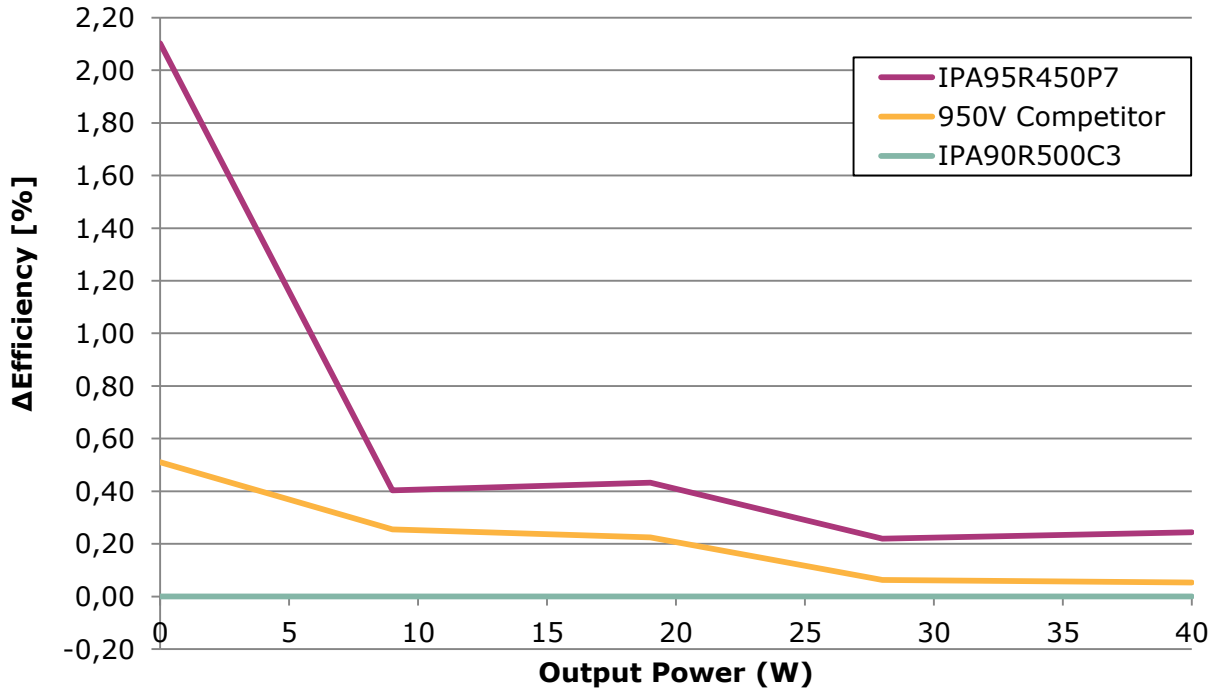

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Table of contents

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4 Evaluation board features

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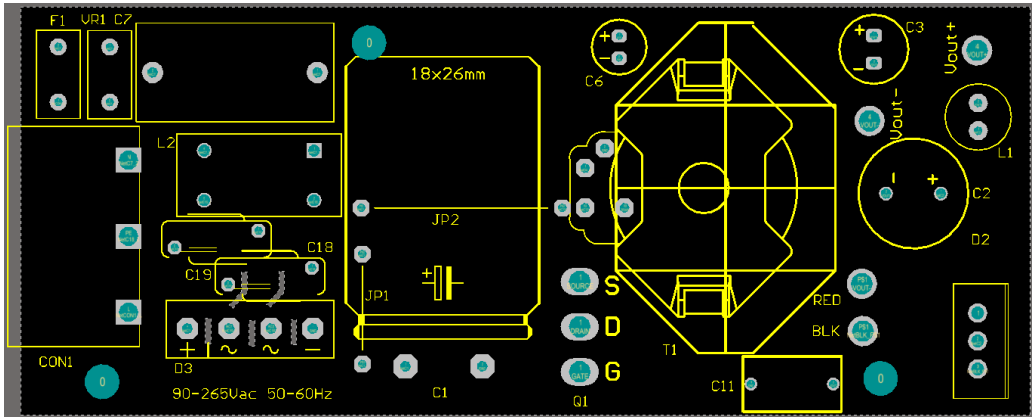
PCB layout

Board layout top



Board layout bottom

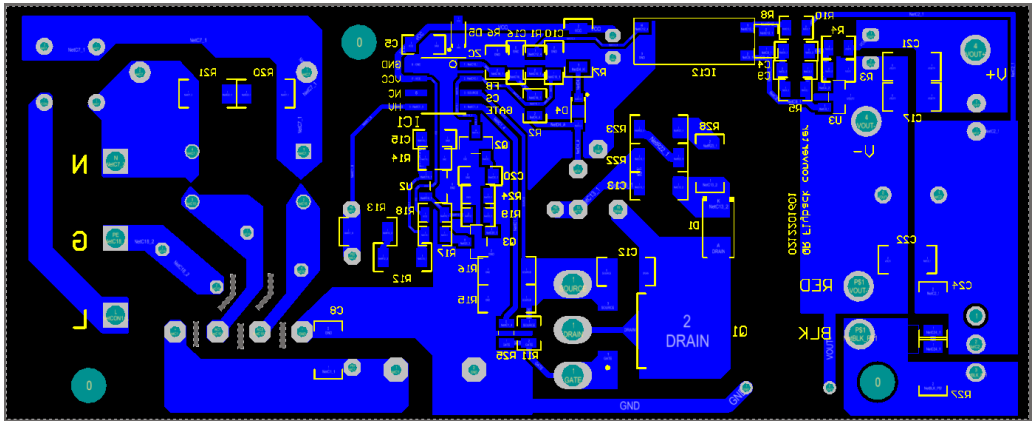


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Table of contents

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3 PCB layout

4 Evaluation board features

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Evaluation board features

- **Fold back point protection** - For a QR flyback converter, the maximum possible output power is increased when a constant current limit value is used across the entire mains input voltage range. This is usually not desired as this will increase the cost of the transformer and output diode in the case of output over power conditions. The internal fold back protection is implemented to adjust the V_{CS} voltage limit according to the bus voltage. Here, the input line voltage is sensed using the current flowing out of the ZC pin, during the MOSFET on-time. As the result, the maximum current limit adjusts with the AC line voltage.

- **V_{CC} over voltage and under voltage protection** - During normal operation, the V_{cc} voltage is continuously monitored. When the V_{cc} voltage increases to VVCC OVP or V_{cc} voltage falls below the under voltage lock out level VVCC off, the IC will enter into auto restart mode.

- **Over load/open loop protection** - In the case of an open control loop, the feedback voltage is pulled up with an internal block. After a fixed blanking time, the IC enters into auto restart mode. In case of a secondary short-circuit or overload, the regulation voltage V_{FB} will also be pulled up, the same protection is applied and the IC will auto restart.

- **Adjustable output overvoltage protection** - During the off-time of the power switch, the voltage at the zero-crossing pin, ZC, is monitored for output overvoltage detection. If the voltage is higher than the preset threshold 3.7 V for a preset period of 100 µs, the IC is latched off.

- **Auto restart for over temperature protection** - The IC has a built-in over temperature protection function. When the controller's temperature reaches 140 °C, the IC will shut down the switch and enters into auto restart. This can protect the power MOSFET from overheating.

- **Short winding protection** - The source current of the MOSFET is sensed via external resistors, R15 and R16. If the voltage at the current sensing pin is higher than the preset threshold VCSSW of 1.68 V during the on-time of the power switch, the IC is latched off. This constitutes a short winding protection. To avoid an accidental latch off, a spike blanking time of 190 ns is integrated in the output of internal comparator.

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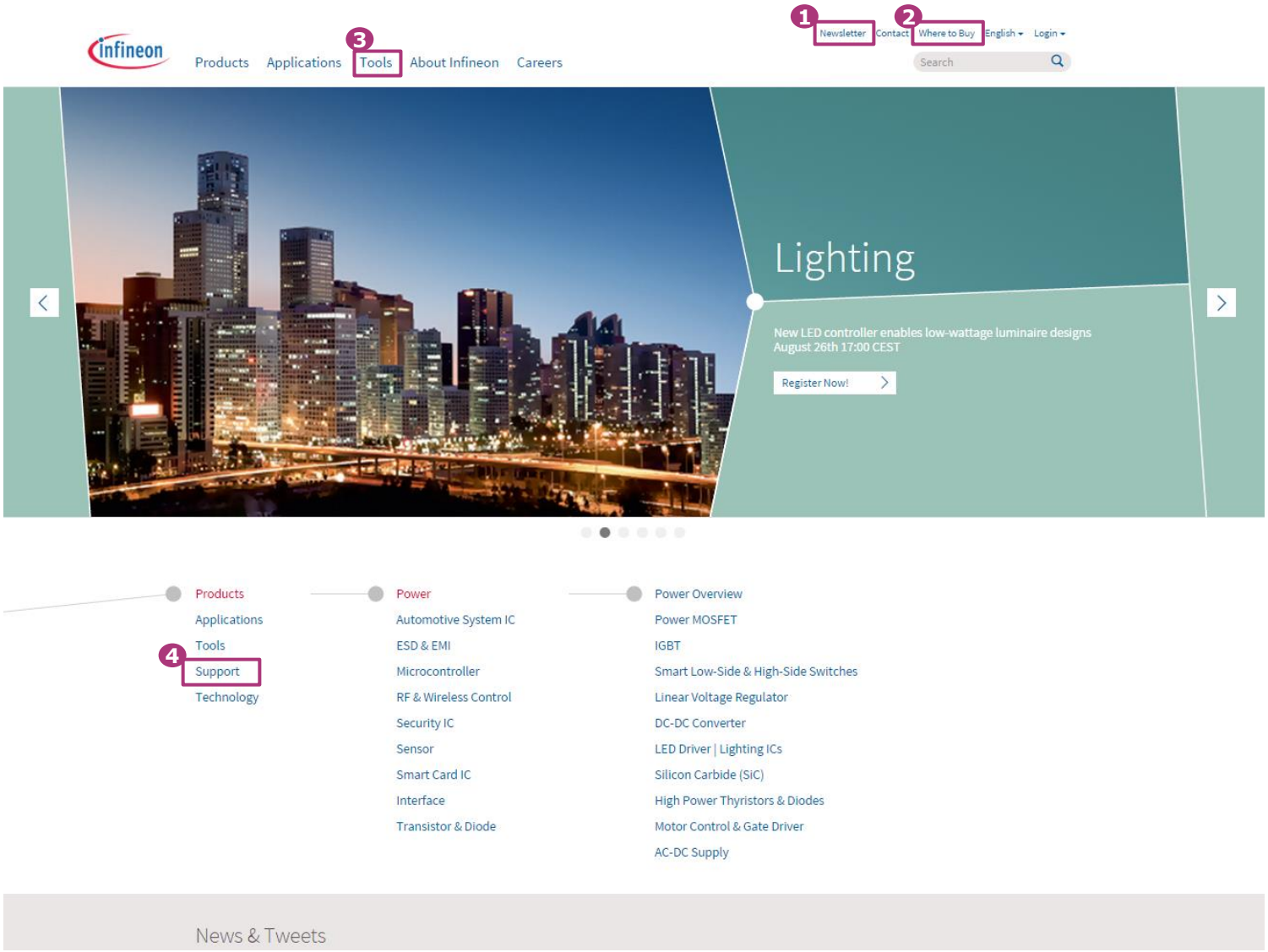

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