MOTIX ™ 6EDL7141

Addendum

About this Document

This addendum is addressed to developers using 6EDL7141. It describes product deviations with respect to the user documentation listed below. It is strongly recommended that the device behavior and proposed workarounds are considered for the application.

Reference Datasheet

Table 1 Current User Documentation

Document	Version	Date
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Affected Products: 6EDL7141

Silicon version: A24

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1 Functional Deviations

1.1 CP_01 - VCCLS pre-charge feature not working

Description: VCCLS pre-charge voltage is not present in some devices under some conditions when VCCLS pre-charge is enabled (described in section 3.4.3 of above-mentioned datasheet).

Workaround: Recommend to disable the charge pump enable feature by setting register bit CP_PRECHARGE_EN = 0.

1.2 WD_01 - EN_DRV watchdog time not programmable

Description: EN_DRV watchdog timer input frequency $t_{WD_EN_DRV_FREQ}$ is fixed at 500 Hz typical (450 Hz min, 550 Hz max). The period after which the missing signal will result in a fault (WD_TIMER_T) is not applied when watchdog input is selected to be EN_DRV. Watchdog period programmed by register bits WD_TIMER_T will have no effect. If EN_DRV signal frequency deviates from target frequencies, fault will happen without waiting for WD_TIMER_T.

Workaround: No. User must consider this in the design.

1.3 WD_02 - EN_DRV watchdog timer reports a fault when EN_DRV toggles

Description: If EN_DRV pin is used as watchdog input by configuring WD_INSEL bitfield, a fault is reported when EN_DRV signal changes from Low to High, or from High to Low even if frequency is within specified range.

Workaround: Ignore the nFAULT pin and register WD_FLT reporting at EN_DRV changes, clear fault by writing FAULTS_CLR register.

Revision history

Page or Reference	Description of change
v1.00	First public version

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