CoolSET™ ICE5xRxxxxBZx-1 design guide for flyback topology in DIP package

About this document

Scope and purpose

This document is a design guide for a Fixed Frequency flyback converter using the latest CoolSET™ 5th Generation Fixed Frequency Plus ICE5xRxxxxBZx-1 switching controller from Infineon, which offers high efficiency, low standby power with selectable entry and exit standby power options, wider V_{CC} operating range with fast startup, and various protection modes for a highly reliable system.

Intended audience

This document is intended for power supply design/application engineers, students, etc. who wish to design power supplies with the latest CoolSET™ 5th Generation Fixed Frequency Plus ICE5xRxxxxBZx-1 switching controller from Infineon for flyback topology.

For buck topology, see the design guide.

CoolSET™

Infineon's CoolSET™ AC-DC integrated power stages in fixed-frequency switching scheme offers increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protective features, and reduced system costs and is ideally suited for auxiliary power supply applications in a wide variety of potential applications such as:

- SMPS
- Home appliances
- Server
- Telecom

Table of contents

About this document **1**
Table of contents **2**
1 Introduction **4**
2 Description **5**
2.1 List of features 5
2.2 Pin configuration and functionality 5
3 Overview of fixed frequency flyback converter **7**
4 Functional description and component design **8**
4.1 V_{CC} pre-charging and typical V_{CC} voltage during startup 8
4.1.1 V_{CC} capacitor 9
4.2 Soft start 10
4.3 Normal operation 10
4.3.1 PWM operation and peak current mode control 10
4.3.1.1 Switch-on determination 11
4.3.1.2 Switch-off determination 11
4.3.2 Current sensing 11
4.3.3 Frequency reduction 12
4.3.4 Slope compensation 13
4.3.5 Oscillator and frequency jittering 14
4.3.6 Modulated gate drive 14
4.4 Peak current limitation (PCL) 15
4.4.1 Propagation delay compensation 16
4.5 ABM with selectable power level 17
4.5.1 Entering ABM operation 17
4.5.2 During ABM operation 17
4.5.3 Leaving ABM operation 18
4.5.4 ABM configuration 20
4.6 Non-isolated/isolated configuration 20
4.6.1 Non-isolated FB 21
4.6.2 Isolated FB 22
4.7 Protection functions 23
4.7.1 V_{CC} OV/UV 23
4.7.2 Over-load/open-loop 23
4.7.3 Over-temperature 23
4.7.4 V_{CC} short-to-GND 23
4.7.5 Protection modes 24
5 Schematic **26**
6 PCB layout recommendation **27**
7 Output power of CoolSET™ 5th Generation Fixed Frequency Plus ICs **28**
8 CoolSET™ 5th Generation Fixed Frequency Plus fixed frequency FLYCAL design example **31**
8.1 Pre-calculation 32
8.2 Input diode bridge (BR1) 33
8.3 Input capacitor (C1) 33
8.4 Transformer design (TR1) 35
8.5 Post calculation 38
8.6 Transformer winding design 39

Table of contents

8.6.1 Primary winding 40
8.6.2 Secondary 1 winding (V_{Out1}) 41
8.6.3 Secondary 2 winding (V_{Out2}) 43
8.7 Clamping network 44
8.8 CS resistor 45
8.9 Output rectifier 46
8.9.1 Output 1 46
8.9.2 Output 2 48
8.10 V_{CC} diode and capacitor 49
8.11 Calculation of losses 50
8.12 CoolSET™/MOSFET temperature 53
8.13 Output regulation (non-isolated) 54
References 55
Design support 56
Revision history 57
Disclaimer 58

1 Introduction

This design guide is for a fixed frequency flyback converter using the latest CoolSET™ 5th Generation Fixed Frequency Plus ICE5xRxxxxBZx-1 switching controller.

The IC is optimized for offline SMPS applications including home appliances/white goods, TVs, PCs, servers, and notebook adapters. The frequency reduction with soft gate-driving and frequency-jitter operation offers lower EMI and better efficiency between light and medium loads. The selectable entry/exit standby power active burst mode (ABM) enables flexibility and low-power consumption in standby mode with small and controllable output voltage ripple. The product has a wide operating range (10~30.5 V) of IC power supply and lower power consumption. The numerous protection functions give full protection to the power supply system in failure situations. All of these features make the ICE5xRxxxxBZx-1 an outstanding CoolSET™ switching controller for fixed frequency flyback converter.

2 Description

2.1 List of features

- Integrated 700 V/800 V/950 V avalanche rugged CoolMOS™
- Enhanced ABM with selectable entry and exit standby power
- Frequency reduction for better overall system efficiency
- Fast startup, achieved with cascode configuration
- Discontinuous conduction mode (DCM) and continuous conduction mode (CCM) operation with slope compensation
- Frequency jitter and soft gate-driving for low EMI
- Built-in digital soft start
- Cycle-to-cycle peak current limitation (PCL)
- Integrated error amplifier to support direct feedback (FB) in a non-isolated flyback converter
- Comprehensive protection with V_{CC} OV, V_{CC} undervoltage (UV), over-load/open-loop, overtemperature
- All protections are in auto-restart mode
- Limited charging current for V_{CC} short-to-GND
- Pb-free lead plating, halogen-free mold compound, RoHS compliant

2.2 Pin configuration and functionality

The pin configuration is shown in Figure 1 and the functions are described in Table 1.

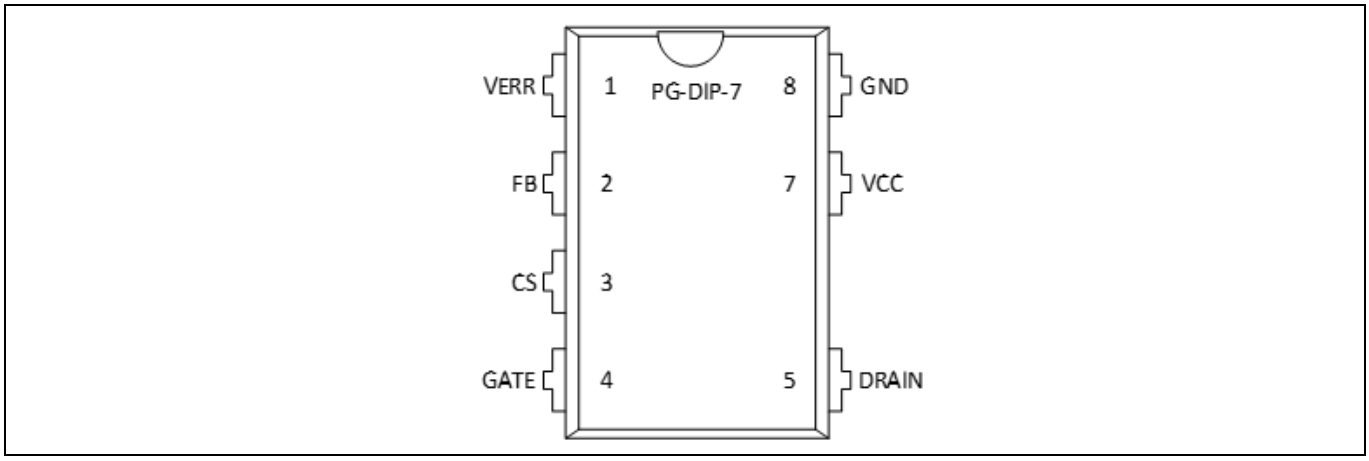

Figure 1 Pin configuration

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	VERR	Error amplifier The VERR pin is internally connected to the transconductance error amplifier for a non-isolated converter. Connect this pin to GND for an isolated converter.
2	FB	FB and ABM entry/exit control The FB pin combines the functions of FB control, selectable burst entry/exit control and over-load/open-loop protection.
3	CS	Current sense The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the FB voltage) internally.
4	GATE	Gate driver output The GATE pin is connected to the gate of the power MOSFET and a pull-up resistor is connected from the bus voltage to turn on the power MOSFET for charging up the V_{CC} capacitor during startup.
5	DRAIN	Drain (drain of integrated CoolMOS™) The DRAIN pin is connected to the drain of the integrated CoolMOS™ power MOSFET.
7	VCC	VCC (positive voltage supply) The VCC pin is the positive voltage supply to the IC. The operating range is between V_{VCC_OFF} and V_{VCC_OVP}.
8	GND	Ground The GND pin is the common ground of the controller.

3 Overview of fixed frequency flyback converter

Figure 2 shows the typical application of ICE5xRxxxxBZx-1 switching controller in an isolated fixed frequency flyback converter using TL431 IC and an optocoupler.

Figure 3 shows the typical application of ICE5xRxxxxBZx-1 switching controller in a non-isolated fixed frequency flyback converter using an integrated error amplifier.

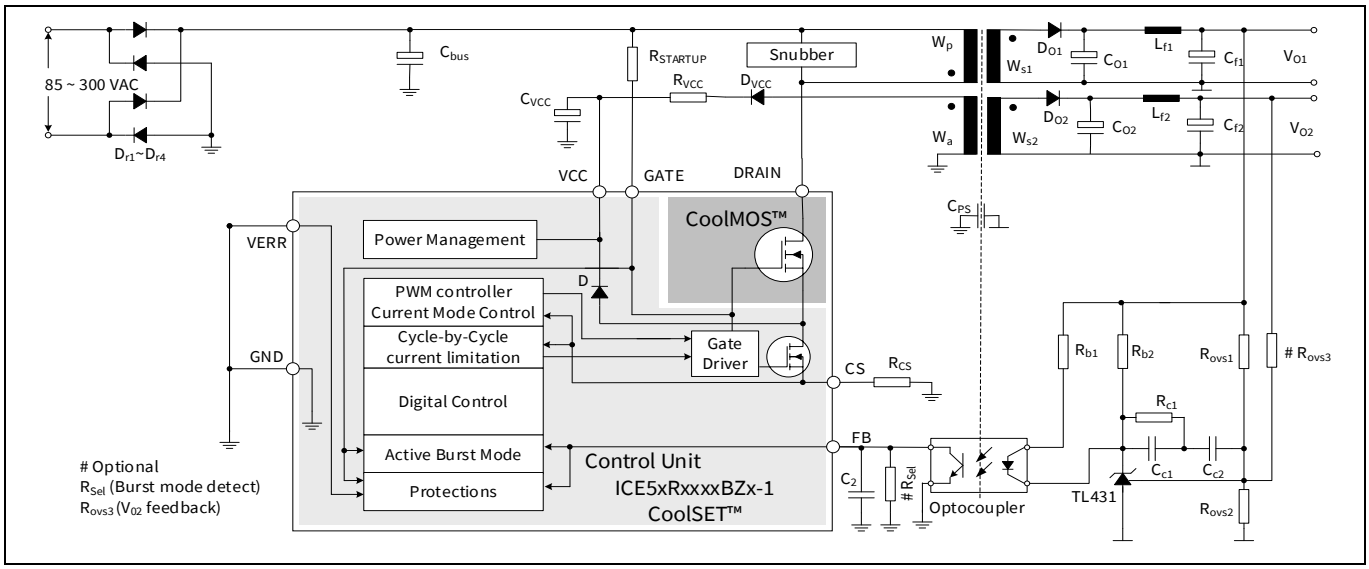

Figure 2 Typical application in an isolated fixed frequency flyback converter using TL431 IC and an optocoupler

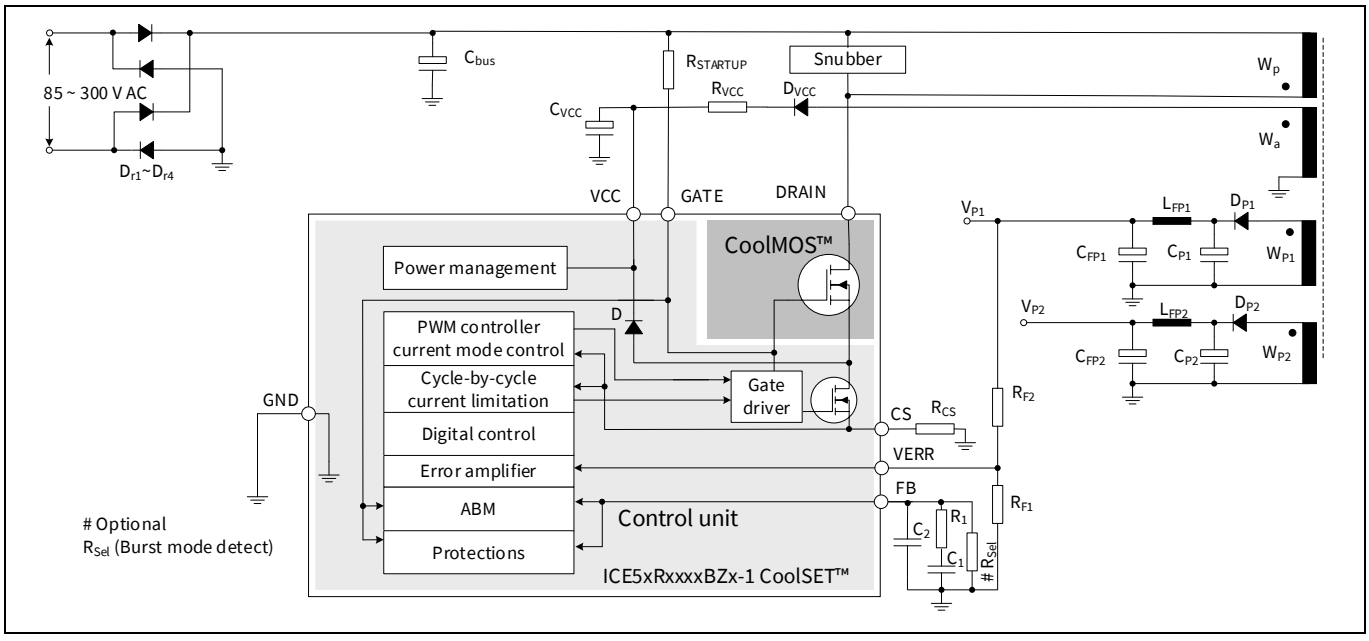

Figure 3 Typical application in a non-isolated flyback converter using an integrated error amplifier

4 Functional description and component design

4.1 V_{CC} pre-charging and typical V_{CC} voltage during startup

When AC line input voltage is applied, a rectified voltage appears across the capacitor (C_{bus}) (see Figure 2, Figure 3). The pull-up resistor ($R_{StartUp}$) provides a current to charge the input capacitance (C_{iss}) of the power MOSFET, generating one voltage level. If the voltage across input capacitance (C_{iss}) is sufficiently high, the power MOSFET will turn on and the V_{CC} capacitor will be charged through primary inductance of transformer (L_P), the power MOSFET and the internal diode with two steps of constant current source ($I_{VCC_Charge1}$[1] and $I_{VCC_Charge3}$[1]).

A very small constant current source ($I_{VCC_Charge1}$) charges the V_{CC} capacitor until V_{CC} reaches V_{VCC_SCP} to protect the controller from a V_{CC} pin short-to-GND during startup. After this, the second step constant current source ($I_{VCC_Charge3}$) is provided to further charge the V_{CC} capacitor, until V_{CC} exceeds the turn-on threshold V_{VCC_ON}. As shown in Phase I in Figure 4, the V_{CC} voltage increases linearly, with two steps.

Note: The recommended typical value for $R_{StartUp}$ is 50 MΩ (20 MΩ~100 MΩ). $R_{StartUp}$ value is directly proportional to $t_{StartUp}$ and inversely proportional to no-load standby power.

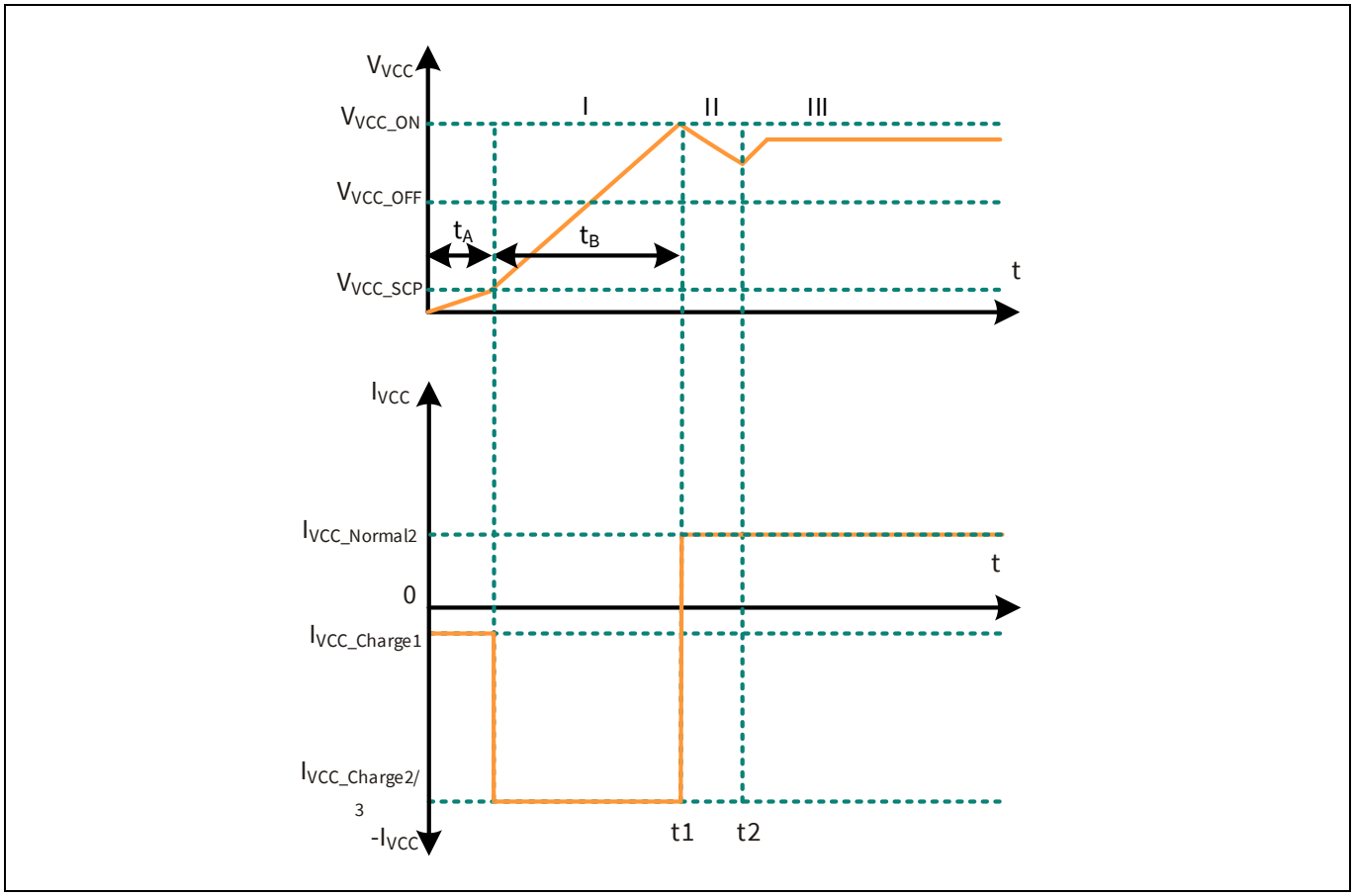

Figure 4 V_{CC} voltage and current at startup

[1] $I_{VCC_Charge1/2/3}$ is charging current from the controller to the V_{CC} capacitor during startup.

The time taken for the V_{CC} pre-charging can be calculated as follows:

$$t_{\mathrm{StartUp}} = t_{\mathrm{A}} + t_{\mathrm{B}} = \frac{V_{VCC_SCP} \cdot C_{VCC}}{I_{VCC_Charge1}} + \frac{(V_{VCC_ON} - V_{VCC_SCP}) \cdot C_{VCC}}{I_{VCC_Charge3}}$$

Equation 1 Time for V_{cc} pre-charging

Where,

V_{VCC_SCP} = V_{CC} short-circuit protection voltage

C_{VCC} = V_{CC} capacitor

V_{VCC_ON} = V_{CC} turn-on threshold voltage

$I_{VCC_Charge1}$ = V_{CC} charge current 1

$I_{VCC_Charge3}$ = V_{CC} charge current 3

When the V_{CC} voltage exceeds the V_{VCC_ON} at time t_1, the IC begins to operate with a soft start. Because of power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the V_{CC} capacitor before the output voltage is built up, the V_{CC} voltage drops (Phase II). After the output voltage rises close to regulation, the auxiliary winding starts to charge the V_{CC} capacitor from the time t_2 onwards, delivering the power to the IC. The V_{CC} will then reach a constant value depending on output load.

4.1.1 V_{CC} capacitor

As there is a V_{CC} UV protection, select the V_{CC} capacitor to be large enough to ensure that enough energy is stored in the V_{CC} capacitor so that the V_{CC} voltage will not drop below the V_{CC} UV protection threshold V_{VCC_OFF} before the auxiliary power kicks in. Therefore, the minimum capacitance should be as follows:

$$C_{VCC} > \frac{I_{VCC_normal2} \times t_{ss}}{V_{VCC_ON} - V_{VCC_OFF}}$$

Equation 2 Minimum capacitance

Where,

C_{VCC} = V_{CC} capacitor

$I_{VCC_normal2}$ = V_{CC} supply current with active gate

t_{ss} = Soft start time

During ABM condition where the auxiliary winding cannot provide enough power to supply the IC because of the burst switching, the V_{CC} voltage may drop below the V_{VCC_OFF}. Therefore, increase the capacitance, as the calculation above may not be enough.

4.2 Soft start

After the supply voltage of the IC exceeds V_{VCC_ON}, which corresponds to t_1 of Figure 4, the IC starts switching with a soft start. The soft start implemented is a digital time-based function. The preset soft start time is t_{SS} (12 ms) with four steps (see Figure 5). If not limited by other functions, the peak voltage on the CS pin will increase incrementally from V_{SS1} to V_{CS_N}. The normal FB loop will take over the control when the output voltage reaches its regulated value.

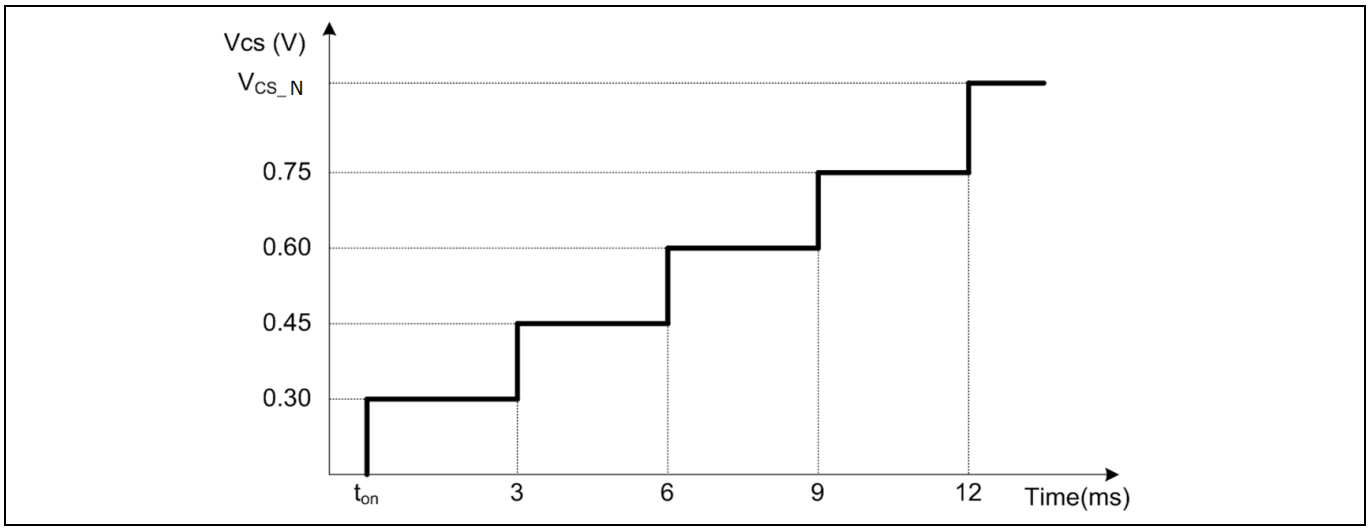

Figure 5 Maximum CS voltage during soft start

4.3 Normal operation

During normal operation, the PWM controller consists of: digital signal processing circuit, regulation control, analog circuit, current measurement unit, and comparator. Details of normal operation are described in the following sections.

4.3.1 PWM operation and peak current mode control

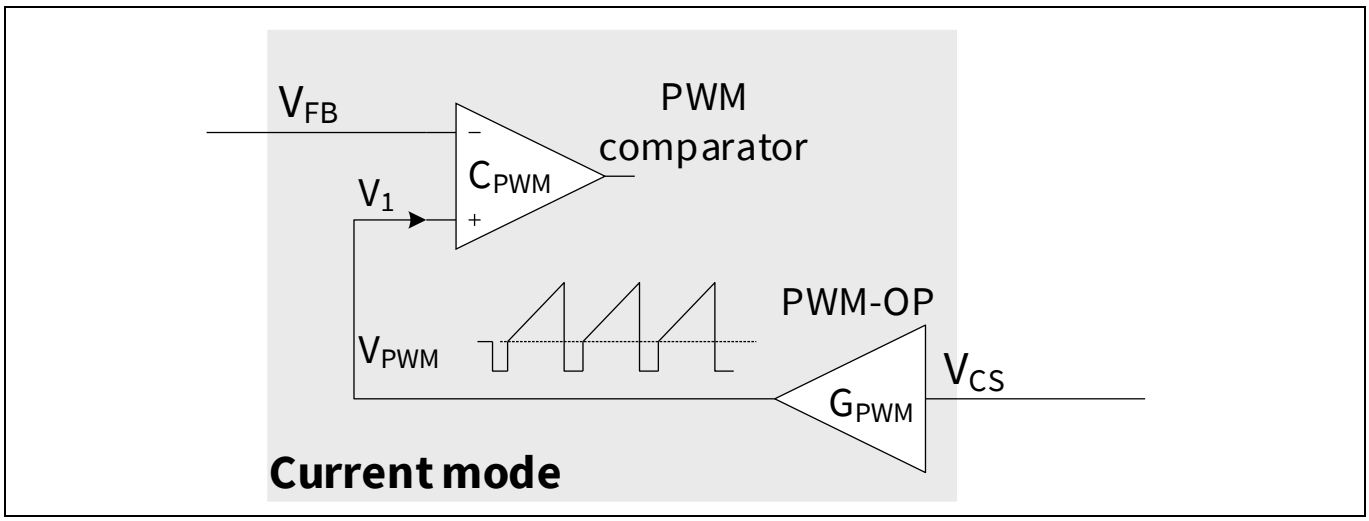

Figure 6 Pulse width modulation block

4.3.1.1 Switch-on determination

The power MOSFET turn-on is synchronized with an internal oscillator, with a switching frequency F_{SW} that corresponds to the voltage level V_{FB} (see Figure 8).

4.3.1.2 Switch-off determination

In peak current mode control, the PWM comparator monitors voltage V_1 (see Figure 6) that represents the instantaneous current of the power MOSFET. When V_1 exceeds V_{FB}, the PWM comparator sends a signal to switch off the gate of the power MOSFET. Therefore, the peak current of the power MOSFET is controlled by the FB voltage V_{FB} (see Figure 7).

At switch-on transient of the power MOSFET, a voltage spike across R_{CS} can cause V_1 to increase and exceed V_{FB}. To avoid a false switch-off, the IC has a blanking time t_{CS_LEB} before detecting the voltage across R_{CS} to mask the voltage spike. Therefore, the minimum turn-on time of the power MOSFET is t_{CS_LEB}.

If the voltage level at V_1 takes a long time to exceed V_{FB}, the IC will implement a maximum duty cycle control to force the power MOSFET to switch off when D_{MAX} = 0.75.

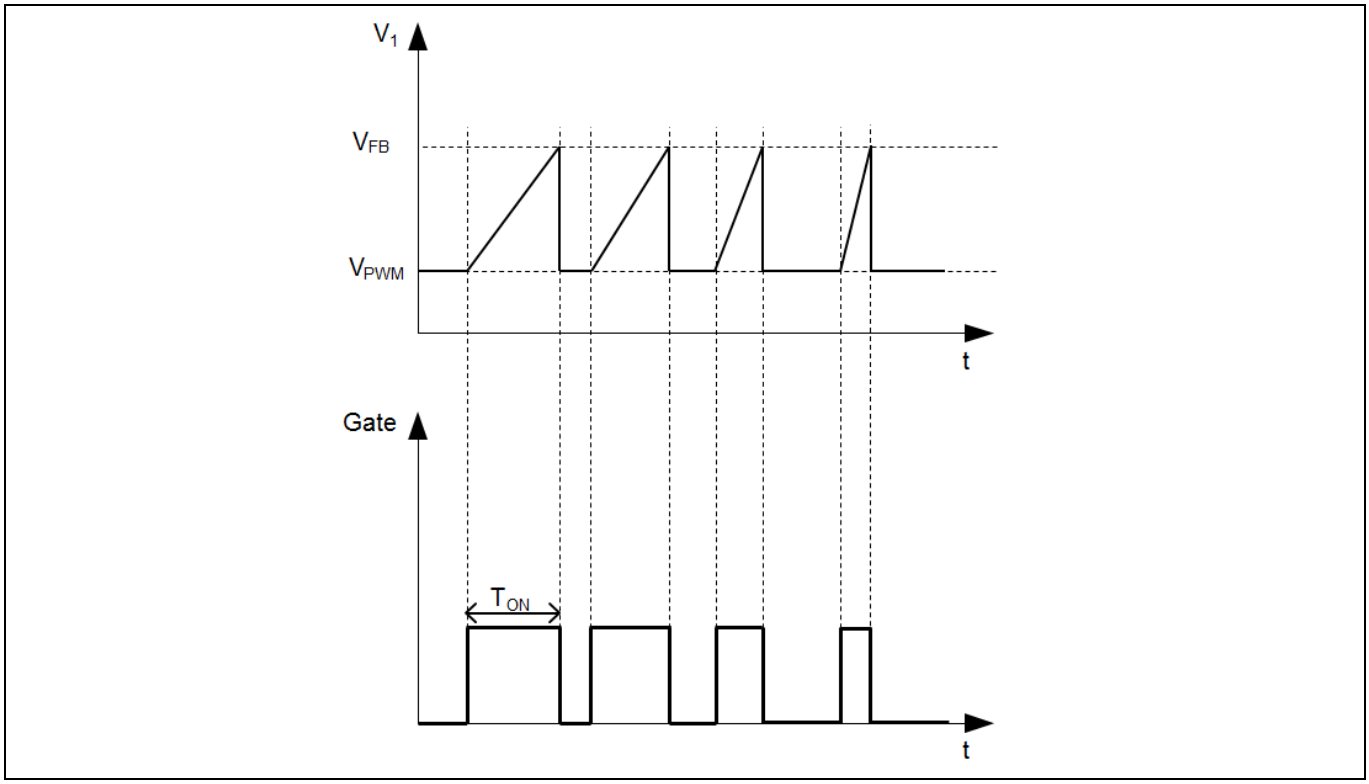

Figure 7 PWM

4.3.2 Current sensing

The power MOSFET current generates a voltage V_{CS} across the CS resistor R_{CS} connected between the CS pin and the GND pin. V_{CS} is amplified with gain G_{PWM}, then added with an offset V_{PWM} to become V_1, as described in the following equation.

$$V_{CS} = I_D \times R_{CS}$$

Equation 3 Current sensing voltage

Where,

V_{CS} = CS pin voltage

I_D = Power MOSFET current

R_{CS} = Resistance of the CS resistor

$$V_1 = V_{\mathrm{CS}} * G_{\mathrm{PWM}} + V_{\mathrm{PWM}}$$

Equation 4 Voltage level

Where,

V_1 = Voltage level compared to V_{FB} as described in Section 4.3.1.2

G_{PWM} = PWM-OP gain

V_{PWM} = Offset for voltage ramp

4.3.3 Frequency reduction

Frequency reduction is implemented to achieve better efficiency at light-load condition. At light-load, the reduced switching frequency F_{SW} improves efficiency by reducing the switching losses.

When load decreases, V_{FB} decreases as well. F_{SW} is dependent on the V_{FB} as shown in Figure 8. Therefore, F_{SW} decreases as the load decreases.

Typically, F_{SW} at high load is 65/100 kHz and starts to decrease at V_{FB} = 1.7 V. There is no further frequency reduction once it reaches the f_{OSCx_MIN} even if the load is further reduced.

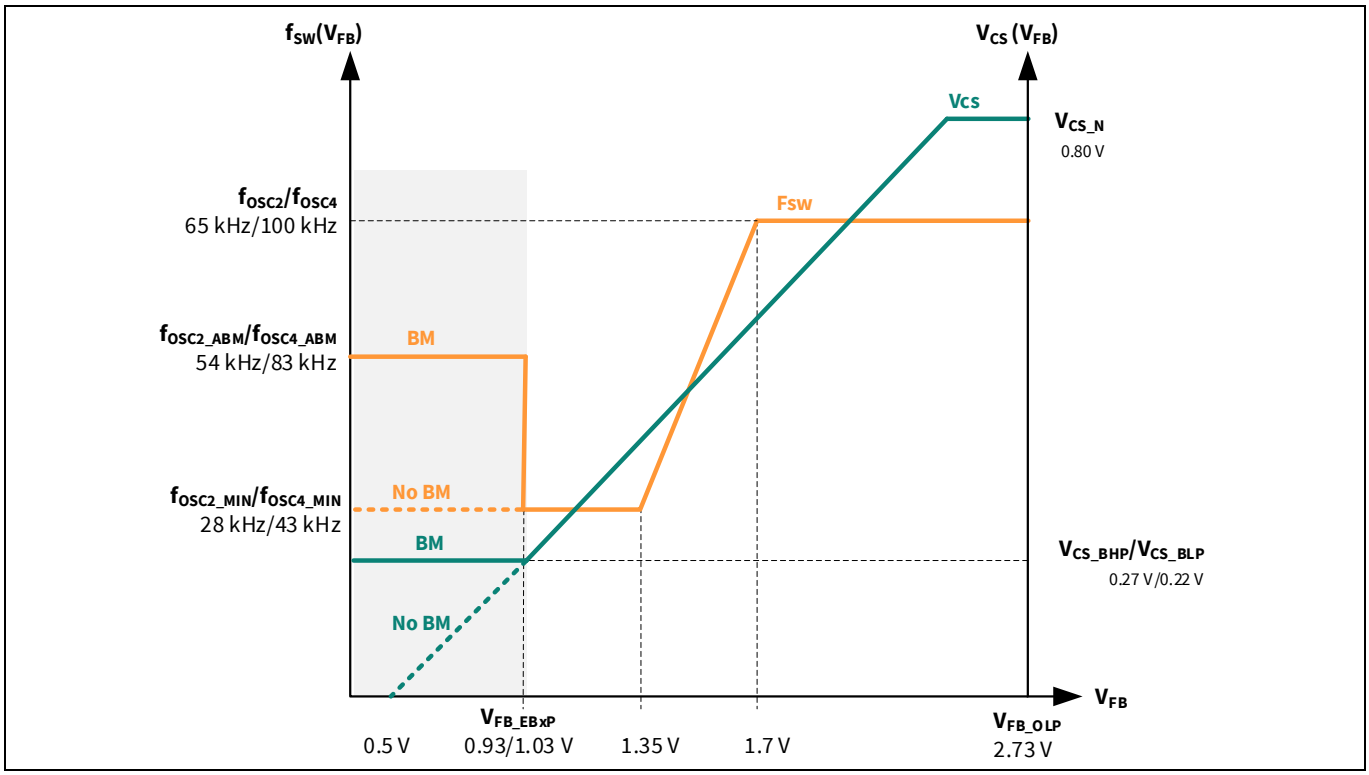

Figure 8 Frequency reduction curve

4.3.4 Slope compensation

In CCM operation, a duty cycle greater than 50 percent may generate a sub-harmonic oscillation. A small perturbation on the transformer flux φ can result in loop instability where the system cannot auto-correct itself, as seen in the following figure right, where $\Delta\varphi_2$ is greater than $\Delta\varphi_1$. $\Delta\varphi_2$ should be less than $\Delta\varphi_1$ for a system to be stable (following figure left). DCM operation is more stable, as the transformer flux always goes to zero.

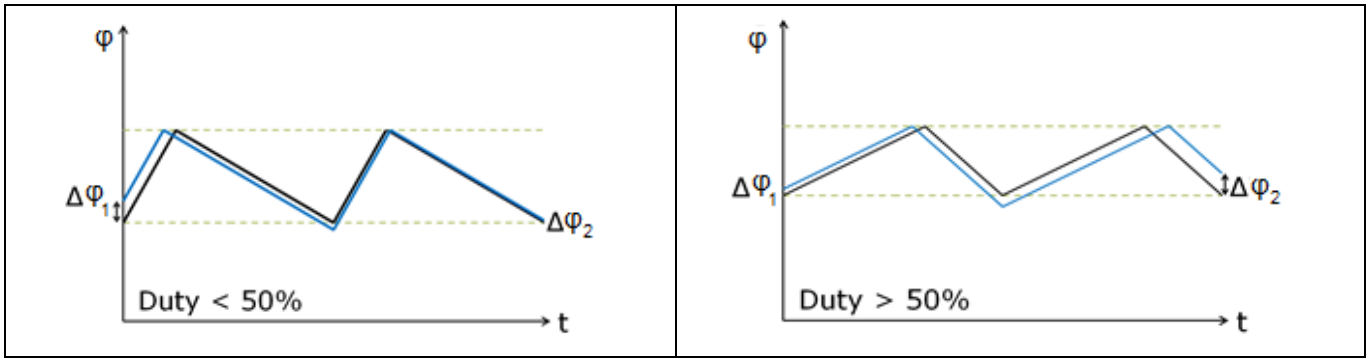

Figure 9 Perturbed transformer charging and discharging flux (black line is the stabilized transformer flux)

ICE5xRxxxxBZx-1 switching controller can operate in CCM. To avoid the sub-harmonic oscillation, slope compensation is added to V_{CS} when the gate of the power MOSFET is turned on for more than 40 percent of the switching cycle period. The relationship between V_{FB} and the V_{CS} for CCM operation is described in following the equation.

$$V_{\mathrm{FB}} = V_{\mathrm{CS}} * G_{\mathrm{PWM}} + V_{\mathrm{PWM}} + M_{\mathrm{COMP}} * (T_{\mathrm{ON}} - 40\% * T_{\mathrm{PERIOD}})$$

Equation 5 CCM operation

Where,

T_{ON} = Gate turn-on time of the power MOSFET

M_{COMP} = Slope compensation rate

T_{PERIOD} = Switching cycle period

As a result of slope compensation, $\Delta\phi_2$ is reduced to smaller than $\Delta\phi_1$. Therefore, the system can stabilize itself as shown in the following figure.

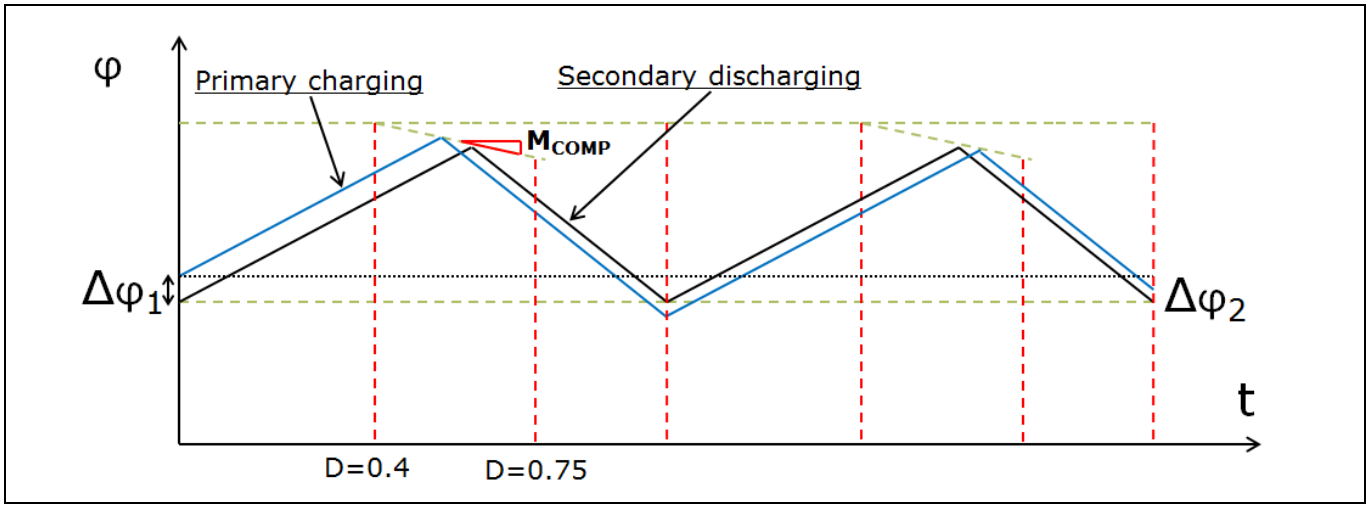

Figure 10 Perturbed transformer flux with slope compensation

The slope compensation circuit is disabled and no slope compensation is added to the V_{CS} pin during ABM operation to save on power consumption.

4.3.5 Oscillator and frequency jittering

The oscillator generates a frequency of 65/100 kHz (depending on part selected) with frequency jittering of ±4 percent at a jittering period of T_{JITTER} (4 ms). The frequency jittering helps to reduce conducted EMI.

A capacitor, current source, and current sink that determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed to achieve a highly accurate switching frequency.

After the soft start period is over and when the IC goes into normal operating mode, the frequency jittering is enabled. There is also frequency jittering during frequency reduction.

4.3.6 Modulated gate drive

The drive stage is optimized for EMI consideration. The switch-on speed is slowed down before it reaches the power MOSFET turn-on threshold. There is a slope control on the rising edge at the output of the driver (see Figure 11). In this way the leading switch spike during turn-on is minimized.

The gate drive is 10 V (V_{GATE_HIGH}). For a 1 nF load capacitance, the typical values of rise time and fall time are 117 ns and 27 ns respectively.

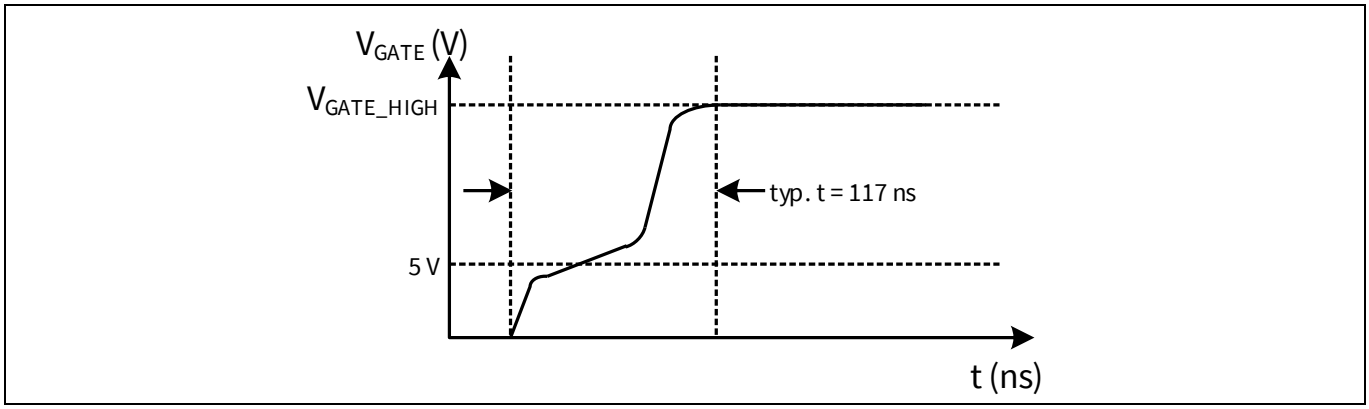

Figure 11 Gate – rising waveform

Do not add a gate discharge resistor on the gate of the power MOSFET or the GATE pin. The discharge resistor together with the $R_{StartUp}$ forms a voltage divider. With the high ratio of the resistance of $R_{StartUp}$ with discharge resistor, the gate voltage of the power MOSFET cannot turn it on and charge the V_{CC} to exceed V_{VCC_ON}. Similarly, connecting a voltage probe on the GATE pin can result in a non-startup or a longer startup time, depending on the probe resistance.

4.4 Peak current limitation (PCL)

There is a cycle-by-cycle PCL realized by the current limit comparator to provide primary overcurrent protection (OCP). The primary current generates a voltage V_{CS} across the CS resistor R_{CS} connected between CS and GND pins. If the voltage V_{CS} exceeds an internal voltage limit V_{CS_N}, the comparator immediately turns off the gate drive.

The primary peak current I_{PEAK_PRI} can be calculated as follows:

$$I_{\mathrm{PEAK_PRI}} = V_{\mathrm{CS_N}} / R_{\mathrm{CS}}$$

Equation 6 Primary peak current

Where,

I_{PEAK_PRI} = Maximum peak current in the primary

V_{CS_N} = Threshold voltage for the PCL

R_{CS} = Resistance of the CS resistor

To avoid mis-triggering caused by MOSFET switch-on transient voltage spikes, a leading edge blanking (LEB) time (t_{CS_LEB}) is integrated into the current sensing path.

Note: In case of high switch-on noise at the CS pin, the IC can switch off immediately after the LEB time, especially at light-load high-line conditions. To avoid this, a noise-filtering ceramic capacitor (e.g., 100 pF~100 nF) can be added across CS pin and GND pin.

4.4.1 Propagation delay compensation

In case of overcurrent detection, there is always a propagation delay from sensing the V_{CS} to switching off the power MOSFET. An overshoot on the peak current I_{peak} caused by the delay depends on the ratio of dI/dt of the primary current (see Figure 12).

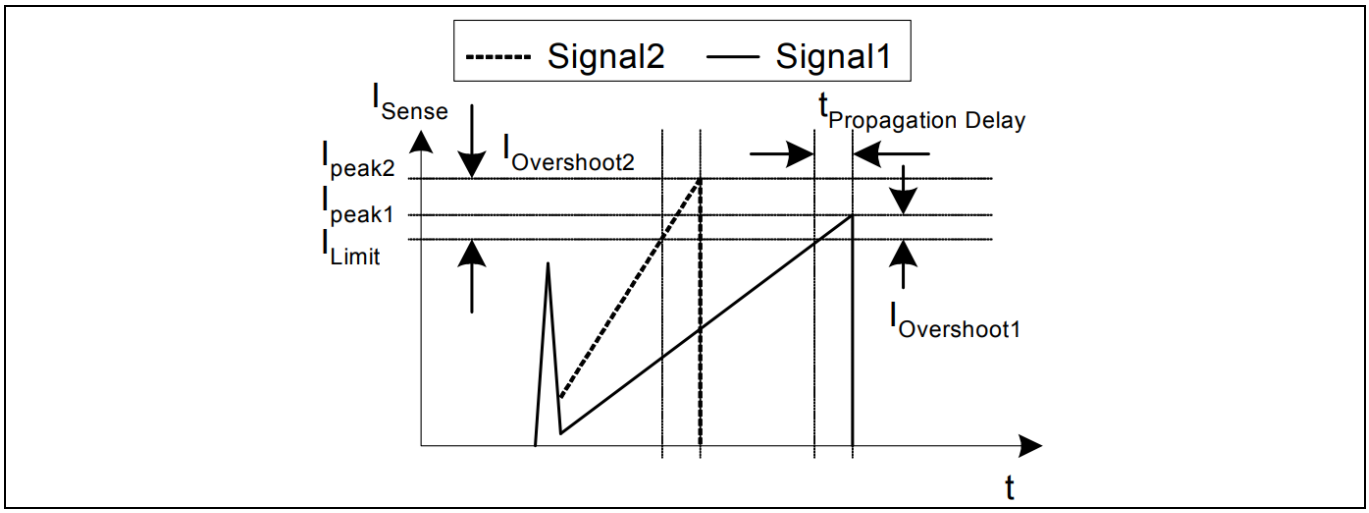

Figure 12 Current limiting

The overshoot of Signal2 is larger than Signal1 due to the steeper rising waveform. This change in the slope depends on the AC input voltage. Propagation delay compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Therefore, the propagation delay time between exceeding the CS threshold V_{CS_N} and the switching off of the power MOSFET is compensated over a wide bus voltage range. Current limiting becomes more accurate, which will result in a minimum difference of over-load protection triggering power between low and high AC-line input voltage.

Under CCM operation, the same V_{CS} does not result in the same power. To achieve a close over-load triggering level for CCM operation, the ICE5xRxxxxBZx-1 switching controller has implemented a two-curve compensation, as shown in Figure 13. One of the curves is used for T_{ON} greater than 0.40 duty cycle and the other is for T_{ON} lower than 0.40 duty cycle.

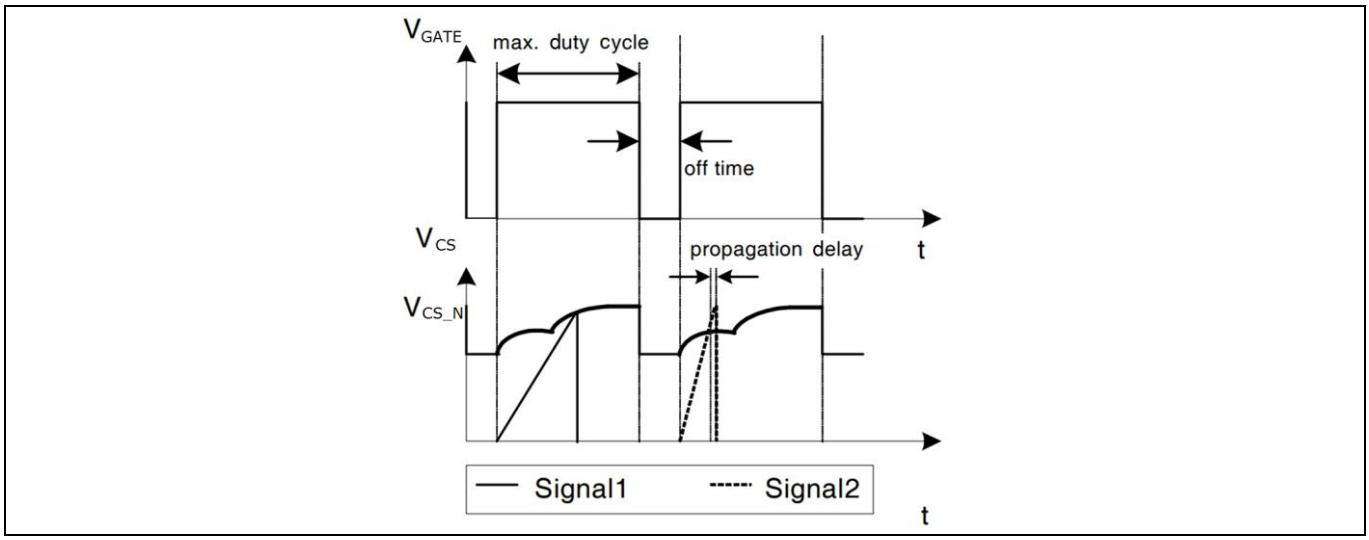

Figure 13 Dynamic voltage threshold V_{CS_N}

Similarly, the same concept of propagation delay compensation is also implemented in ABM operation at a reduced level. With this implementation, the entry and exit burst mode power can remain close between low and high AC-line input voltage.

4.5 ABM with selectable power level

At light load, the IC enters ABM operation to minimize power consumption. Details of ABM operation are explained in the following sections.

4.5.1 Entering ABM operation

The system will enter ABM operation when two conditions are met:

- The FB voltage is lower than the threshold of V_{FB_EBLP}/V_{FB_EBHP} depending on burst configuration option set up
- A certain blanking time t_{FB_BEB}.

Once both of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This dual-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM operation only when the output power is really low.

The threshold power to enter burst mode can be determined using the following equation.

$$P_{\text{enter_burst}} = \frac{1}{2} \cdot L_p \cdot f_{OSCx_MIN} \cdot \left(\frac{V_{FB_EBxP} - V_{PWM}}{R_{CS} \cdot G_{PWM}}\right)^2$$

Equation 7 Threshold power

Where,

L_P = Primary inductance

f_{OSCx_MIN} = Minimum switching frequency (f_{osc2_min} or f_{osc4_min})

V_{FB_EBxP} = V_{FB} entering ABM

The burst power as a ratio to the maximum input power P_{IN_Max} can be expressed in the following equation.

$$\frac{P_{enter_burst}}{P_{IN_Max}} = \frac{f_{OSCx_MIN}}{f_{OSC4}} \cdot \left(\frac{V_{FB_EBxP} - V_{PWM}}{V_{CS_N} \cdot G_{PWM}}\right)^2$$

Equation 8 Burst power

4.5.2 During ABM operation

After entering ABM, the PWM section will be inactive, making the V_{Out} start to decrease. As the V_{Out} decreases, the V_{FB} rises. Once V_{FB} exceeds V_{FB_BOn}, the internal circuit is again activated by the internal bias to start the switching.

If the PWM is still operating and the output load is still low, V_{Out} increases and the V_{FB} signal start to decrease. When V_{FB} reaches the low threshold V_{FB_BOff}, the internal bias is reset again and the PWM section is disabled, with no switching until V_{FB} increases and once again exceeds the V_{FB_BOn} threshold.

In ABM, V_{FB} is like a sawtooth waveform swinging between V_{FB_BOff} and V_{FB_BOn}, as shown in Figure 14.

During ABM, for example the switching frequency f_{OSC4_ABM} is 83 kHz. The peak current I_{PEAK_ABM} of the power MOSFET is defined as follows:

$$I_{\mathrm{PEAK_ABM}} = V_{\mathrm{CS_BxP}}/R_{\mathrm{CS}}$$

Equation 9 Peak current of the power MOSFET

Where,

V_{CS_BxP} = PCL in ABM

4.5.3 Leaving ABM operation

The FB voltage immediately increases if there is a sudden increase in the output load. When V_{FB} exceeds V_{FB_LB}, it will leave ABM and the PCL threshold voltage will return back to V_{CS_N} immediately.

The power on leaving ABM can be determined using the following equation.

$$P_{\mathrm{leave_burst}} = \frac{1}{2} \cdot L_p \cdot f_{OSC4_ABM} \cdot \left(\frac{V_{CS_BxP}}{R_{CS}}\right)^2$$

Equation 10 Power on leaving ABM

Where,

f_{OSC4_ABM} = ABM switching frequency

V_{CS_BxP} = PCL in ABM

Therefore, the ratio of the power on leaving ABM to maximum input power can be determined using the following equation.

$$\frac{P_{leave_burst}}{P_{IN_Max}} = \frac{f_{OSC4_ABM}}{f_{OSC4}} \cdot \left(\frac{V_{CS_BxP}}{V_{CS_N}}\right)^2$$

Equation 11 Ratio of the power on leaving ABM

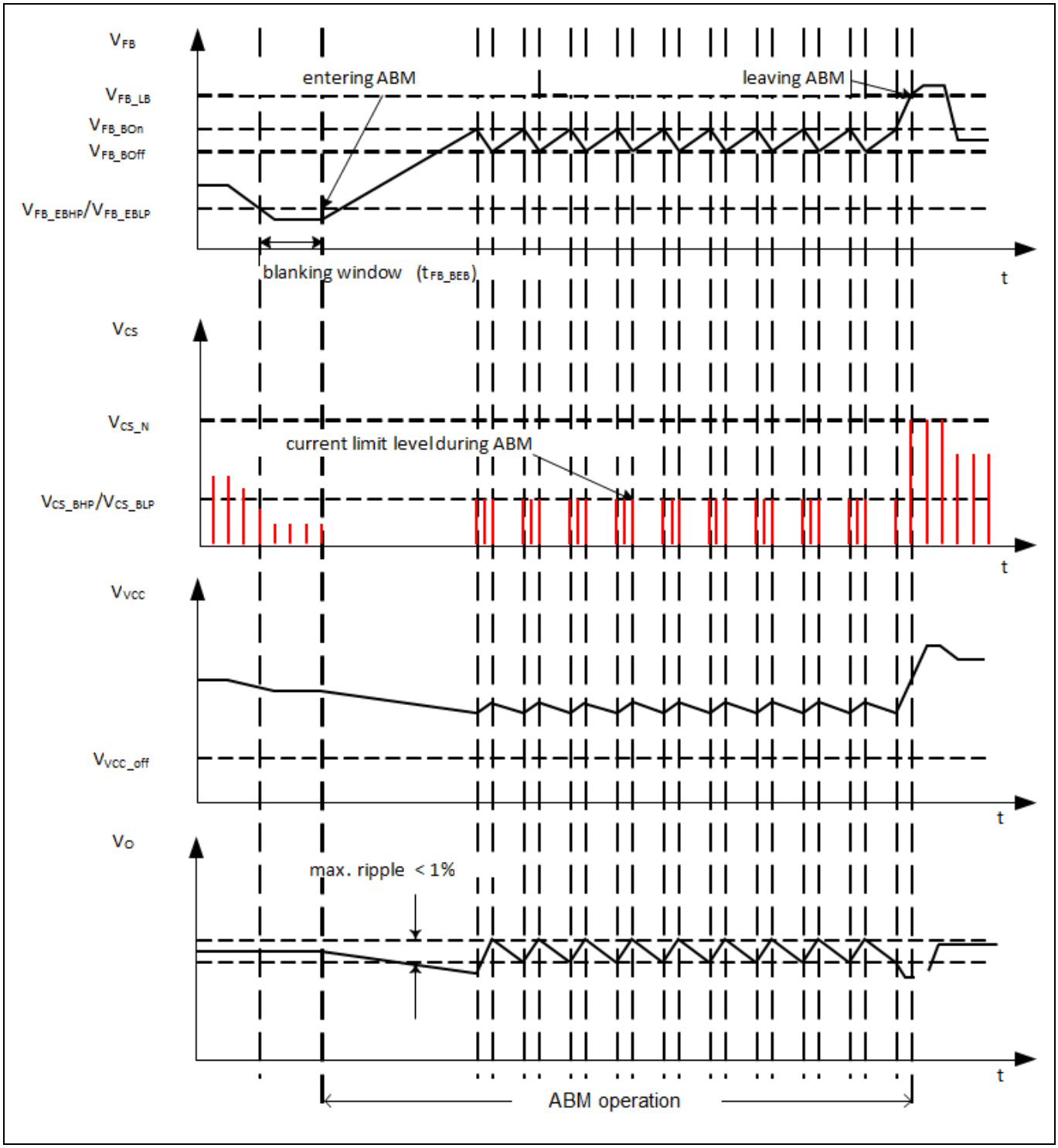

Figure 14 Signals in ABM

4.5.4 ABM configuration

The burst mode entry level can be selected by changing the resistance R_{Sel} at the FB pin. There are three configuration options depending on R_{Sel}, which corresponds to the options of no ABM (Option 1), low range of ABM power (Option 2), and high range of ABM power (Option 3). The following table shows the control logic for the entry and exit levels with the FB voltage.

Table 2 ABM configuration option set-up

Option	R_{Sel}	V_{FB}	V_{CS_BxP}	Entry level		Exit level	
				V_{FB_EBxP}	Percentage of P_{IN_Max}	V_{FB_LB}	Percentage of P_{IN_Max}
1	400~ 470 kΩ	$V_{FB} < V_{FB_P_BIAS1}$	–	–	No ABM	–	No ABM
2	720~790 kΩ	$V_{FB_P_BIAS1} < V_{FB} < V_{FB_P_BIAS2}$	0.22 V	0.93 V	~3 %	2.73 V	~6.2 %
3 (default)	preferable open	$V_{FB} > V_{FB_P_BIAS2}$	0.27 V	1.03 V	~4.5 %	2.73 V	~9.4 %

P_{IN_Max} is the input power before the over-load protection is triggered.

During startup of the IC, the controller presets the ABM selection to Option 3, the FB resistor (R_{FB}) is turned off by internal switch S2 (see Figure 15) and a current source I_{sel} is turned on instead. From V_{CC} = 4.4 V to the V_{CC} on-threshold, the FB pin will source current I_{Sel} through R_{Sel} and external FB network. When V_{CC} reaches the V_{CC} on-threshold, the FB voltage is sensed. The burst mode option is then chosen according to the FB voltage level. After finishing the selection, any change on the FB level will not change the burst mode option, and the current source (I_{sel}) is turned off while the FB resistor (R_{FB}) is connected back to the circuit.

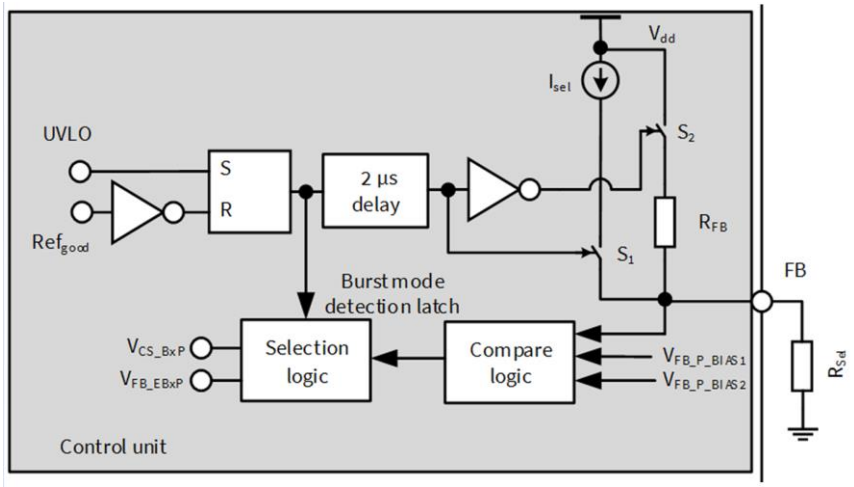

Figure 15 ABM detect and adjust

4.6 Non-isolated/isolated configuration

ICE5xRxxxxBZx-1 switching controller has a VERR pin, which is connected to the input of an integrated error amplifier to support non-isolated flyback application (see Figure 3). When the V_{CC} is charging and before reaching the V_{CC} on-threshold, a current source $I_{ERR_P_BIAS}$ from the VERR pin together with R_{F1} and R_{F2} will generate a voltage across it. If the VERR voltage is more than $V_{ERR_P_BIAS}$ (0.2 V), non-isolated configuration is selected; otherwise, isolated configuration is selected. In isolated configuration, the error amplifier output is disconnected from the FB pin.

Connect the VERR pin to GND if an error amplifier is not used or if isolated configuration is selected.

4.6.1 Non-isolated FB

In case of non-isolated configuration (see Figure 3), the voltage divider R_{F1} and R_{F2} is used to sense the output voltage and compare it with the internal reference voltage V_{ERR_REF}. The difference between the sensed voltage and the reference voltage is converted as an output current by the error amplifier. The output current will charge/discharge the resistor and capacitor network connected at the FB pin for the loop compensation.

To properly detect a non-isolated configuration, the minimum resistance for the parallel combination of resistors R_{F1} and R_{F2} is calculated as follows:

$$R_{F1//F2} \geq V_{ERR_P_BIAS_max} / I_{ERR_P_BIAS_min} = 0.24\,V / 9.5\mu A = 25.3\,k\Omega$$

Equation 12 Minimum resistance for parallel resistors

Where,

$R_{F1//F2}$ = Parallel combination of R_{F1} and R_{F2}

$V_{ERR_P_BIAS_max}$ = Maximum voltage for error amplifier mode

$I_{ERR_P_BIAS_min}$ = Minimum bias current for error amplifier mode

The output voltage V_{P1} (see Figure 3) is set by R_{F1} and R_{F2} using the following equation.

$$R_{F2} = R_{F1} \cdot \left(\frac{V_{P1}}{V_{ERR_REF}} - 1 \right)$$

Equation 13 Voltage divider resistors

Where,

R_{F1} and R_{F2} = Voltage divider resistors

V_{P1} = Output voltage

V_{ERR_REF} = Error amplifier reference voltage

4.6.2 Isolated FB

In an isolated configuration, the output is usually sensed by a TL431 IC, and the output is fed to the FB pin by the optocoupler (see Figure 16). Inside the IC, the FB pin is connected to a (V_{REF}) 3.3 V reference voltage through an internal pull-up resistor R_{FB}. Outside the IC, this pin is connected to the collector of the optocoupler. Normally, a ceramic capacitor C_{FB}, e.g., 1 nF, can be placed between this pin and GND to filter out noise.

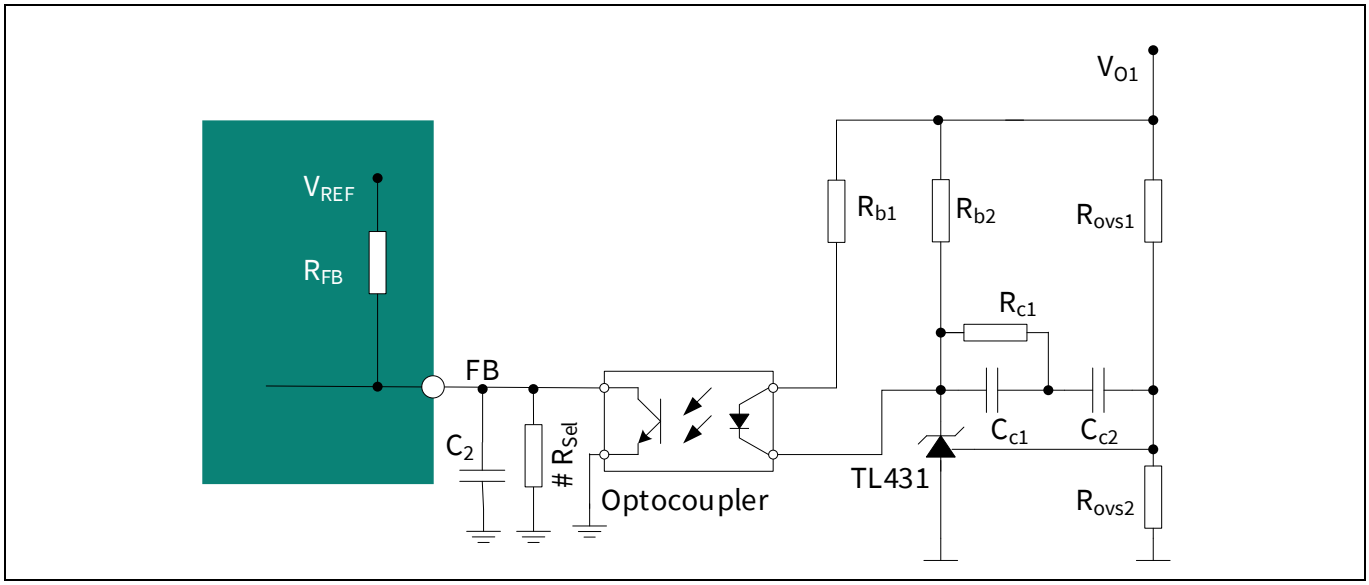

Figure 16 FB circuit for isolated configuration

The output voltage V_{O1} (see Figure 16) is set by R_{OVS1} and R_{OVS2} using the following equation.

$$R_{OVS1} = R_{OVS2}\left(\frac{V_{O1}}{V_{REF_TL}} - 1\right)$$

Equation 14 Output voltage of divide resistors

Where,

R_{OVS1} and R_{OVS2} = Voltage divider resistors

V_{O1} = Output voltage

V_{REF_TL} =: TL431 reference voltage

4.7 Protection functions

ICE5xRxxxxBZx-1 safety controller provides numerous protection functions that considerably improve the power supply system robustness, safety, and reliability. The following table summarizes these protection functions and the corresponding protection mode, whether non-switch auto-restart, auto-restart, or extended cycle skip auto-restart. See Figure 17, Figure 18, and Figure 19 for the waveform illustration of the protection modes.

Table 3 Protection functions

Protection functions	Normal mode	Burst mode		Protection mode
		Burst ON	Burst OFF	
V_{CC} OV	√	√	NA[2]	Extended cycle skip auto-restart
V_{CC} UV	√	√	√	Auto-restart
Over-load/open-loop	√	NA[2]	NA[2]	Extended cycle skip auto-restart
Over-temperature	√	√	√	Non-switch auto-restart
V_{CC} short-to-GND	√	√	√	No startup

4.7.1 V_{CC} OV/UV

During operation, the V_{CC} voltage is continuously monitored. If V_{CC} is either below V_{VCC_OFF} for 50 µs ($t_{VCC_OFF_B}$) or above V_{VCC_OVP} for 55 µs ($t_{VCC_OVP_B}$), the power MOSFET is kept switched off. After the V_{CC} voltage falls below the threshold V_{VCCoff}, the new startup sequence is activated. The V_{CC} capacitor is then charged up. After the voltage exceeds the threshold V_{VCC_ON}, the IC begins to operate with a new soft start.

4.7.2 Over-load/open-loop

In case of open control-loop or output over-load, the FB voltage will be pulled up. When V_{FB} exceeds V_{FB_OLP} after a blanking time of $t_{FB_OLP_B}$, the IC enters odd-skip auto-restart mode. The blanking time enables the converter to provide peak power in case the increase in V_{FB} is due to a sudden load increase.

4.7.3 Over-temperature

If the junction temperature of the controller exceeds T_{jcon_OTP}, the IC enters overtemperature protection (OTP) in auto-restart mode. The IC is also implemented with a 40°C hysteresis. It means the IC can only be recovered from OTP when the controller junction temperature drops 40°C lower than the OT trigger point.

4.7.4 V_{CC} short-to-GND

To limit the power dissipation of the startup circuit at V_{CC} short-to-GND, the V_{CC} charging current is limited to a minimum level of $I_{VCC_Charge1}$. With such low current, the power loss of the IC is limited to prevent over-heating.

[2] Not applicable.

4.7.5 Protection modes

All the protections are in auto-restart mode with a new soft start sequence. The three auto-restart modes are illustrated in the following figures.

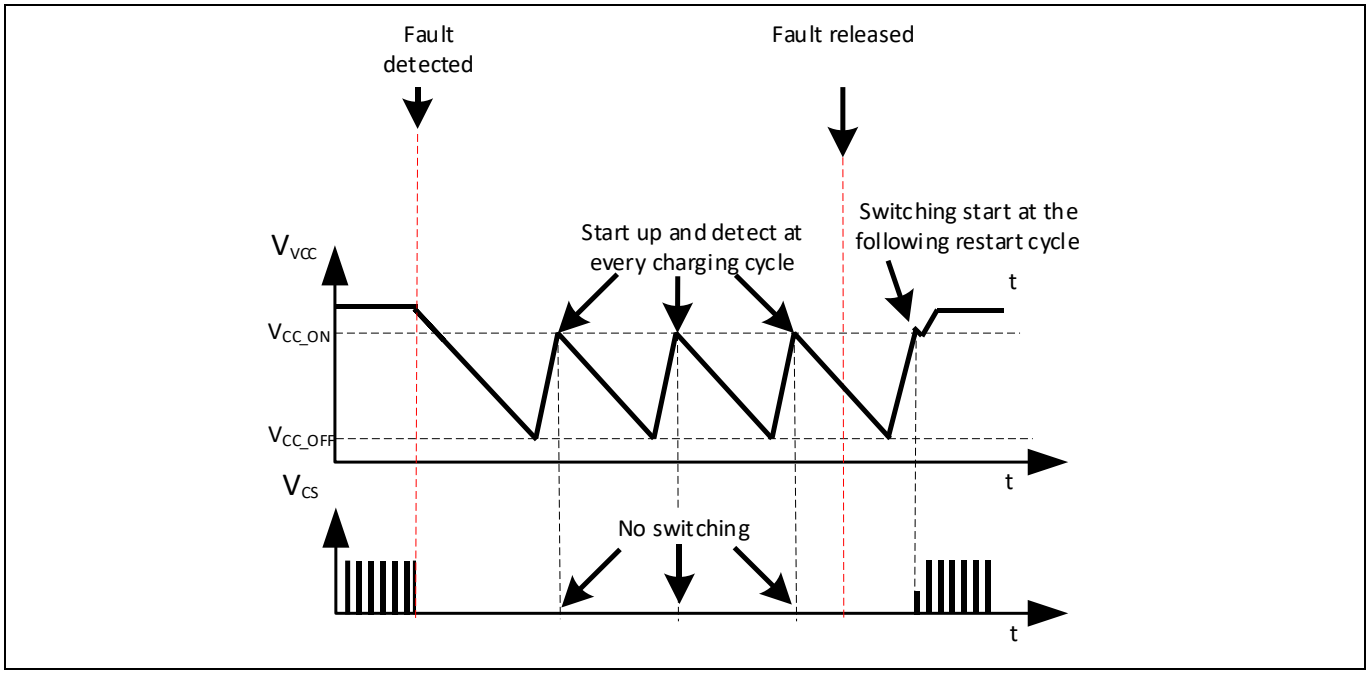

Figure 17 Non-switch auto-restart mode

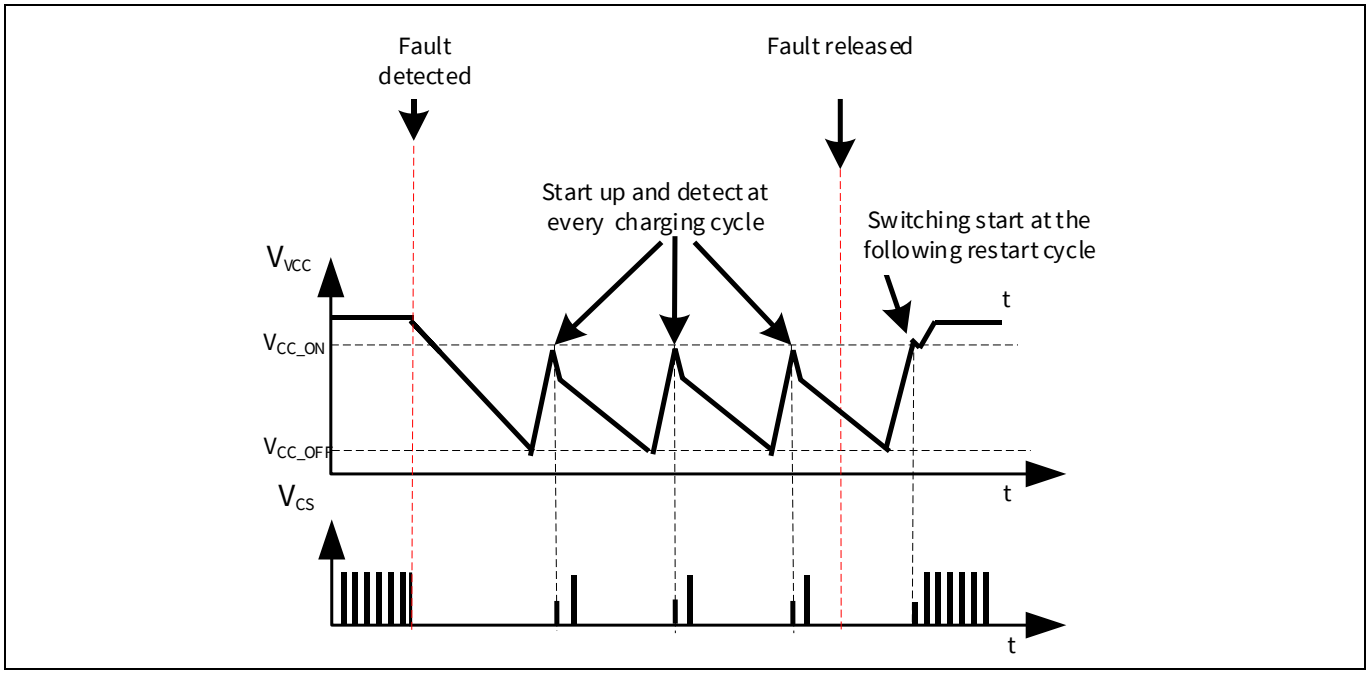

Figure 18 Auto-restart mode

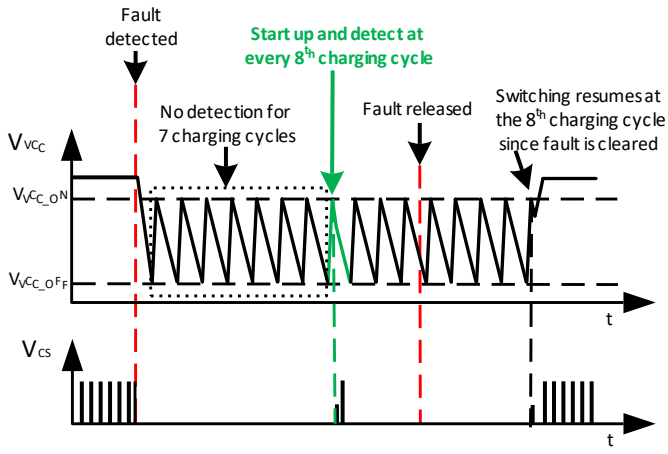

Figure 19 Extended cycle skip auto-restart

5 Schematic

A 14.5 W reference board schematic circuit with ICE5AR4780BZS-1 switching controller is shown in the following figure.

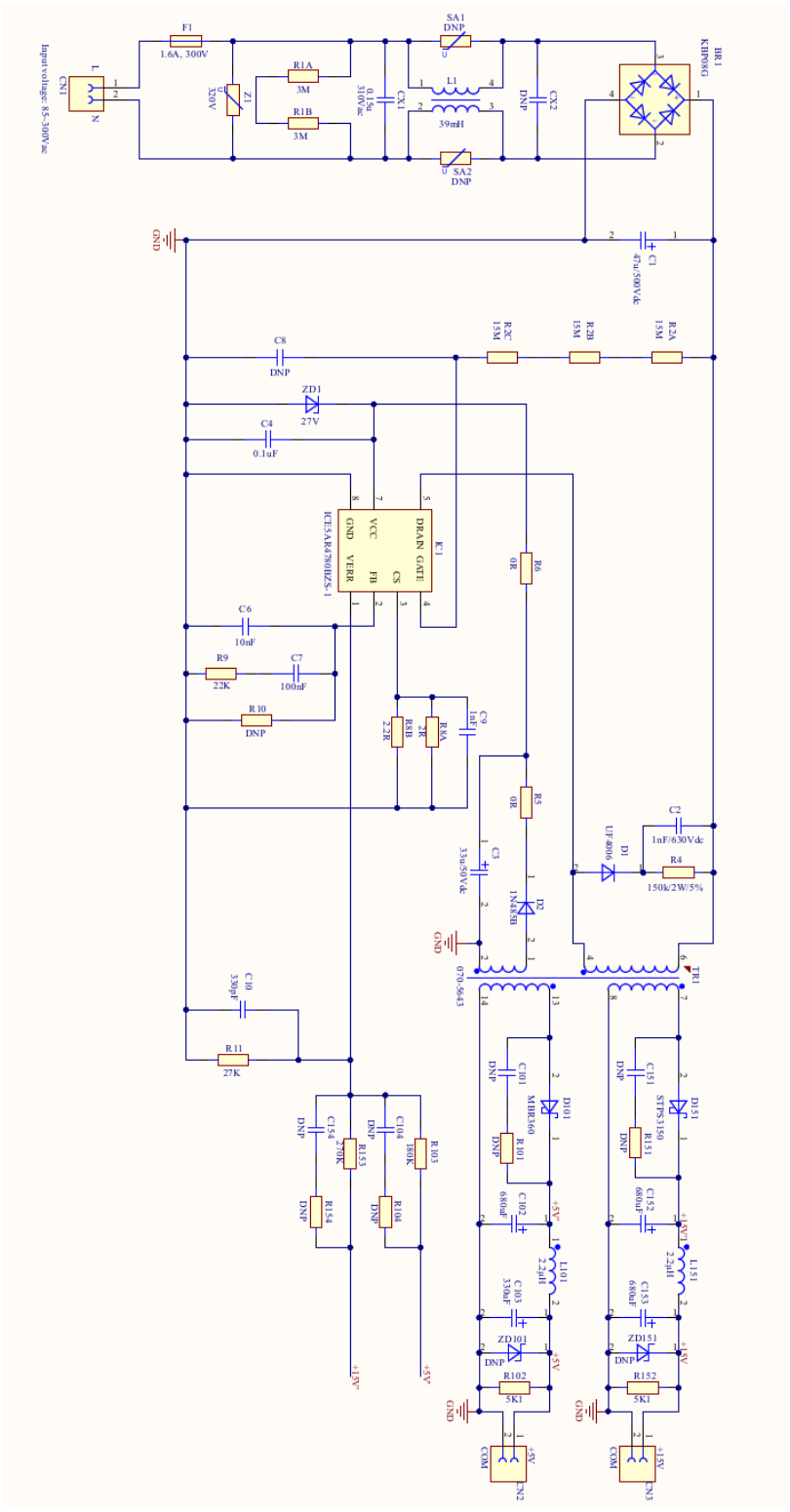

Figure 20 Schematic of REF_5AR4780BZS-1_14W1

6 PCB layout recommendation

In an SMPS, the PCB layout is crucial to a successful design. Recommendations (see Figure 20) are as follows:

1. Minimize the loop with pulse share current or voltage; examples are the loop formed by the bus voltage source, primary winding, main power switch (power switch CoolMOS™ power MOSFET inside the CoolSET™ switching controller), and CS resistor or the loop consisting of the secondary winding, output diode and output capacitor, or the loop of the V_{CC} power supply.
2. Star the ground at the bulk capacitor C1: Connect all primary grounds to the ground of the bulk capacitor C1 separately at one point. This can reduce the switching noise entering the sensitive pins of the CoolSET™ device. The primary star ground can be split into four groups as follows:

a) Combine signal (all small-signal grounds connecting to the controller/CoolSET™ GND pin such as the filter capacitor C4, C6, C8, C9, and optocoupler ground) and power ground (CS resistor R8A and R8B).

b) V_{CC} ground includes the V_{CC} capacitor C3 ground and the auxiliary winding ground, pin 2 of the power transformer.

c) EMI return ground includes the Y capacitor for isolated flyback application.

d) DC ground from the bridge rectifier BR1.

3. Place the filter capacitor close to the controller ground: Place the filter capacitors C4, C6, C8, and C9 as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.
4. HV trace clearance: Maintain HV traces sufficient spacing to the nearby traces. Otherwise, arcing can occur.

a) 400 V traces (positive rail of bulk capacitor C1) to nearby traces: greater than 2.0 mm.

b) 700/800 V traces (DRAIN pin of CoolSET™ IC1, see Figure 20) to nearby traces: greater than 3 mm.

5. Recommended minimum of 232 mm^2 copper area at the DRAIN pin to add to the PCB for better thermal performance of the CoolSET™ switching controller.

7 Output power of CoolSET™ 5th Generation Fixed Frequency Plus ICs

Table 4 Output power of CoolSET™ 5th Generation Fixed Frequency Plus controllers

Type	Package	Marking	V_{DS}	F_{sw}	R_{DSon}[3]	220 V AC ±20 percent[4] at DCM	85–300 V AC[2] at DCM	85–300 V AC[2] at CCM
ICE5AR4770BZS-1	PG-DIP-7	5AR4770BZS-1	700 V	100 kHz	4.73 Ω	26.5 W	14.5 W	16 W
ICE5AR4780BZS-1	PG-DIP-7	5AR4780BZS-1	800 V	100 kHz	4.13 Ω	27.5 W	15 W	16 W
ICE5BR4780BZ-1	PG-DIP-7	5BR4780BZ-1	800 V	65 kHz	4.13 Ω	27.5 W	15 W	16.5 W
ICE5AR3995BZ-1	PG-DIP-7	5AR3995BZ-1	950 V	100 kHz	3.46 Ω	30 W	16.5 W	18 W
ICE5BR3995BZ-1	PG-DIP-7	5BR3995BZ-1	950 V	65 kHz	3.46 Ω	30 W	16.5 W	18 W
ICE5BR2280BZ-1	PG-DIP-7	5BR2280BZ-1	800 V	65 kHz	2.13 Ω	40 W	22 W	24 W
ICE5AR0680BZS-1	PG-DIP-7	5AR0680BZS-1	800 V	100 kHz	0.71 Ω	66 W	39 W	41 W

The calculated output power curves showing typical output power against ambient temperature are shown in the following figure. The curves are derived based on an open-frame design at T_a = 50°C, T_J = 125°C (integrated HV MOSFET for CoolSET™), using the minimum pin copper area in a 2 oz. copper single-sided PCB and steady-state operation only (no design margins for abnormal operation modes are included). The output power figure is for selection purposes only. The actual power can vary depending on the specific design.

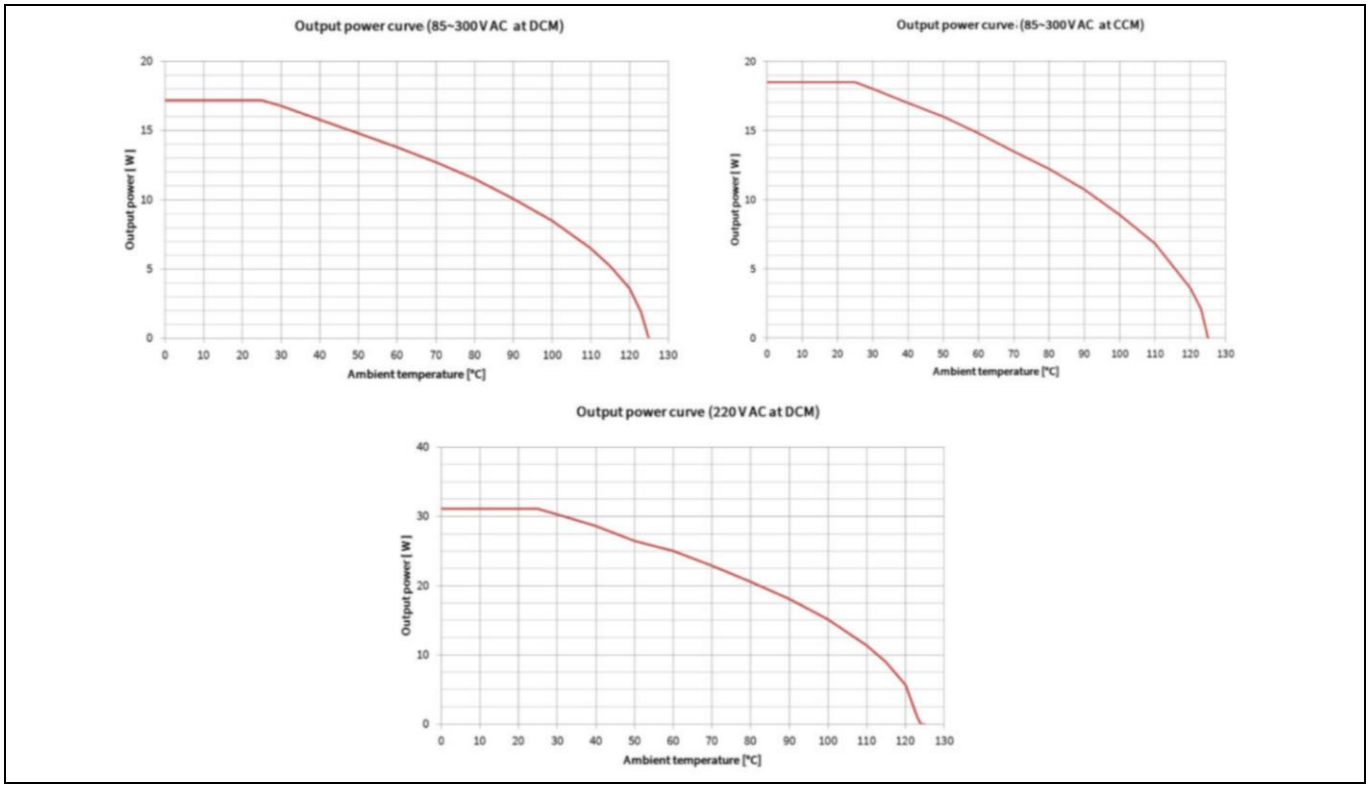

Figure 21 Output power curve of ICE5AR4770BZS-1 switching controller

[3] Typ. at T_J = 25°C (inclusive of low-side MOSFET).

[4] Calculated maximum output power rating in an open-frame design at T_a = 50°C, T_J = 125°C (integrated HV MOSFET) and using minimum drain pin copper area in a 2 oz. copper single-sided PCB. The output power figure is for selection purposes only. The actual power can vary depending on the particular design. Contact Technical support from Infineon for more information.

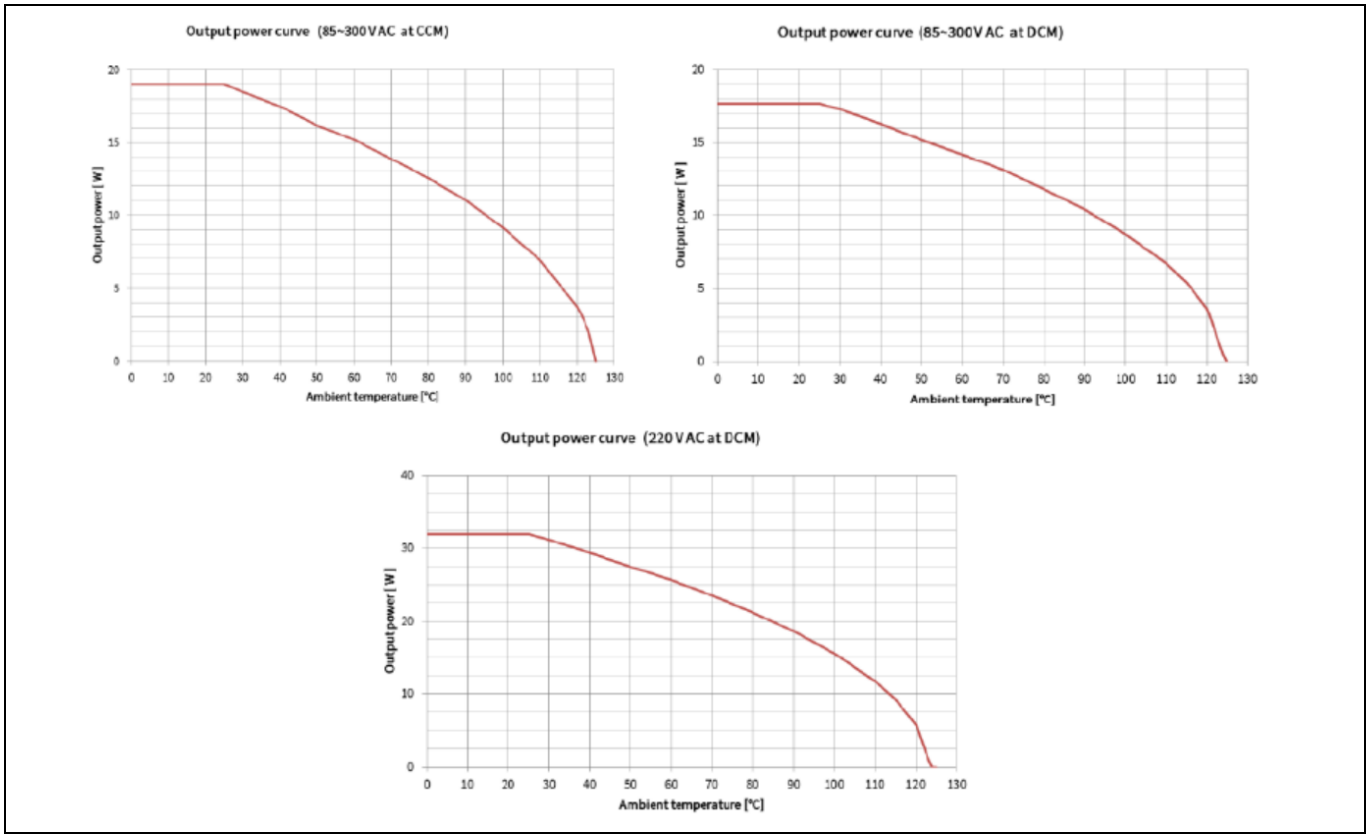

Figure 22 Output power curve of ICE5XR4780BZS-1 switching controller

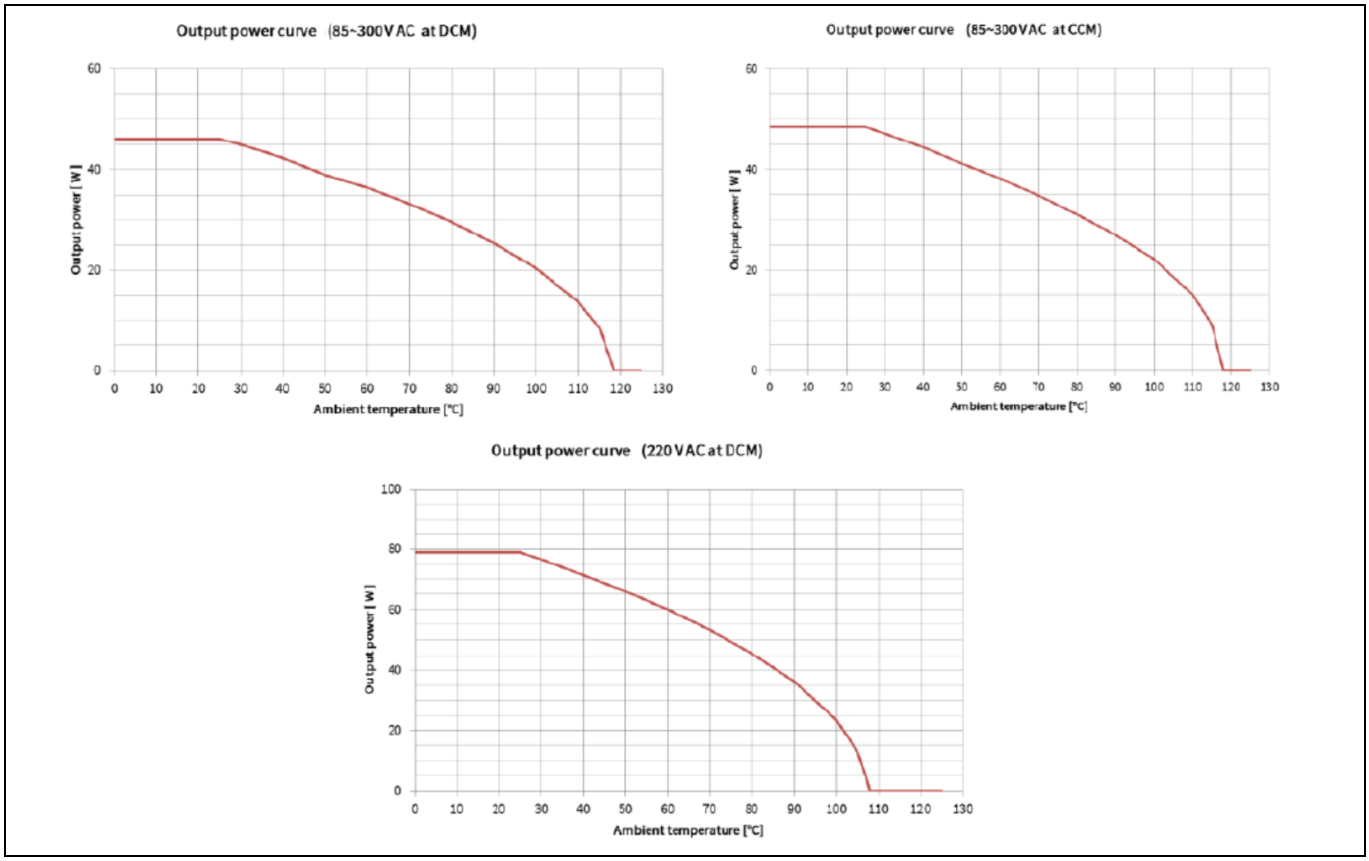

Figure 23 Output power curve of ICE5AR0680BZS-1 switching controller

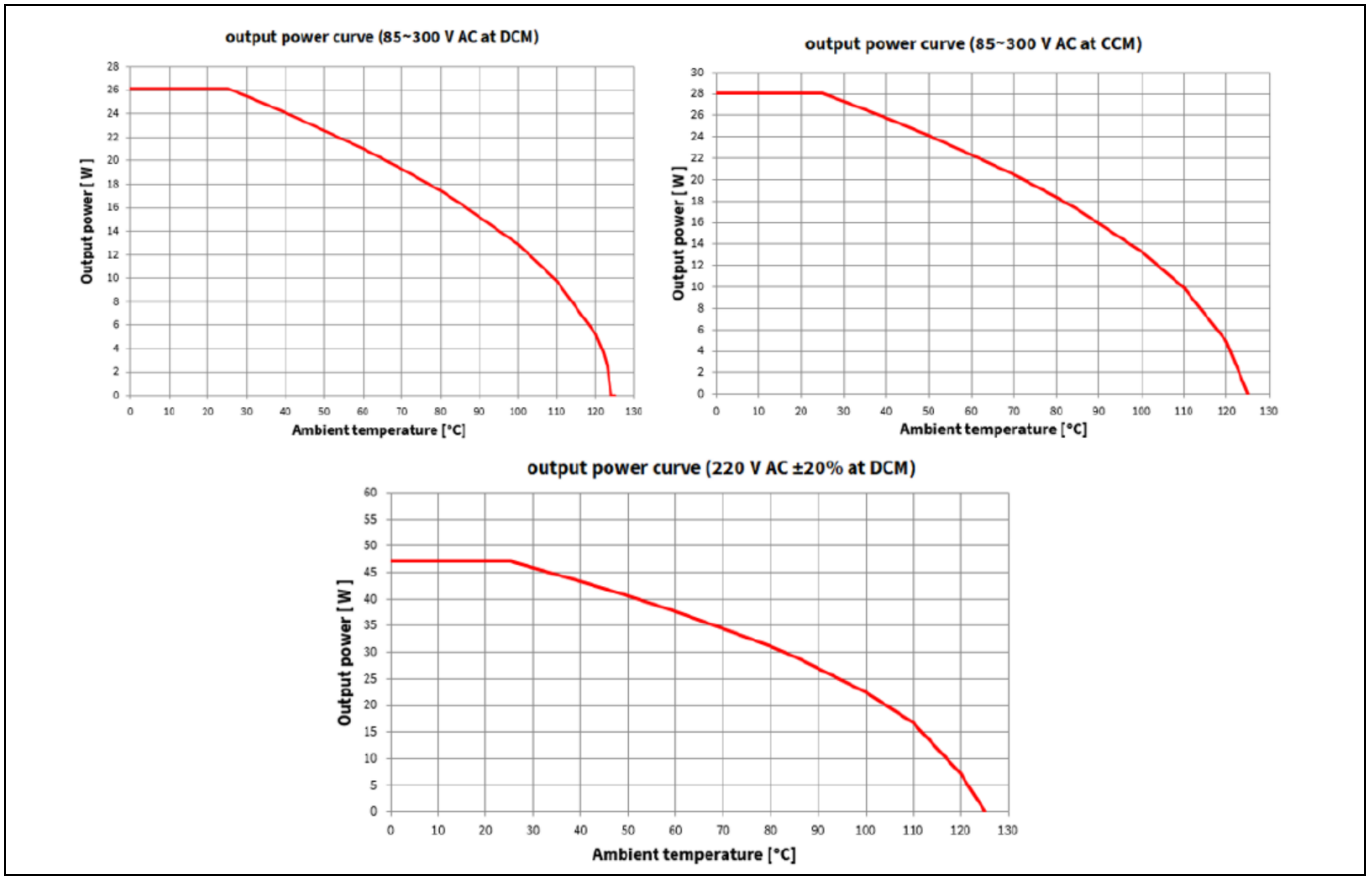

Figure 24 Output power curve of ICE5BR2280BZ-1 switching controller

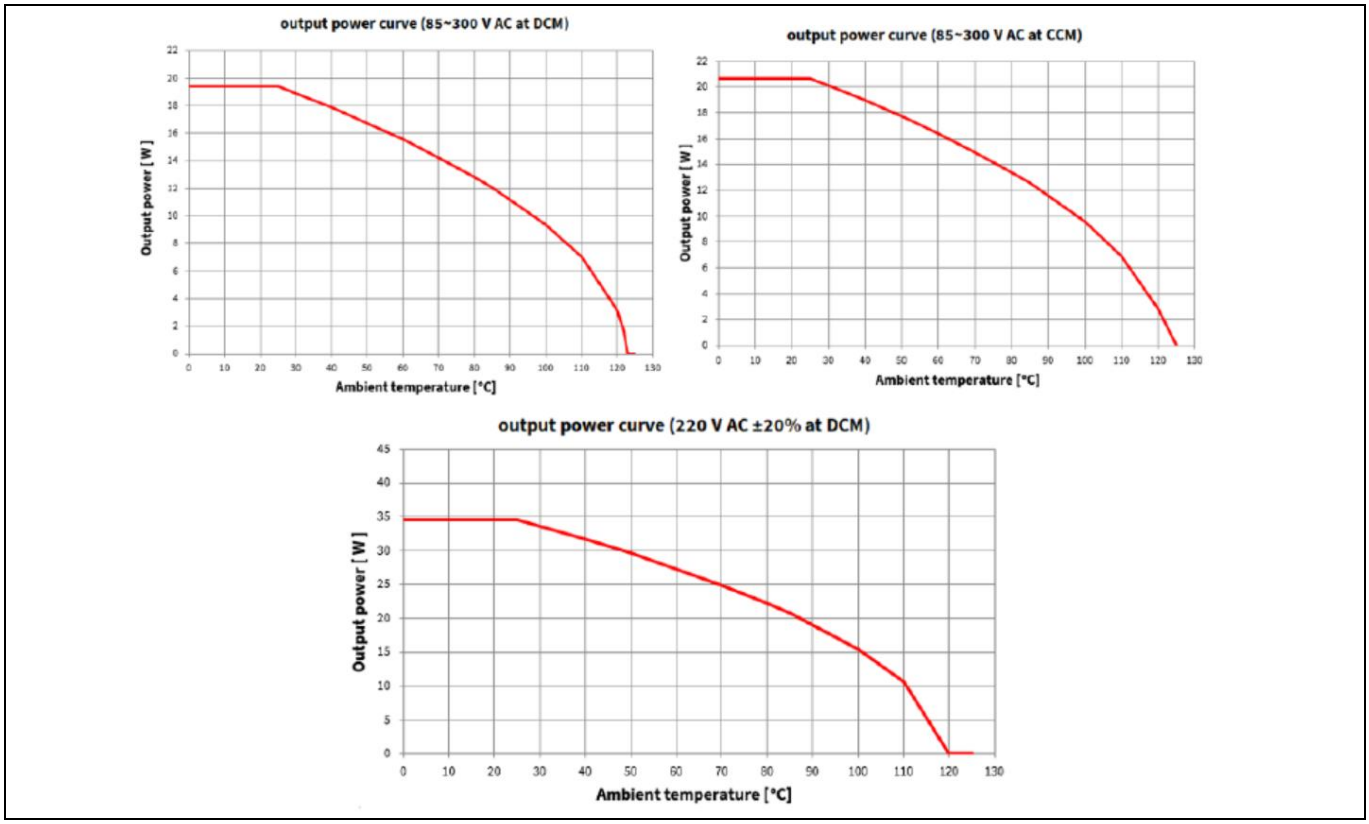

Figure 25 Output power curve of ICE5xR3995BZ-1 switching controller

8 CoolSET™ 5th Generation Fixed Frequency Plus fixed frequency FLYCAL design example

A design example of a 14.5 W, 15 V and 5 V fixed frequency non-isolated DCM flyback converter with ICE5AR4780BZS–1 is as follows:

Table 5 Parameters

Define input parameters	Symbol	Value	Unit
Minimum AC input voltage	V_{ACMin}	85	V AC
Maximum AC input voltage	V_{ACMax}	330	V AC
Line frequency	f_{AC}	60	Hz
Bulk capacitor DC ripple voltage	$V_{DCRipple}$	27	V
Output voltage 1	V_{Out1}	15	V
Output current 1	I_{Out1}	0.83	A
Forward voltage of output diode 2	V_{FOut1}	0.6	V
Output ripple voltage 1	$V_{OutRipple1}$	0.2	V
Output voltage 2	V_{Out2}	5	V
Output current 2	I_{Out2}	0.4	A
Forward voltage of output diode 2	V_{FOut2}	0.2	V
Output ripple voltage 2	$V_{OutRipple2}$	0.2	V
Maximum output power	P_{OutMax}	17	W
Minimum output power	P_{OutMin}	1	W
Efficiency at V_{ACMin} and P_{OutMax}	η	83	%
Reflection voltage	V_{RSET}	97.5	V
V_{CC} voltage	V_{Vcc}	14	V
Forward voltage of V_{CC} diode (D2)	V_{FVcc}	0.6	V
CoolSET™ 5th Generation Fixed Frequency Plus	CoolSET™	ICE5AR4780BZS-1	
Switching frequency	f_s	100	kHz
Breakdown voltage	V_{DSMax}	800	V
Drain-to-source capacitance of MOSFET (including $C_{o(er)}$ of MOSFET)	C_{DS}	7	pF
Effective output capacitance of MOSFET	$C_{O(er)}$	3	pF
Startup resistor $R_{StartUp}$ (R2A, R2B, R2C)	$R_{StartUp}$	45	MΩ
Maximum ambient temperature	T_a	50	°C

8.1 Pre-calculation

Output power of output 1:

$$P_{Out1} = V_{Out1} \cdot I_{Out1} \quad \Rightarrow \quad P_{Out1} = 15V \cdot 0.83A = 12.45W$$

Equation 15

Output power of output 2:

$$P_{Out2} = V_{Out2} \cdot I_{Out2} \quad \Rightarrow \quad P_{Out2} = 5V \cdot 0.4A = 2W$$

Equation 16

Nominal output power:

$$P_{OutNom} = P_{Out1} + P_{Out2} \quad \Rightarrow \quad P_{OutNom} = 12.45W + 2W = 14.45W$$

Equation 17

Output power 1 load weight:

$$K_{L1} = P_{Out1}/P_{OutNom} \quad \Rightarrow \quad K_{L1} = 12.45W/14.45W = 0.86$$

Equation 18

Output power 2 load weight:

$$K_{L2} = P_{Out2}/P_{OutNom} \quad \Rightarrow \quad K_{L1} = 2W/14.45W = 0.14$$

Equation 19

Maximum input power:

$$P_{InMax} = \frac{P_{OutMax}}{\eta} \quad \Rightarrow \quad P_{InMax} = \frac{17W}{0.83} = 20.48W$$

Equation 20

8.2 Input diode bridge (BR1)

Input RMS current:

Power factor	cosφ	0.6
$I_{ACRMS} = \frac{P_{InMax}}{V_{ACMin} \cdot \boldsymbol{cos}\,\phi}$	⇒	$I_{ACRMS} = \frac{20.48W}{85V \cdot 0.6} = 0.402A$

Equation 21 Input RMS current

Maximum DC input voltage:

$V_{DC\,\boldsymbol{max}\,PK} = V_{ACMax} \cdot \sqrt{2}$	⇒	$V_{DCMaxPk} = 330V \cdot \sqrt{2} = 466.7V$

Equation 22

8.3 Input capacitor (C1)

Peak voltage at minimum AC input:

$V_{DCMinPk} = V_{ACMin} \cdot \sqrt{2}$	⇒	$V_{DCMinPk} = 85V \cdot \sqrt{2} = 120.2V$

Equation 23

Minimum DC input voltage-based ripple voltage setting:

$V_{DCMinSet} = V_{DCMinPk} - V_{DC\rightleftarrows Ripple}$	⇒	$V_{DCMin}Set = 120.2V - 27V = 93.2V$

Equation 24

Discharging time at each half-line cycle:

$T_D = \frac{1}{4 \cdot f_{AC}} \cdot \left(1 + \frac{\boldsymbol{sin}^{-1}\frac{V_{DCMinSet}}{V_{DCMinPk}}}{90}\right)$	⇒	$T_D = \frac{1}{4 \cdot 60Hz} \cdot \left(1 + \frac{\boldsymbol{sin}^{-1}\frac{93.2V}{120.2V}}{90}\right) = 6.52ms$

Equation 25

Required energy at discharging time of input capacitor:

$W_{IN} = P_{INMax} \cdot T_D$	⇒	$W_{IN} = 20.48W \cdot 6.52ms = 0.13W \cdot s$

Equation 26

Calculated input capacitor:

$$C_{INCal} = \frac{2 \cdot W_{IN}}{V_{DCMinPk}^2 - V_{DCMinSet}^2} \quad \Rightarrow \quad C_{INCal} = \frac{2 \cdot 0.13W \cdot s}{(120.2V)^2 - (93.2V)^2} = 46.35\mu F$$

Equation 27

Alternatively, a thumb rule for estimating the input capacitor can be applied based on maximum input power, as follows:

Table 6 Input capacitor estimation

Input voltage	Factor
115 V AC	2 µF/W
230 V AC	1 µF/W
85–265 V AC	2–3 µF/W

Applying the thumb rule using the 2 µF/W factor:

$$C_{INEst} = P_{INMax} \cdot factor \quad \Rightarrow \quad C_{INEst} = 20.48 \cdot 2\mu = 41\mu F$$

Equation 28

Choose a capacitance greater than or equal to calculated (Equation 27) or estimated (Equation 28) value, whichever is greater. The voltage rating should be greater than or equal to the maximum DC input voltage.

Input capacitor	C_{IN}	47 µF/500 V

Recalculation after input capacitor selection:

$$V_{DCMin} = \sqrt{V_{DCMinPk}^2 - \frac{2 \cdot W_{IN}}{C_{IN}}} \quad \Rightarrow \quad V_{DCMin} = \sqrt{(120.2V)^2 - \frac{2 \cdot 0.13W \cdot s}{47\mu F}} = 93.63V$$

Equation 29

Note: Special requirements for hold-up time, including cycle skip/drop-out, or other factors that affect the resulting minimum DC input voltage and capacitor discharging time, are not considered above.

8.4 Transformer design (TR1)

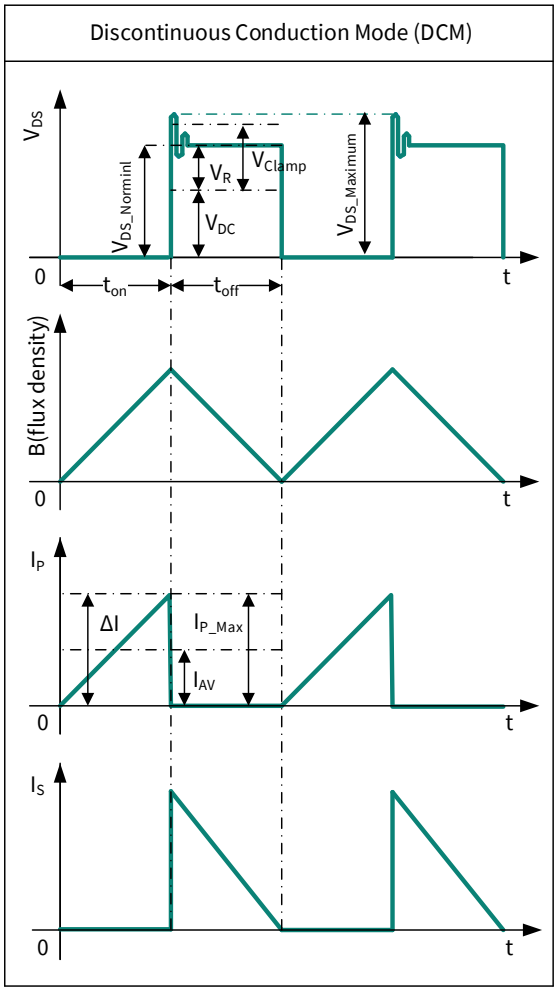

Figure 26 Typical waveforms of DCM operation

Maximum duty cycle:

$$D_{Max} = \frac{V_{RSET}}{V_{RSET}+V_{DCMin}} \quad \Rightarrow \quad D_{Max} = \frac{97.5V}{97.5V + 93.63V} = 0.51$$

Equation 30

Primary inductance:

$$L_P = \frac{(V_{DCMin}\times D_{Max})^2}{2\times P_{InMax}\times f_s \times K_{RF}} \quad \Rightarrow \quad L_P = \frac{(93.63V \times 0.51)^2}{2 \times 20.48W \times 100kHz \times 1} = 556.7\mu H$$

Equation 31

Primary average current during turn-on:

$$I_{AV} = \frac{P_{InMax}}{V_{DCMin} \times D_{Max}} \quad \Rightarrow \quad I_{AV} = \frac{20.48W}{93.63V \times 0.51} = 0.43A$$

Equation 32

Primary peak-to-peak current:

$$\Delta I = \frac{V_{DCMin} \times D_{Max}}{L_P \times f_s} \quad \Rightarrow \quad \Delta I = \frac{93.63V \times 0.51}{556.7\mu H \times 100kHz} = 0.86A$$

Equation 33

Primary peak current:

$$I_{PMax} = I_{AV} + \frac{\Delta I}{2} \quad \Rightarrow \quad I_{PMax} = 0.43A + \frac{0.86A}{2} = 0.86A$$

Equation 34

Primary valley current:

$$I_{Valley} = I_{PMax} - \Delta I \quad \Rightarrow \quad I_{Valley} = 0.86A - 0.86A = 0A$$

Equation 35

Primary RMS current:

$$I_{PRMS} = \sqrt{[3 \times (I_{AV})^2 + (\frac{\Delta I}{2})^2] \times \frac{Dmax}{3}} \quad \Rightarrow \quad I_{PRMS} = \sqrt{[3 \times (0.43)^2 + (\frac{0.86A}{2})^2] \times \frac{0.51}{3}} = 0.35A$$

Equation 36

Choose core type and bobbin from magnetic suppliers that can support the required power. Maximum flux density, typically from 200 mT to 400 mT, depends on the type of ferrite material. Select the following transformer material.

Table 7 Transformer material

Material	Value
Core type	E 20/10/6
Core material	N87
Maximum flux density (B_S)	390 mT at 100°C
Cross-sectional area (A_e)	32 mm²
Bobbin width (BW)	11 mm

Material	Value
Winding cross-section (A_N)	34 mm^2
Winding perimeter (l_N)	41.2 mm

Set maximum flux density	B_{MAX}	200 mT

Calculate minimum primary number of turns:

$N_{PCal} \geq \frac{I_{PMax} \cdot L_p}{B_{Max} \cdot A_e}$	⇒	$N_{PCal} \geq \frac{0.86A \times 556.7\mu H}{200mT \times 32mm^2} = 74.6Turns$
Primary number of turns	N_P	78 turns

Equation 37

Calculate secondary number of turns for V_{Out}:

$N_{S1Cal} = \frac{N_P \cdot (V_{Out1} + V_{FOut1})}{V_R}$	⇒	$N_{S1Cal} = \frac{78Turns \times (15V + 0.6V)}{97.5V} = 12.48Turns$
Secondary 1 number of turns	N_{S2}	12 turns

Equation 38

Calculate secondary number of turns for V_{Out}:

$N_{S2Cal} = \frac{N_P \cdot (V_{Out2} + V_{FOut2})}{V_R}$	⇒	$N_{S2Cal} = \frac{78Turns \times (5V + 0.2V)}{97.5V} = 4.16Turns$
Secondary 2 number of turns	N_{S2}	4 turns

Equation 39

Calculate number of turns for V_{CC}:

$N_{VccCal} = \frac{N_P \cdot (V_{Vcc} + V_{FVcc})}{V_R}$	⇒	$N_{VccCal} = \frac{78Turns \times (14V + 0.6V)}{97.5V} = 11.7Turns$
Auxiliary number of turns	N_{Vcc}	11 turns

Equation 40

Auxiliary supply voltage:

$$V_{VccCal} = (V_{Out1} + V_{FOut1}) \cdot N_{Vcc}/N_{S1} - V_{FVcc} \quad \Rightarrow \quad V_{VccCal} = (15V + 0.6V) \cdot 11/12 - 0.6V = 13.7V$$

Equation 41

8.5 Post calculation

Primary to secondary 1 turns ratio:

$$N_{PS1} = N_P/N_{S1} \quad \Rightarrow \quad N_{PS1} = 78turns/12turns = 6.5$$

Equation 42

Primary to secondary 2 turns ratio:

$$N_{PS2} = N_P/N_{S2} \quad \Rightarrow \quad N_{PS2} = 78turns/4turns = 19.5$$

Equation 43

Post-calculated reflected voltage:

$$V_{RPost} = (V_{Out1} + V_{FOut1}) \cdot N_P/N_{S1} \quad \Rightarrow \quad V_{RPost} = (15V + 0.6V) \cdot 78/12 = 101.4V$$

Equation 44

Post-calculated maximum duty cycle:

$$D_{MaxPost} = \frac{V_{RPost}}{V_{RPost}+V_{DCMin}} \quad \Rightarrow \quad D_{MaxPost} = \frac{101.4V}{101.4V + 93.63V} = 0.52$$

Equation 45

Duty cycle prime:

$$D'_{Max} = \frac{L_P \cdot f_s \cdot (I_{PMax} - I_{Valley})}{V_{RPost}} \quad \Rightarrow \quad D'_{Max} = \frac{556.7\mu H \cdot 100kHz \cdot (0.86A - 0A)}{101.4V} = 0.47$$

Equation 46

Actual flux density:

$$B_{MaxAct} = \frac{L_P \cdot I_{PMax}}{N_P \cdot A_e} \quad \Rightarrow \quad B_{MaxAct} = \frac{556.7\mu H \cdot 0.86A}{78 \cdot 32mm^2} = 191mT$$

Equation 47

Maximum DC input voltage for CCM operation:

$$V_{DC\,max\,CCM} = \left(\frac{1}{\sqrt{2 \cdot P_{InMax} \cdot L_P \cdot f_s}} - \frac{1}{V_{RPost}}\right)^{-1} \Rightarrow V_{DC\,max\,CCM} = \left(\frac{1}{\sqrt{2 \cdot 20.48W \cdot 557\mu H \cdot 100kHz}} - \frac{1}{101.4V}\right)^{-1} = 90.3V$$

Equation 48

8.6 Transformer winding design

Transformer design plays a significant role in efficiency. Interlacing primary and output windings can reduce leakage inductance, and this is one way to improve efficiency. It is also critical for safety concerns, especially in isolated applications. Therefore, consider creepage and clearance.

Standard safety margins between primary and secondary windings:

- M = 4 mm for European safety standard
- M = 3.2 mm for UL1950
- M = 0 mm for triple-insulated wire on either primary or secondary winding

Table 8 Safety margin

Safety margin	Symbol	Value
Standard safety margin	M	0 mm
Copper space factor	f_{Cu}	0.4 (0.2–0.4)

Effective bobbin width:

$$BW_E = BW - (2 \times M) \Rightarrow BW_E = 11mm - (2 \times 0) = 11mm$$

Equation 49

Effective winding cross-section:

$$A_{Ne} = \frac{A_N \times BW_e}{BW} \Rightarrow A_{Ne} = \frac{34mm^2 \times 11mm}{11mm} = 34mm^2$$

Equation 50

The effective winding cross-section must be divided between the primary and secondary windings. The design example is divided as follows:

Table 9 Effective winding

Winding	Symbol	Factor (%)
Primary winding	AF_{NP}	50
Secondary winding 1	AF_{NS1}	30
Secondary winding 2	AF_{NS2}	15
Auxiliary winding	AF_{NVcc}	5

8.6.1 Primary winding

Calculate copper wire cross-sectional area:

$$A_{PCal} = \frac{AF_{NP} \times f_{Cu} \times A_{Ne}}{N_P} \quad \Rightarrow \quad A_{PCal} = \frac{0.5 \times 0.4 \times 34mm^2}{78} = 0.087mm^2$$

Equation 51

Calculate maximum wire size:

$$AWG_{PCal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot log\left(2 \cdot \sqrt{\frac{A_{PCal}}{\pi}}\right)\right)\right) \quad \Rightarrow \quad AWG_{PCal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot log\left(2 \cdot \sqrt{\frac{0.087}{\pi}}\right)\right)\right) = 28$$

Selected wire size	AWG_P	30
Number of parallel wires	n_P	1

Equation 52

Copper wire diameter:

$$d_P = 10^{\left(\frac{1.8277}{2} - \frac{AWG_P}{2 \cdot 9.97}\right)} \quad \Rightarrow \quad d_P = 10^{\left(\frac{1.8277}{2} - \frac{30}{2 \cdot 9.97}\right)} = 0.26mm$$

Equation 53

Copper wire cross-sectional area:

$$A_P = \frac{\pi}{4} \cdot {d_P}^2 \cdot n_p \quad \Rightarrow \quad A_P = \frac{\pi}{4} \cdot (0.26mm)^2 \cdot 1 = 0.0517mm^2$$

Equation 54

Wire current density:

$$S_P = \frac{I_{PRMS}}{A_P} \quad \Rightarrow \quad S_P = \frac{0.35A}{0.052mm^2} = 6.8A/mm^2$$

Equation 55

Note: Recommended wire current density is less than 8 A/mm².

Number of turns per layer using INS = 0.01 mm:

$$NL_P = \frac{BW_E}{n_P \cdot (d_P + 2 \cdot INS)} \quad \Rightarrow \quad NL_P = \frac{11mm}{1 \cdot (0.26mm + 2 \cdot 0.01mm)} = 39Turns/layer$$

Equation 56

Note: Insulation thickness (INS) for single-, double-, and triple-insulated wire is 0.01, 0.02, and 0.04 mm respectively. Ask the magnetics supplier for the actual insulation thickness.

Number of layers:

$$Ln_P = N_p / NL_P \quad \Rightarrow \quad Ln_P = 78Turns/(39Turns/layer) = 2layers$$

Equation 57

8.6.2 Secondary 1 winding (V_{Out1})

Calculate copper wire cross-sectional area:

$$A_{NS1Cal} = \frac{AF_{NS1} \times f_{Cu} \times A_{Ne}}{N_{S1}} \quad \Rightarrow \quad A_{NS1Cal} = \frac{0.30 \times 0.4 \times 34mm^2}{12} = 0.34mm^2$$

Equation 58

Calculate maximum wire size:

$$AWG_{NS1Cal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot log\left(2 \cdot \sqrt{\frac{A_{NS1Cal}}{\pi}}\right)\right)\right) \quad \Rightarrow \quad AWG_{NS1Cal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot log\left(2 \cdot \sqrt{\frac{0.34mm^2}{\pi}}\right)\right)\right) = 22$$

Selected wire size	AWG_{S1}	26
Number of parallel wires	n_{S1}	2

Equation 59

Copper wire diameter:

$$d_{S1} = 10^{\left(\frac{1.8277}{2} - \frac{AWG_{S1}}{2 \cdot 9.97}\right)} \quad \Rightarrow \quad d_{S1} = 10^{\left(\frac{1.8277}{2} - \frac{26}{2 \cdot 9.97}\right)} = 0.407mm$$

Equation 60

Copper wire cross-sectional area:

$$A_{S1} = \frac{\pi}{4} \cdot {d_{S1}}^2 \cdot n_{S1} \quad \Rightarrow \quad A_{S1} = \frac{\pi}{4} \cdot (0.407)^2 \cdot 2 = 0.261mm^2$$

Equation 61

Peak current:

$$I_{S1Max} = I_{PMax} \cdot K_{L1} \cdot N_{PS1} \quad \Rightarrow \quad I_{S1Max} = 0.86A \cdot 0.86 \cdot 6.5 = 4.8A$$

Equation 62

RMS current:

$$I_{S1RMS} = I_{PRMS} \cdot K_{L1} \cdot \sqrt{\frac{1-D_{MaxPost}}{D_{MaxPost}}} \cdot N_{PS1} \quad \Rightarrow \quad I_{S1RMS} = 0.35A \cdot 0.86 \cdot \sqrt{\frac{1-0.52}{0.52}} \cdot 6.5 = 1.9A$$

Equation 63

Wire current density:

$$S_{S1} = \frac{I_{S1RMS}}{A_{S1}} \quad \Rightarrow \quad S_{S1} = \frac{1.9A}{0.261mm^2} = 7.3A/mm^2$$

Equation 64

Number of turns per layer using INS = 0.01 mm (non-isolated design does not need triple-insulated wire):

$$NL_{S1} = \left\lfloor \frac{BW_E}{nw_{S1} \cdot (d_{S1} + 2 \cdot INS_{S1})} \right\rfloor \quad \Rightarrow \quad NL_{S1} = \left\lfloor \frac{11mm}{2 \cdot (0.407mm + 2 \cdot 0.01mm)} \right\rfloor = 12Turns/layer$$

Equation 65

Number of layers of secondary 1 winding:

$$Ln_{S1} = \lceil N_{S1}/NL_{S1} \rceil \quad \Rightarrow \quad Ln_{S1} = \lceil 12Turns/(12Turns/layer) \rceil = 1layers$$

Equation 66

8.6.3 Secondary 2 winding (V_{Out2})

Calculate copper wire cross-sectional area:

$$A_{NS2Cal} = \frac{AF_{NS2} \times f_{Cu} \times A_{Ne}}{N_{S2}} \quad \Rightarrow \quad A_{NS2Cal} = \frac{0.15 \times 0.4 \times 34mm^2}{4} = 0.51mm^2$$

Equation 67

Calculate maximum wire size:

$$AWG_{NS2Cal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot log\left(2 \cdot \sqrt{\frac{A_{NS2Cal}}{\pi}}\right)\right)\right) \quad \Rightarrow \quad AWG_{NS2Cal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot log\left(2 \cdot \sqrt{\frac{0.34}{\pi}}\right)\right)\right) = 20$$

Selected wire size	AWG_{S2}	26
Number of parallel wires	n_{S2}	26

Equation 68

Copper wire diameter:

$$d_{S2} = 10^{\left(\frac{1.8277}{2} - \frac{AWG_{S2}}{2 \cdot 9.97}\right)} \quad \Rightarrow \quad d_{S2} = 10^{\left(\frac{1.8277}{2} - \frac{26}{2 \cdot 9.97}\right)} = 0.407mm$$

Equation 69

Copper wire area:

$$A_{S2} = \frac{\pi}{4} \cdot {d_{S2}}^2 \cdot n_{S2} \quad \Rightarrow \quad A_{S2} = \frac{\pi}{4} \cdot (0.407)^2 \cdot 1 = 0.13mm^2$$

Equation 70

Peak current:

$$I_{S2Max} = I_{PMax} \cdot K_{L2} \cdot N_{PS2} \quad \Rightarrow \quad I_{S2Max} = 0.86A \cdot 0.14 \cdot 19.5 = 2.3A$$

Equation 71

RMS current:

$$I_{S2RMS} = I_{PRMS} \cdot K_{L2} \cdot \sqrt{\frac{1-D_{MaxPost}}{D_{MaxPost}}} \cdot N_{PS2} \quad \Rightarrow \quad I_{S2RMS} = 0.35A \cdot 0.14 \cdot \sqrt{\frac{1-0.52}{0.52}} \cdot 19.5 = 0.9A$$

Equation 72

Wire current density:

$$S_{S2} = \frac{I_{S2RMS}}{A_{S2}} \quad \Rightarrow \quad S_{S2} = \frac{0.9A}{0.130mm^2} = 7A/mm^2$$

Equation 73

Number of turns per layer using INS = 0.01 mm (non-isolated design does not need triple-insulated wire):

$$NL_{S2} = \left\lfloor \frac{BW_E}{nw_{S2} \cdot (d_{S2} + 2 \cdot INS_{S2})} \right\rfloor \quad \Rightarrow \quad NL_{S2} = \left\lfloor \frac{11mm}{1 \cdot (0.407mm + 2 \cdot 0.01mm)} \right\rfloor = 25Turns/layer$$

Equation 74

Number of layers:

$$Ln_{S2} = \lceil N_{S2}/NL_{S2} \rceil \quad \Rightarrow \quad Ln_{S2} = \lceil 4Turns/25Turns/layer \rceil = 1layer$$

Equation 75

8.7 Clamping network

For calculating the clamping network, it is required to know the leakage inductance L_{LK}. The most common approach is to have the L_{LK} value given in a percentage of the L_p. If it is known that the transformer construction is consistent, the L_{LK} can be measured by shorting the secondary windings (assuming the availability of a good LCR meter).

Leakage inductance:

Leakage inductance percentage	$L_{LK\%}$	2 percent
$L_{LK} = L_{LK\%} \cdot L_P$	$\Rightarrow$	$L_{LK} = 2\% \times 556.7\mu H = 11\mu H$

Equation 76

Clamping voltage:

Clamping voltage	⇒	$V_{Clamp} = 800V - 466.7V - 101.4V = 231.9V$
		$V_{Clamp} = 200V$

Equation 77

Calculate clamping resistor:

$R_{Clamp} = \frac{(V_{Clamp}+V_{Rpost})*V_{Clamp}}{0.5*L_{LK}*I_{Pmax}^2*f_s}$	⇒	$R_{Clamp} = \frac{(200 + 101.4) * 200}{0.5 \times 11\mu H \times (0.86A)^2 \times 100kHz} = 150k\Omega$
Clamping resistor	R_{Clamp}	150 kΩ

Equation 78

Assuming 10% ripple for snubber voltage:

$C_{ClampCal} = \frac{V_{Clamp}+V_{Rpost}}{(Ripple*R_{Clamp})\cdot f_s}$	⇒	$C_{ClampCal} = \frac{200V + 101.4}{(20V * 150k\Omega) \times 100kHz} = 1nF$
Clamping capacitor	C_{Clamp}	1 nF

Equation 79

8.8 CS resistor

The CS resistor value defines the peak current of the power MOSFET. Therefore, design the transformer not to saturate at this peak current value. Because the IC cycle-by-cycle PCL is defined by this resistor and it also defines the maximum output power that can be delivered.

PCL threshold	V_{CS_N}	0.8 V
$R_{Sense} = \frac{V_{CS_N}}{I_{PMax}}$	⇒	$R_{Sense} = \frac{0.8V}{0.86A} = 0.93\Omega$
Current sense resistor selected	R8A, R8B	2 Ω, 2.2 Ω (fine-tuned bench values)

Equation 80 CS resistor

8.9 Output rectifier

A low forward voltage and an ultrafast diode such as a Schottky diode are recommended for a highly efficient design. These diodes are subjected to large peak and RMS current stress. The minimum voltage rating (not including voltage spikes) and minimum current rating (not including peak power transients) are calculated in the following sections.

The output capacitor is required to minimize the output ripple. It also holds the necessary energy needed during high-load jumps. Therefore, the output capacitor must have enough capacitance and low ESR. It should also meet the ripple current rating.

An LC filter can be added to further reduce the output ripple.

8.9.1 Output 1

Diode reverse voltage and RMS current:

$V_{RDiode1} = V_{Out1} + \left(\frac{V_{DCMaxPK}}{N_{PS1}}\right)$	⇒	$V_{RDiode1} = 15V + \left(\frac{466.7V}{6.5}\right) = 86.8V$
Diode RMS current	I_{S1RMS}	1.9 A

Equation 81

Output capacitor ripple current:

Maximum voltage undershoot	ΔV_{Out}	0.3 V
Number of clock periods	n_{CP1}	20
$I_{Ripple1} = \sqrt{(I_{S1RMS})^2 - (I_{Out1})^2}$	⇒	$I_{Ripple1} = \sqrt{(1.9A)^2 - (0.83A)^2} = 1.71A$

Equation 82

Calculated output capacitance:

$C_{Out1Cal} = \frac{I_{Out1} \cdot n_{CP1}}{\Delta V_{OUT1} \cdot f_S}$	⇒	$C_{Out1Cal} = \frac{0.83A \cdot 20}{0.3V \cdot 100kHz} = 553\mu F$
Output capacitor	C_{Out1}	680 µF
ESR	R_{ESR1}	32 mΩ
Number of output capacitors in parallel	nc_{COut1}	1

Equation 83

Zero-frequency output capacitor:

$$f_{ZCOut1} = \frac{1}{2 \cdot \pi \cdot R_{ESR1} \cdot C_{Out1}} \quad \Rightarrow \quad f_{ZCOut1} = \frac{1}{2 \cdot \pi \cdot 32m\Omega \cdot 680\mu F} = 7.3kHz$$

Equation 84

Ripple voltage of first stage:

$$V_{Ripple1} = \frac{I_{S1Max} \cdot R_{ESR1}}{nc_{Cout1}} \quad \Rightarrow \quad V_{Ripple1} = \frac{4.8A \cdot 32m\Omega}{1} = 0.15V$$

Equation 85

Calculated LC filter capacitor:

Select LC filter inductor	L_{Out1}	2.2 µH
$C_{LCCal1} = \frac{(C_{Out1} \cdot R_{ESR1})^2}{L_{out1}}$ ⇒ $C_{LCCal1} = \frac{(680\mu F \cdot 32m\Omega)^2}{2.2\mu H} = 215\mu F$		
LC filter capacitor	C_{LC1}	680 µF

Equation 86

LC filter frequency:

$$f_{LC1} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_{LC1} \cdot L_{OUT1}}} \quad \Rightarrow \quad f_{LC1} = \frac{1}{2 \cdot \pi \cdot \sqrt{680\mu F \cdot 2.2\mu H}} = 4.1kHz$$

Equation 87

Second stage ripple voltage:

$$V_{2ndRipple1} = V_{Ripple1} \cdot \frac{\frac{1}{2 \cdot \pi \cdot f_S \cdot C_{LC1}}}{\frac{1}{2 \cdot \pi \cdot f_S \cdot C_{LC1}} + (2 \cdot \pi \cdot f_S \cdot L_{OUT1})} \quad \Rightarrow \quad V_{2ndRipple1} = 0.15V \cdot \frac{\frac{1}{2 \cdot \pi \cdot 100kHz \cdot 680\mu F}}{\frac{1}{2 \cdot \pi \cdot 100kHz \cdot 680\mu F} + (2 \cdot \pi \cdot 100kHz \cdot 2.2\mu H)} = 0.26mV$$

Equation 88

8.9.2 Output 2

Diode reverse voltage and RMS current:

$V_{RDiode2} = V_{Out2} + \left(\frac{V_{DCMaxPk}}{N_{PS2}}\right)$	⇒	$V_{RDiode2} = 5V + \left(\frac{466.7V}{19.5}\right) = 28.9V$
Diode RMS current	I_{S2RMS}	0.92 A

Equation 89

Output capacitor ripple current for V_{Out2}:

Maximum voltage undershoot (V_{Out2})	ΔV_{Out}	0.15 V
Number of clock periods	n_{CP2}	20
$I_{Ripple2} = \sqrt{(I_{S2RMS})^2 - (I_{Out2})^2}$	⇒	$I_{Ripple2} = \sqrt{(0.92A)^2 - (0.4A)^2} = 0.83A$

Equation 90

Calculated output capacitance:

$C102 = \frac{I_{Out2} \cdot n_{CP2}}{\Delta V_{OUT2} \cdot f_S}$	⇒	$C102 = \frac{0.4A \cdot 20}{0.15V \cdot 100kHz} = 533\mu F$
Output capacitor	C102	680 µF
ESR	R_{ESR2}	32 mΩ
Number of output capacitors in parallel	nc_{COut2}	1

Equation 91

Zero-frequency output capacitor:

$f_{ZCOut2} = \frac{1}{2 \cdot \pi \cdot R_{ESR2} \cdot C102}$	⇒	$f_{ZCOut2} = \frac{1}{2 \cdot \pi \cdot 32m\Omega \cdot 680\mu F} = 7.3kHz$

Equation 92

Ripple voltage of first stage:

$$V_{Ripple2} = \frac{I_{S2Max} \cdot R_{ESR2}}{nC102} \quad \Rightarrow \quad V_{Ripple2} = \frac{2.31A \cdot 32m\Omega}{1} = 0.07V$$

Equation 93

Calculated LC filter capacitor:

Select LC filter inductor	L101	2.2 µH
$C_{LCCal2} = \frac{(C102 \cdot R_{ESR2})^2}{L101}$ ⇒		$C_{LCCal2} = \frac{(680\mu F \cdot 32m\Omega)^2}{2.2\mu H} = 215\mu F$
LC filter capacitor	C103	330 µF

Equation 94

LC filter frequency:

$$f_{LC2} = \frac{1}{2 \cdot \pi \cdot \sqrt{C103 \cdot L101}} \quad \Rightarrow \quad f_{LC2} = \frac{1}{2 \cdot \pi \cdot \sqrt{330\mu F \cdot 2.2\mu H}} = 5.9kHz$$

Equation 95

Second stage ripple voltage:

$$V_{2ndRipple2} = V_{Ripple2} \cdot \frac{\frac{1}{2 \cdot \pi \cdot f_S \cdot C103}}{\frac{1}{2 \cdot \pi \cdot f_S \cdot C103} + (2 \cdot \pi \cdot f_S \cdot L101)} \quad \Rightarrow \quad V_{2ndRipple2} = 0.07V \cdot \frac{\frac{1}{2 \cdot \pi \cdot 100kHz \cdot 330\mu F}}{\frac{1}{2 \cdot \pi \cdot 100kHz \cdot 330\mu F} + (2 \cdot \pi \cdot 100kHz \cdot 2.2\mu H)} = 0.26mV$$

Equation 96

8.10 V_{CC} diode and capacitor

Auxiliary diode reverse voltage:

$$V_{RDiodeVCC} = V_{VccCal} + \left(V_{DCMaxPk} \cdot \frac{N_{Vcc}}{N_P}\right) \quad \Rightarrow \quad V_{RDiodeVCC} = 13.7V + \left(466.7 \times \frac{11}{78}\right) = 79.5V$$

Equation 97

Calculate minimum V_{CC} capacitor:

Soft start time from datasheet	t_{SS}	12 ms
$I_{VCC_Normal2}$ from datasheet	$I_{VCC_Normal2}$	2.2 mA
V_{VCC_ON} from datasheet	V_{VCC_ON}	16 V
V_{VCC_OFF} from datasheet	V_{VCC_OFF}	10 V
Selected V_{CC} capacitor	C_{VCC}	33 µF
$C_{Vcc} > \frac{I_{VCC_normal2} \times t_{ss}}{V_{VCC_ON} - V_{VCC_OFF}}$	⇒	$C_{Vcc} > \frac{2.2\,mA \cdot 12\,ms}{16V\ -10V} = 4.4\,\mu F$

Equation 98

Startup time:

V_{CC} short threshold from datasheet	V_{VCC_SCP}	1.1 V
$I_{VCC_Charge1}$ from datasheet	$I_{VCC_Charge1}$	0.2 mA
$t_{StartUp} = \frac{V_{VCC_SCP} \cdot C_{VCC}}{I_{VCC_Charge1}} + \frac{(V_{VCC_ON} - V_{VCC_SCP}) \cdot C_{VCC}}{I_{VCC_Charge3}}$	⇒	$t_{StartUp} = \frac{1.1V \cdot 22\mu F}{0.2mA} + \frac{(16V - 1.1V) \cdot 33\mu F}{3mA} = 345ms$

Equation 99

8.11 Calculation of losses

Input diode bridge loss:

Diode bridge forward voltage	V_{FBR}	1 V
$P_{DIN} = I_{ACRMS} \cdot V_{FBR} \cdot 2$	⇒	$P_{DIN} = 0.4A \cdot 0.7V \cdot 2 = 0.56W$

Equation 100

Transformer copper loss:

Copper resistivity at 100°C	ρ_{100}	0.0172 Ω·mm²/m

$$R_{PCu} = \frac{l_N \cdot N_P \cdot \rho_{100}}{A_P} \quad \Rightarrow \quad R_{PCu} = \frac{41.2mm \cdot 78 \cdot 0.0172\Omega \cdot mm^2/m}{0.052mm^2} = 1068.5m\Omega$$

Equation 101

$$R_{S1Cu} = \frac{l_N \cdot N_{S1} \cdot \rho_{100}}{A_{S1}} \quad \Rightarrow \quad R_{S1Cu} = \frac{41.2mm \cdot 12 \cdot 0.0172\Omega \cdot mm^2/m}{0.2602mm^2} = 32.6m\Omega$$

Equation 102

$$R_{S2Cu} = \frac{l_N \cdot N_{S2} \cdot \rho_{100}}{A_{S2}} \quad \Rightarrow \quad R_{S1Cu} = \frac{41.2mm \cdot 4 \cdot 0.0172\Omega \cdot mm^2/m}{0.13mm^2} = 21.8m\Omega$$

Equation 103

$$P_{PCu} = {I_{PRMS}}^2 \cdot R_{PCU} \quad \Rightarrow \quad P_{PCu} = (0.35A)^2 \cdot 1068.5m\Omega = 133.63mW$$

Equation 104

$$P_{S1Cu} = {I_{S1RMS}}^2 \cdot R_{S1CU} \quad \Rightarrow \quad P_{S1Cu} = (1.9A)^2 \cdot 32.6m\Omega = 118mW$$

Equation 105

$$P_{S2Cu} = {I_{S2RMS}}^2 \cdot R_{S2CU} \quad \Rightarrow \quad P_{S2Cu} = (0.92A)^2 \cdot 21.8m\Omega = 18mW$$

Equation 106

$$P_{Cu} = P_{PCu} \cdot P_{S1CU} \cdot P_{S2Cu} \quad \Rightarrow \quad P_{Cu} = 133mW + 118mW + 18mW = 270mW$$

Equation 107

Output rectifier diode loss:

$$P_{Diode1} = I_{S1RMS} \cdot V_{FOut1} \quad \Rightarrow \quad P_{Diode1} = 1.9A \cdot 0.6V = 1.14W$$

Equation 108

Output rectifier diode loss:

$$P_{Diode2} = I_{S2RMS} \cdot V_{FOut2} \quad \Rightarrow \quad P_{Diode2} = 0.92A \cdot 0.2V = 0.18W$$

Equation 109

RCD clamper loss:

$$P_{Clamper} = \frac{1}{2} \cdot L_{LK} \cdot I_{PMax}^2 \cdot f_S \cdot \frac{V_{Clamp}+V_{RPost}}{V_{Clamp}} \quad \Rightarrow \quad P_{Clamper} = \frac{1}{2} \cdot 11\mu H \cdot (0.86A)^2 \cdot 100kHz. \cdot \frac{200V + 101.4V}{200V} = 0.61W$$

Equation 110

CS resistor loss:

$$P_{CS} = (I_{PRMS})^2 \cdot R_{CS} \quad \Rightarrow \quad P_{CS} = (0.35A)^2 \cdot 1.04\Omega = 0.127W$$

Equation 111

MOSFET loss:

$R_{DS(on)}$ at T_J = 125°C from datasheet	$R_{DS(on)}$	8.69 Ω
$C_{o(er)}$ from datasheet	$C_{o(er)}$	3 pF
External drain-to-source capacitance	C_{DS}	0 pF

$$P_{SONMinAC} = \frac{1}{2} \cdot (C_{o(er)} + C_{DS}) \cdot (V_{DCMin} + V_{RPost})^2 \cdot f_S \quad \Rightarrow \quad P_{SONMinAC} = \frac{1}{2} \cdot (3pF + 0pF) \cdot (93.6V + 101.4V)^2 \cdot 100kHz = 5.7mW$$

Equation 112

$$P_{condMinAC} = {I_{PRMS}}^2 \cdot R_{DSON} \quad \Rightarrow \quad P_{condMinAC} = (0.35A)^2 \cdot 8.69\Omega = 1.087W$$

Equation 113

$$P_{MOSMinAC} = P_{SONMinAC} + P_{condMinAC} \quad \Rightarrow \quad P_{MOSMinAC} = 5.7mW + 1.087W = 1.093W$$

Equation 114

$$P_{SONMaxAC} = \frac{1}{2} \cdot (C_{o(er)} + C_{DS}) \cdot (V_{DCMaxPk} + V_{RPost})^2 \cdot f_S \quad \Rightarrow \quad P_{SONMaxAC} = \frac{1}{2} \cdot (3pF + 0pF) \cdot (466.7V + 101.4V)^2 \cdot 100kHz = 48.4mW$$

Equation 115

$$P_{condMaxAC} = \frac{1}{3} \cdot R_{DSON} \cdot I_{PMax}^2 \cdot \left(\frac{L_P \cdot I_{PMax} \cdot f_S}{V_{DCMaxPk}}\right) \quad \Rightarrow \quad P_{condMaxAC} = \frac{1}{3} \cdot 8.69\Omega \cdot (0.86A)^2 \cdot \left(\frac{557\mu H \cdot 0.86A \cdot 100kHz}{466.7V}\right) = 0.22W$$

Equation 116

$$P_{MOSMaxAC} = P_{SONMaxAC} + P_{condMaxAC} \quad \Rightarrow \quad P_{MOSMaxAC} = 48.4mW + 0.22W = 0.27W$$

Equation 117

Controller loss:

Controller current consumption	$I_{VCC_Norma2l}$	2.2 mA

$$P_{Ctrl} = V_{VCCCal} \cdot I_{VCC_Normal2} \quad \Rightarrow \quad P_{Ctrl} = 13.7V * 2.2mA = 30.14mW$$

Equation 118

Total power loss:

$$P_{losses} = P_{DIN} + P_{Cu} + P_{Diode1} + P_{Diode2} + P_{Clamper} + P_{CS} + P_{MOS} + P_{Ctrl} \quad \Rightarrow \quad P_{losses} = 0.56 + 0.27 + 1.14 + 0.18 + 0.61 + 0.30 + 1.1 + 0.01 = 4.17W$$

Equation 119

Efficiency after losses at 50°C ambient temperature:

$$\eta_{Post} = P_{OutMax}/(P_{OutMax} + P_{losses}) \quad \Rightarrow \quad \eta_{Post} = 17W/(17W + 4.17W) = 80.3\%$$

Equation 120

8.12 CoolSET™/MOSFET temperature

CoolSET™/MOSFET temperature:

$$\Delta T = R_{thJA_As} \cdot P_{MOS} \quad \Rightarrow \quad \Delta T = 65K/W \cdot 1.093W = 71°K$$

Equation 121

Assumed junction-to-ambient thermal impedance (include copper pour)	R_{thJA_As}	65 K/W
$T_{jmax} = \Delta T + T_{amax}$	⇒	$T_{jmax} = 71 + 50 = 121℃$

Equation 122

8.13 Output regulation (non-isolated)

Setting resistor dividers for two non-isolated outputs:

Error amplifier reference voltage	V_{ERR_REF}	1.8 V
Weighted regulation factor of V_{Out1}	W_1	73 percent
Select voltage divider R11		27 kΩ
$R153 = \frac{V_{Out1} - V_{ERR_REF}}{W_1 \cdot V_{ERR_REF}/R11}$	⇒	$R_{O2Cal} = \frac{15V - 1.8V}{73\% \cdot 1.8V/27k\Omega} = 271k\Omega$
Select voltage divider R153	R153	270 kΩ

Equation 123

Setting resistor dividers for two non-isolated outputs:

$R103 = \frac{V_{Out2} - V_{ERR_REF}}{\frac{V_{ERR_REF}}{R11} - \frac{V_{Out1} - V_{ERR_REF}}{R153}}$	⇒	$R103 = \frac{5V - 1.8V}{\frac{1.8V}{27k\Omega} - \frac{15V - 1.8V}{270k\Omega}} = 180k\Omega$
Select voltage divider R_{103}	R103	180 kΩ

Equation 124

References

[1] Infineon Technologies AG: *ICE5ARxxxxBZx-1 datasheet*; Available online

[2] Infineon Technologies AG: *Application note for REF_5AR4780BZS-1_14W1*; Available online

[3] Infineon Technologies AG*: CoolSET™ 5th Generation Plus Calculation tool for Fixed Frequency flyback*; Available online

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Revision history

Document revision	Date	Description of changes
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