

HW-Z1-ZCU104 Evaluation Board

(XCZU7EV-2FFVC1156)

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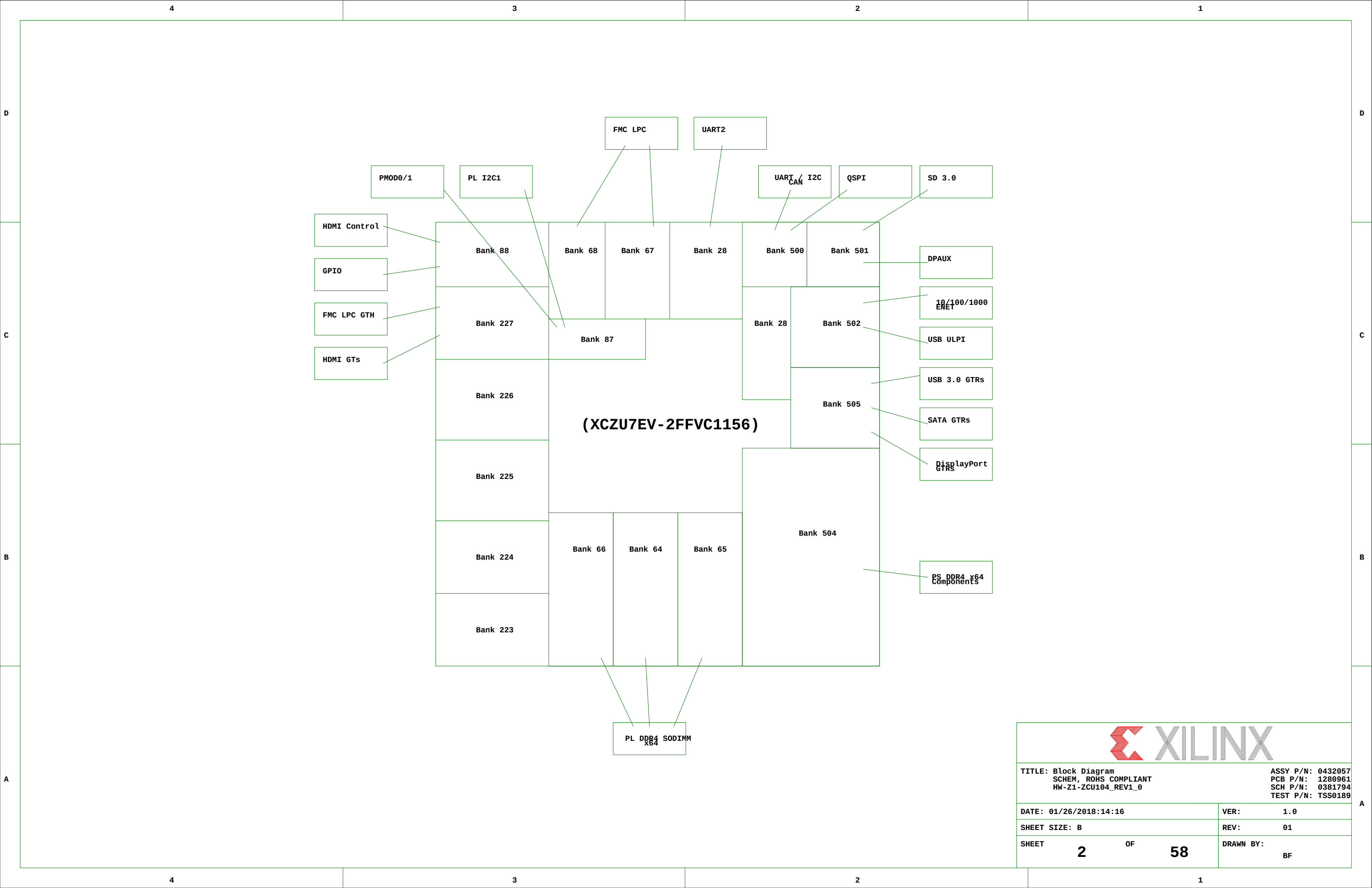
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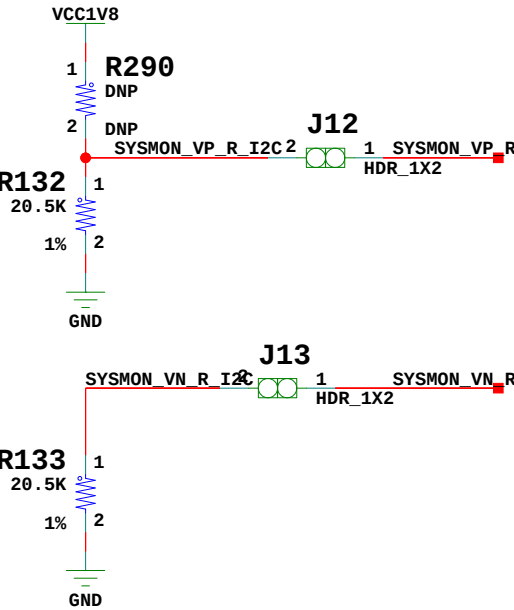
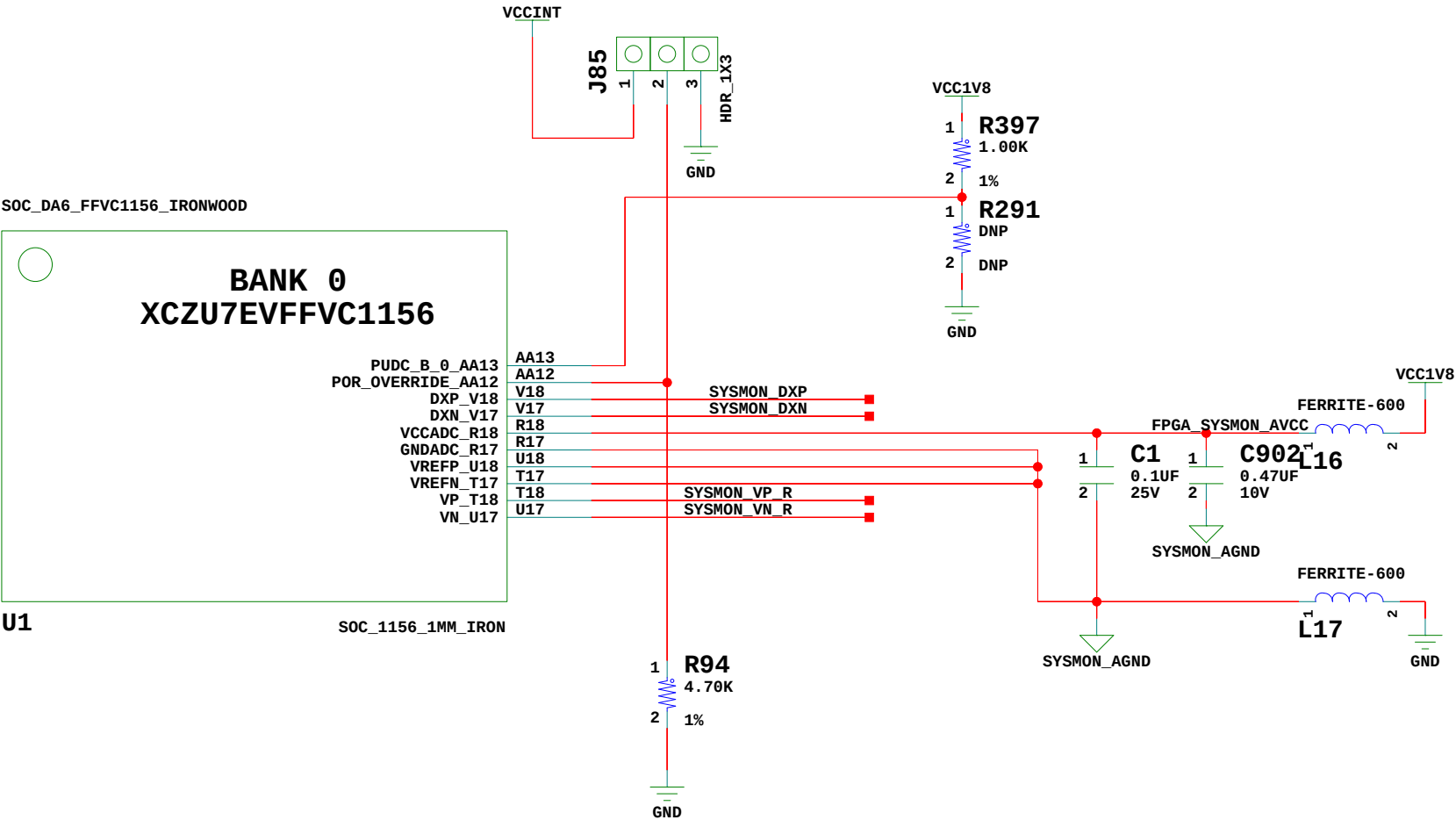
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TITLE: Title Page SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	1	OF	58
		DRAWN BY:	BF



TITLE: Block Diagram SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	2	OF	58
DRAWN BY:		BF	

POR_OVERRIDE select
Default: 2-3 GND



SYSMON I2C Address jumpers

Zynq Bank 0

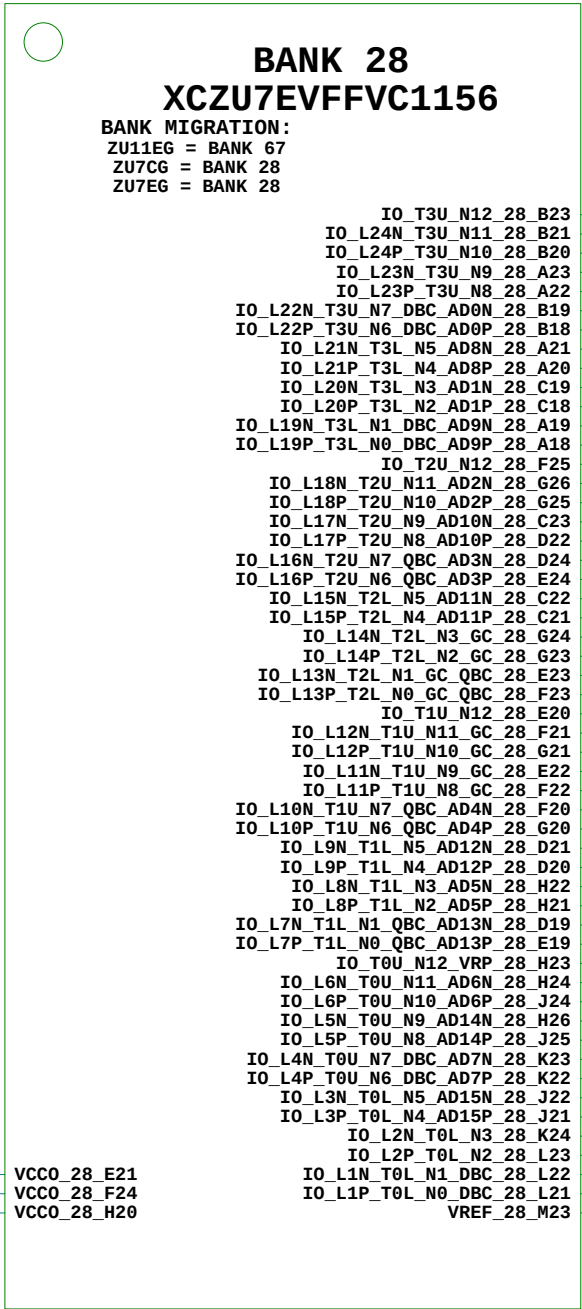


TITLE: Zynq Bank 0
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

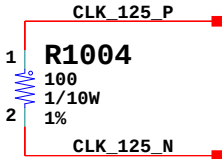
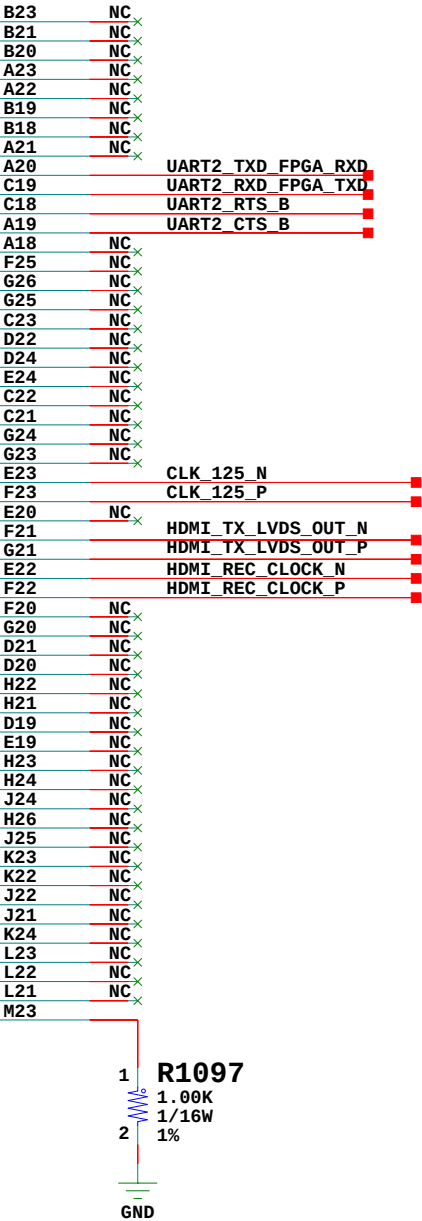
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SHEET 3 OF 58	DRAWN BY: BF

SOC_DA6_FFVC1156_IRONWOOD



U1

SOC_1156_1MM_IRON



Zynq Banks 28

			
TITLE: Zynq Banks 28 SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16		VER:	1.0
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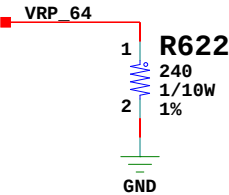
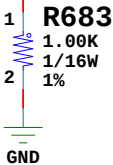
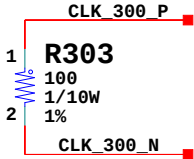
SOC_DA6_FFVC1156_IRONWOOD

BANK 64
XCZU7EVFFVC1156

IO_T3U_N12_64_AA17
IO_L24N_T3U_N11_64_AD16
IO_L24P_T3U_N10_64_AD17
IO_L23N_T3U_N9_64_AB14
IO_L23P_T3U_N8_64_AA14
IO_L22N_T3U_N7_DBC_AD0N_64_AA15
IO_L22P_T3U_N6_DBC_AD0P_64_AA16
IO_L21N_T3L_N5_AD8N_64_AB15
IO_L21P_T3L_N4_AD8P_64_AB16
IO_L20N_T3L_N3_AD1N_64_AC16
IO_L20P_T3L_N2_AD1P_64_AC17
IO_L19N_T3L_N1_DBC_AD9N_64_AE15
IO_L19P_T3L_N0_DBC_AD9P_64_AD15
IO_T2U_N12_64_AH16
IO_L18N_T2U_N11_AD2N_64_AG14
IO_L18P_T2U_N10_AD2P_64_AG15
IO_L17N_T2U_N9_AD10N_64_AF15
IO_L17P_T2U_N8_AD10P_64_AF16
IO_L16N_T2U_N7_QBC_AD3N_64_AJ14
IO_L16P_T2U_N6_QBC_AD3P_64_AH14
IO_L15N_T2L_N5_AD11N_64_AF17
IO_L15P_T2L_N4_AD11P_64_AE17
IO_L14N_T2L_N3_GC_64_AG18
IO_L14P_T2L_N2_GC_64_AF18
IO_L13N_T2L_N1_GC_QBC_64_AH17
IO_L13P_T2L_N0_GC_QBC_64_AH18
IO_T1U_N12_64_AL17
IO_L12N_T1U_N11_GC_64_AJ15
IO_L12P_T1U_N10_GC_64_AJ16
IO_L11N_T1U_N9_GC_64_AK17
IO_L11P_T1U_N8_GC_64_AJ17
IO_L10N_T1U_N7_QBC_AD4N_64_AK14
IO_L10P_T1U_N6_QBC_AD4P_64_AK15
IO_L9N_T1L_N5_AD12N_64_AL18
IO_L9P_T1L_N4_AD12P_64_AK18
IO_L8N_T1L_N3_AD5N_64_AL15
IO_L8P_T1L_N2_AD5P_64_AL16
IO_L7N_T1L_N1_QBC_AD13N_64_AM15
IO_L7P_T1L_N0_QBC_AD13P_64_AM16
IO_T0U_N12_VRP_64_AP14
IO_L6N_T0U_N11_AD6N_64_AN16
IO_L6P_T0U_N10_AD6P_64_AN17
IO_L5N_T0U_N9_AD14N_64_AP15
IO_L5P_T0U_N8_AD14P_64_AP16
IO_L4N_T0U_N7_DBC_AD7N_64_AN14
IO_L4P_T0U_N6_DBC_AD7P_64_AM14
IO_L3N_T0L_N5_AD15N_64_AN18
IO_L3P_T0L_N4_AD15P_64_AM18
IO_L2N_T0L_N3_64_AP13
IO_L2P_T0L_N2_64_AN13
IO_L1N_T0L_N1_DBC_64_AP17
IO_L1P_T0L_N0_DBC_64_AP18
VREF_64_AG16

AA17 NC
AD16 DDR4_SODIMM_PARITY
AD17 DDR4_SODIMM_CKE0
AB14 DDR4_SODIMM_RESET_B
AA14 DDR4_SODIMM_CAS_B
AA15 DDR4_SODIMM_CS0_B
AA16 DDR4_SODIMM_WE_B
AB15 DDR4_SODIMM_ALERT_B
AB16 DDR4_SODIMM_BG1
AC16 DDR4_SODIMM_BG0
AC17 DDR4_SODIMM_ACT1_B
AE15 DDR4_SODIMM_ODT0
AD15 DDR4_SODIMM_RAS_B
AH16 DDR4_SODIMM_A0
AG14 DDR4_SODIMM_A1
AG15 DDR4_SODIMM_A2
AF15 DDR4_SODIMM_A3
AF16 DDR4_SODIMM_A4
AJ14 DDR4_SODIMM_A5
AH14 DDR4_SODIMM_A6
AF17 DDR4_SODIMM_A7
AE17 NC
AG18 DDR4_SODIMM_CK0_C
AF18 DDR4_SODIMM_CK0_T
AH17 CLK_300_N
AH18 CLK_300_P
AL17 DDR4_SODIMM_CS1_B
AJ15 DDR4_SODIMM_CK1_C
AJ16 DDR4_SODIMM_CK1_T
AK17 DDR4_SODIMM_A8
AJ17 DDR4_SODIMM_A9
AK14 DDR4_SODIMM_A10
AK15 DDR4_SODIMM_A11
AL18 DDR4_SODIMM_A12
AK18 DDR4_SODIMM_A13
AL15 DDR4_SODIMM_BA0
AL16 DDR4_SODIMM_BA1
AM15 DDR4_SODIMM_CKE1
AM16 DDR4_SODIMM_ODT1
AP14 VRP_64
AN16 DDR4_SODIMM_CS3_B
AN17 DDR4_SODIMM_CS2_B
AP15 NC
AP16 NC
AN14 NC
AM14 NC
AN18 NC
AP13 NC
AN13 NC
AP17 NC
AP18 NC
AG16

VCC1V2
AE16 VCC0_64_AE16
AH15 VCC0_64_AH15
AJ18 VCC0_64_AJ18



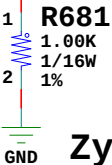
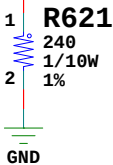
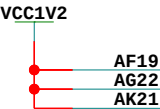
SOC_DA6_FFVC1156_IRONWOOD

BANK 65
XCZU7EVFFVC1156

IO_T3U_N12_65_AE22
IO_L24N_T3U_N11_PERSTN0_65_AA20
IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65_AA19
IO_L23N_T3U_N9_65_AD19
IO_L23P_T3U_N8_I2C_SCLK_65_AC18
IO_L22N_T3U_N7_DBC_AD0N_65_AB18
IO_L22P_T3U_N6_DBC_AD0P_65_AA18
IO_L21N_T3L_N5_AD8N_65_AE20
IO_L21P_T3L_N4_AD8P_65_AD20
IO_L20N_T3L_N3_AD1N_65_AC19
IO_L20P_T3L_N2_AD1P_65_AB19
IO_L19N_T3L_N1_DBC_AD9N_65_AE19
IO_L19P_T3L_N0_DBC_AD9P_65_AE18
IO_T2U_N12_65_AF20
IO_L18N_T2U_N11_AD2N_65_AE24
IO_L18P_T2U_N10_AD2P_65_AE23
IO_L17N_T2U_N9_AD10N_65_AF22
IO_L17P_T2U_N8_AD10P_65_AF21
IO_L16N_T2U_N7_QBC_AD3N_65_AG23
IO_L16P_T2U_N6_QBC_AD3P_65_AF23
IO_L15N_T2L_N5_AD11N_65_AG20
IO_L15P_T2L_N4_AD11P_65_AG19
IO_L14N_T2L_N3_GC_65_AH21
IO_L14P_T2L_N2_GC_65_AG21
IO_L13N_T2L_N1_GC_QBC_65_AH23
IO_L13P_T2L_N0_GC_QBC_65_AH22
IO_T1U_N12_65_AH19
IO_L12N_T1U_N11_GC_65_AJ22
IO_L12P_T1U_N10_GC_65_AJ21
IO_L11N_T1U_N9_GC_65_AK20
IO_L11P_T1U_N8_GC_65_AJ20
IO_L10N_T1U_N7_QBC_AD4N_65_AK23
IO_L10P_T1U_N6_QBC_AD4P_65_AK22
IO_L9N_T1L_N5_AD12N_65_AK19
IO_L9P_T1L_N4_AD12P_65_AJ19
IO_L8N_T1L_N3_AD5N_65_AL23
IO_L8P_T1L_N2_AD5P_65_AL22
IO_L7N_T1L_N1_QBC_AD13N_65_AL21
IO_L7P_T1L_N0_QBC_AD13P_65_AL20
IO_T0U_N12_VRP_65_AM20
IO_L6N_T0U_N11_AD6N_65_AN23
IO_L6P_T0U_N10_AD6P_65_AM23
IO_L5N_T0U_N9_AD14N_65_AP23
IO_L5P_T0U_N8_AD14P_65_AN22
IO_L4N_T0U_N7_DBC_AD7N_65_AN21
IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65_AM21
IO_L3N_T0L_N5_AD15N_65_AP22
IO_L3P_T0L_N4_AD15P_65_AP21
IO_L2N_T0L_N3_65_AN19
IO_L2P_T0L_N2_65_AM19
IO_L1N_T0L_N1_DBC_65_AP20
IO_L1P_T0L_N0_DBC_65_AP19
VREF_65_AB20

AE22 NC
AA20 DDR4_SODIMM_DQ8
AA19 DDR4_SODIMM_DQ9
AD19 DDR4_SODIMM_DQ10
AC18 DDR4_SODIMM_DQ11
AB18 DDR4_SODIMM_DQS1_C
AA18 DDR4_SODIMM_DQS1_T
AE20 DDR4_SODIMM_DQ12
AD20 DDR4_SODIMM_DQ13
AC19 DDR4_SODIMM_DQ14
AB19 DDR4_SODIMM_DQ15
AE19 NC
AE18 DDR4_SODIMM_DM1_B
AF20 NC
AE24 DDR4_SODIMM_DQ0
AE23 DDR4_SODIMM_DQ1
AF22 DDR4_SODIMM_DQ2
AF21 DDR4_SODIMM_DQ3
AG23 DDR4_SODIMM_DQS0_C
AF23 DDR4_SODIMM_DQS0_T
AG20 DDR4_SODIMM_DQ4
AG19 DDR4_SODIMM_DQ5
AH21 DDR4_SODIMM_DQ6
AG21 DDR4_SODIMM_DQ7
AH23 NC
AH22 DDR4_SODIMM_DM0_B
AH19 NC
AJ22 DDR4_SODIMM_DQ16
AJ21 DDR4_SODIMM_DQ17
AK20 DDR4_SODIMM_DQ18
AJ20 DDR4_SODIMM_DQ19
AK23 DDR4_SODIMM_DQS2_C
AK22 DDR4_SODIMM_DQS2_T
AK19 DDR4_SODIMM_DQ20
AJ19 DDR4_SODIMM_DQ21
AL23 DDR4_SODIMM_DQ22
AL22 DDR4_SODIMM_DQ23
AL21 NC
AL20 DDR4_SODIMM_DM2_B
AM20 VRP_65
AN23 DDR4_SODIMM_DQ24
AM23 DDR4_SODIMM_DQ25
AP23 DDR4_SODIMM_DQ26
AN22 DDR4_SODIMM_DQ27
AN21 DDR4_SODIMM_DQS3_C
AM21 DDR4_SODIMM_DQS3_T
AP22 DDR4_SODIMM_DQ28
AP21 DDR4_SODIMM_DQ29
AN19 DDR4_SODIMM_DQ30
AM19 DDR4_SODIMM_DQ31
AP20 NC
AP19 DDR4_SODIMM_DM3_B
AB20

VCC1V2
AF19 VCC0_65_AF19
AG22 VCC0_65_AG22
AK21 VCC0_65_AK21



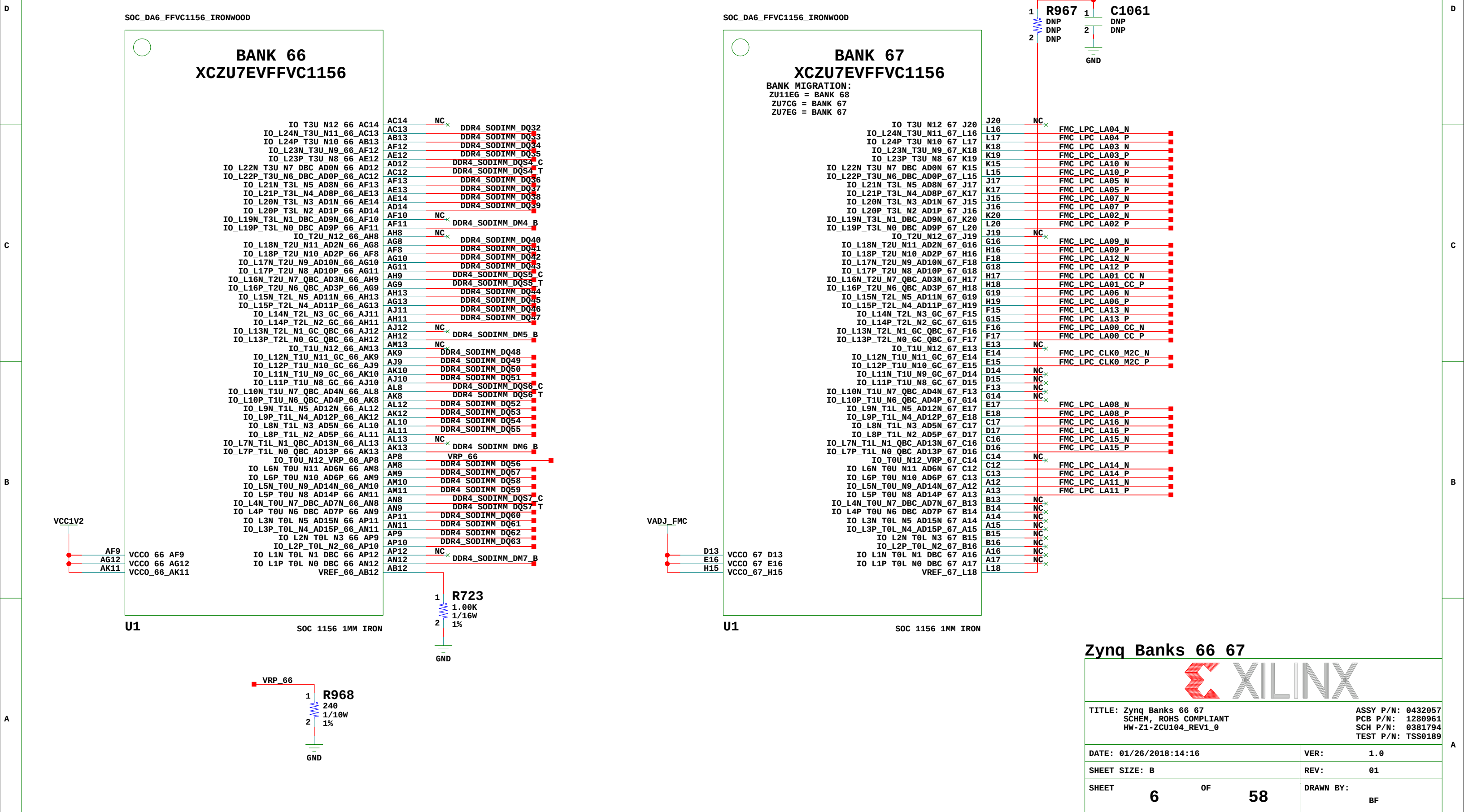
Zynq Banks 64 65



TITLE: Zynq Banks 64 65
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 5 OF 58	DRAWN BY: BF



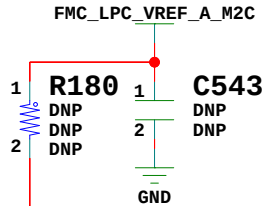
SOC_DA6_FFVC1156_IRONWOOD

BANK 68
XCZU7EVFFVC1156

BANK MIGRATION:
ZU11EG = BANK 69
ZU7CG = BANK 68
ZU7EG = BANK 68

IO_T3U_N12_68_A9
IO_L24N_T3U_N11_68_A11
IO_L24P_T3U_N10_68_B11
IO_L23N_T3U_N9_68_A7
IO_L23P_T3U_N8_68_A8
IO_L22N_T3U_N7_DBC_AD0N_68_A10
IO_L22P_T3U_N6_DBC_AD0P_68_B10
IO_L21N_T3L_N5_AD8N_68_A6
IO_L21P_T3L_N4_AD8P_68_B6
IO_L20N_T3L_N3_AD1N_68_B8
IO_L20P_T3L_N2_AD1P_68_B9
IO_L19N_T3L_N1_DBC_AD9N_68_C6
IO_L19P_T3L_N0_DBC_AD9P_68_C7
IO_T2U_N12_68_G13
IO_L18N_T2U_N11_AD2N_68_C11
IO_L18P_T2U_N10_AD2P_68_D12
IO_L17N_T2U_N9_AD10N_68_E12
IO_L17P_T2U_N8_AD10P_68_F12
IO_L16N_T2U_N7_QBC_AD3N_68_D10
IO_L16P_T2U_N6_QBC_AD3P_68_D11
IO_L15N_T2L_N5_AD11N_68_H12
IO_L15P_T2L_N4_AD11P_68_H13
IO_L14N_T2L_N3_GC_68_E10
IO_L14P_T2L_N2_GC_68_F11
IO_L13N_T2L_N1_GC_QBC_68_G11
IO_L13P_T2L_N0_GC_QBC_68_H11
IO_T1U_N12_68_D7
IO_L12N_T1U_N11_GC_68_F10
IO_L12P_T1U_N10_GC_68_G10
IO_L11N_T1U_N9_GC_68_G9
IO_L11P_T1U_N8_GC_68_H9
IO_L10N_T1U_N7_QBC_AD4N_68_D9
IO_L10P_T1U_N6_QBC_AD4P_68_E9
IO_L9N_T1L_N5_AD12N_68_E8
IO_L9P_T1L_N4_AD12P_68_F8
IO_L8N_T1L_N3_AD5N_68_C8
IO_L8P_T1L_N2_AD5P_68_C9
IO_L7N_T1L_N1_QBC_AD13N_68_E7
IO_L7P_T1L_N0_QBC_AD13P_68_F7
IO_T0U_N12_VRP_68_H14
IO_L6N_T0U_N11_AD6N_68_K13
IO_L6P_T0U_N10_AD6P_68_L14
IO_L5N_T0U_N9_AD14N_68_J14
IO_L5P_T0U_N8_AD14P_68_K14
IO_L4N_T0U_N7_DBC_AD7N_68_J11
IO_L4P_T0U_N6_DBC_AD7P_68_K12
IO_L3N_T0L_N5_AD15N_68_L11
IO_L3P_T0L_N4_AD15P_68_L12
IO_L2N_T0L_N3_68_J10
IO_L2P_T0L_N2_68_K10
IO_L1N_T0L_N1_DBC_68_L13
IO_L1P_T0L_N0_DBC_68_M13
VREF_68_J12

A9 NC
A11 FMC LPC LA23 N
B11 FMC LPC LA23 P
A7 FMC LPC LA27 N
A8 FMC LPC LA27 P
A10 FMC LPC LA21 N
B10 FMC LPC LA21 P
A6 FMC LPC LA24 N
B6 FMC LPC LA24 P
B8 FMC LPC LA26 N
B9 FMC LPC LA26 P
C6 FMC LPC LA25 N
C7 FMC LPC LA25 P
G13 NC
C11 FMC LPC LA19 N
D12 FMC LPC LA19 P
E12 FMC LPC LA20 N
F12 FMC LPC LA20 P
D10 FMC LPC LA18 CC N
D11 FMC LPC LA18 CC P
H12 FMC LPC LA22 N
H13 FMC LPC LA22 P
E10 FMC LPC LA17 CC N
F11 FMC LPC LA17 CC P
G11 NC
H11 NC
D7 NC
F10 FMC LPC CLK1 M2C N
G10 FMC LPC CLK1 M2C P
G9 NC
H9 NC
D9 FMC LPC LA30 N
E9 FMC LPC LA30 P
E8 FMC LPC LA32 N
F8 FMC LPC LA32 P
C8 FMC LPC LA33 N
C9 FMC LPC LA33 P
E7 FMC LPC LA31 N
F7 FMC LPC LA31 P
H14 VRP_68
K13 NC
L14 NC
J14 NC
K14 NC
J11 NC
K12 NC
L11 NC
L12 NC
J10 FMC LPC LA29 N
K10 FMC LPC LA29 P
L13 FMC LPC LA28 N
M13 FMC LPC LA28 P
J12

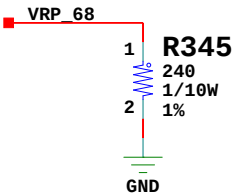


VADJ_FMC

F9 VCC0_68_F9
G12 VCC0_68_G12
K11 VCC0_68_K11

U1

SOC_1156_1MM_IRON



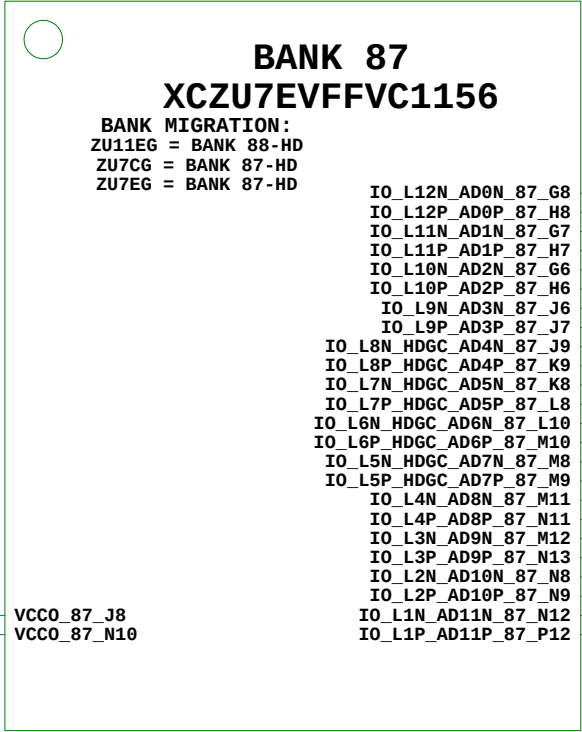
Zynq Banks 68



TITLE: Zynq Banks 68
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0
ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 7 OF 58	DRAWN BY: BF

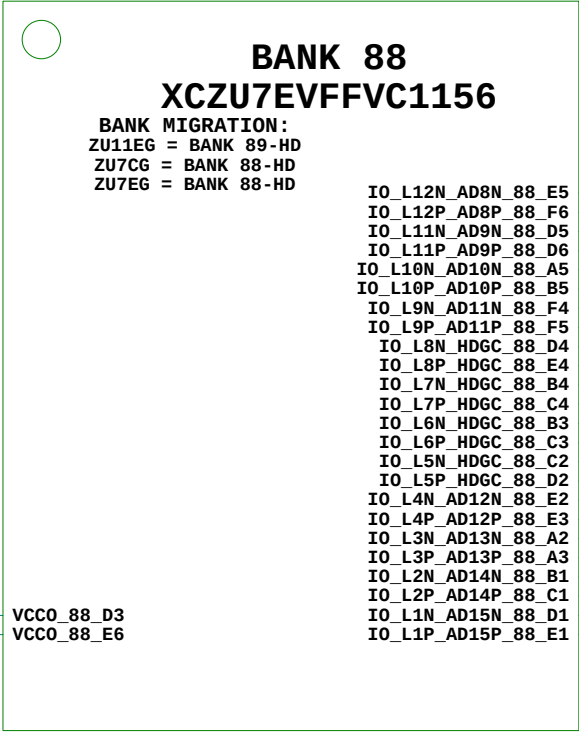
SOC_DA6_FFVC1156_IRONWOOD



U1

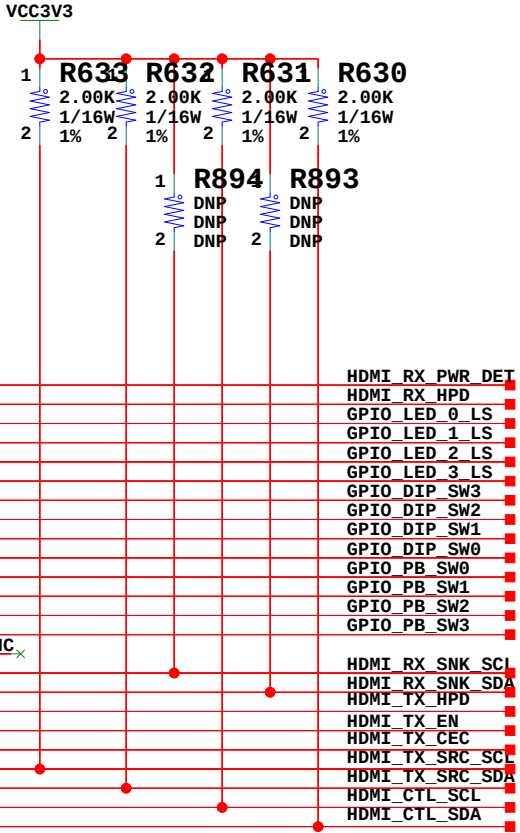
SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD



U1

SOC_1156_1MM_IRON



Zynq Banks 87 88



TITLE: Zynq Banks 87 88
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 8 OF 58	DRAWN BY: BF

SOC_DA6_FFVC1156_IRONWOOD

BANK 223
XCZU7EVFFVC1156

BANK MIGRATION:
ZU11EG = BANK 224
ZU7CG = BANK 223
ZU7EG = BANK 223

MGHTXP0_223_AN6
MGHTXN0_223_AN5
MGTHRX0_223_AP4
MGTHRX0_223_AP3
MGHTXP1_223_AM4
MGHTXN1_223_AM3
MGTHRX1_223_AN2
MGTHRX1_223_AN1
MGHTXP2_223_AL6
MGHTXN2_223_AL5
MGTHRX2_223_AL2
MGTHRX2_223_AL1
MGHTXP3_223_AJ6
MGHTXN3_223_AJ5
MGTHRX3_223_AK4
MGTHRX3_223_AK3
MGTREFCLK0P_223_AD8
MGTREFCLK0N_223_AD7
MGTREFCLK1P_223_AC10
MGTREFCLK1N_223_AC9

AN6 NC
AN5 NC
AP4
AP3
AM4 NC
AM3 NC
AN2
AN1 NC
AL6 NC
AL5 NC
AL2
AL1
AJ6 NC
AJ5 NC
AK4
AK3
AD8 NC
AD7 NC
AC10 NC
AC9 NC

U1

SOC_1156_1MM_IRON

GND

SOC_DA6_FFVC1156_IRONWOOD

BANK 224
XCZU7EVFFVC1156

BANK MIGRATION:
ZU11EG = BANK 225
ZU7CG = BANK 224
ZU7EG = BANK 224

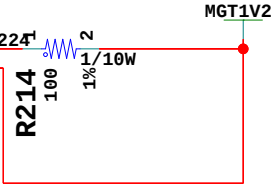
MGHTXP0_224_AH4
MGHTXN0_224_AH3
MGTHRX0_224_AJ2
MGTHRX0_224_AJ1
MGHTXP1_224_AG6
MGHTXN1_224_AG5
MGTHRX1_224_AG2
MGTHRX1_224_AG1
MGHTXP2_224_AE6
MGHTXN2_224_AE5
MGTHRX2_224_AF4
MGTHRX2_224_AF3
MGHTXP3_224_AD4
MGHTXN3_224_AD3
MGTHRX3_224_AE2
MGTHRX3_224_AE1
MGTREFCLK0P_224_AB8
MGTREFCLK0N_224_AB7
MGTREFCLK1P_224_AA10
MGTREFCLK1N_224_AA9
MGTRREF_R_AD10
MGTAVTTRCAL_R_AD9

AH4 NC
AH3 NC
AJ2
AJ1
AG6 NC
AG5 NC
AG2
AG1
AE6 NC
AE5 NC
AF4
AF3
AD4 NC
AD3 NC
AE2
AE1
AB8 NC
AB7 NC
AA10 NC
AA9 NC
AD10
AD9

U1

SOC_1156_1MM_IRON

GND



Zynq Banks 223 224



TITLE: Zynq Banks 223 224
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16

VER: 1.0

SHEET SIZE: B

REV: 01

SHEET

9

OF

58

DRAWN BY:

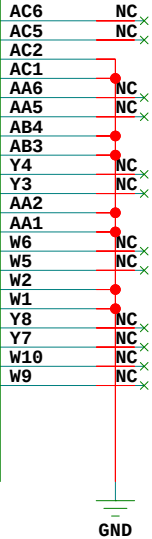
BF

SOC_DA6_FFVC1156_IRONWOOD

BANK 225
XCZU7EVFFVC1156

BANK MIGRATION:
ZU11EG = BANK 226
ZU7CG = BANK 225
ZU7EG = BANK 225

MGTHTXP0_225_AC6
MGHTXN0_225_AC5
MGTHRXP0_225_AC2
MGTHRXN0_225_AC1
MGTHTXP1_225_AA6
MGHTXN1_225_AA5
MGTHRXP1_225_AB4
MGTHRXN1_225_AB3
MGTHTXP2_225_Y4
MGHTXN2_225_Y3
MGTHRXP2_225_AA2
MGTHRXN2_225_AA1
MGTHTXP3_225_W6
MGHTXN3_225_W5
MGTHRXP3_225_W2
MGTHRXN3_225_W1
MGTREFCLK0P_225_Y8
MGTREFCLK0N_225_Y7
MGTREFCLK1P_225_W10
MGTREFCLK1N_225_W9



U1

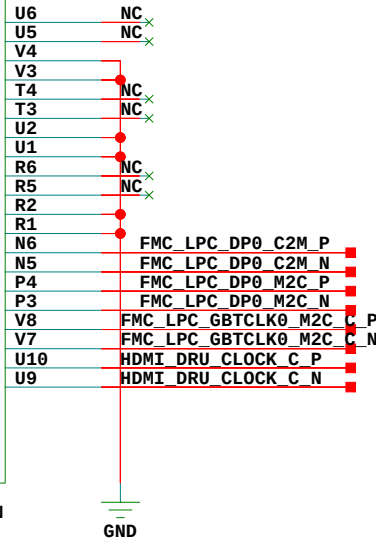
SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD

BANK 226
XCZU7EVFFVC1156

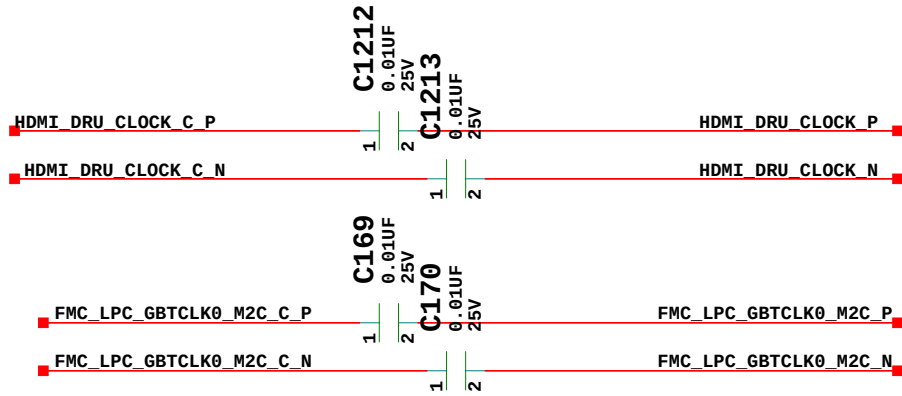
BANK MIGRATION:
ZU11EG = BANK 227
ZU7CG = BANK 226
ZU7EG = BANK 226

MGTHTXP0_226_U6
MGHTXN0_226_U5
MGTHRXP0_226_V4
MGTHRXN0_226_V3
MGTHTXP1_226_T4
MGHTXN1_226_T3
MGTHRXP1_226_U2
MGTHRXN1_226_U1
MGTHTXP2_226_R6
MGHTXN2_226_R5
MGTHRXP2_226_R2
MGTHRXN2_226_R1
MGTHTXP3_226_N6
MGHTXN3_226_N5
MGTHRXP3_226_P4
MGTHRXN3_226_P3
MGTREFCLK0P_226_V8
MGTREFCLK0N_226_V7
MGTREFCLK1P_226_U10
MGTREFCLK1N_226_U9



U1

SOC_1156_1MM_IRON

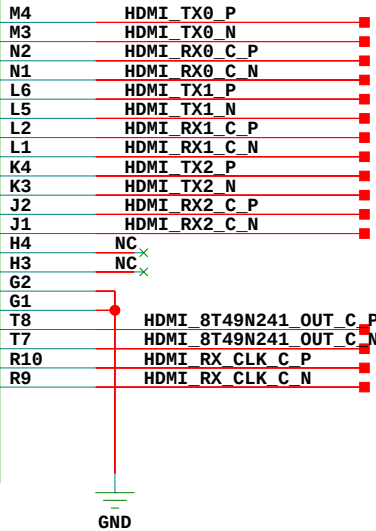


SOC_DA6_FFVC1156_IRONWOOD

BANK 227
XCZU7EVFFVC1156

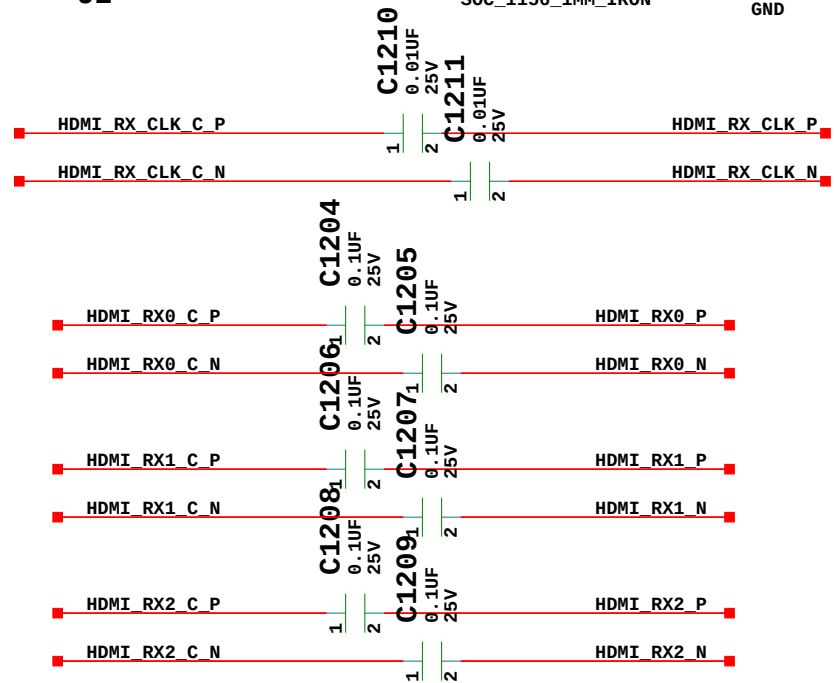
BANK MIGRATION:
ZU11EG = BANK 228
ZU7CG = BANK 227
ZU7EG = BANK 227

MGTHTXP0_227_M4
MGHTXN0_227_M3
MGTHRXP0_227_N2
MGTHRXN0_227_N1
MGTHTXP1_227_L6
MGHTXN1_227_L5
MGTHRXP1_227_L2
MGTHRXN1_227_L1
MGTHTXP2_227_K4
MGHTXN2_227_K3
MGTHRXP2_227_J2
MGTHRXN2_227_J1
MGTHTXP3_227_H4
MGHTXN3_227_H3
MGTHRXP3_227_G2
MGTHRXN3_227_G1
MGTREFCLK0P_227_T8
MGTREFCLK0N_227_T7
MGTREFCLK1P_227_R10
MGTREFCLK1N_227_R9



U1

SOC_1156_1MM_IRON



Zynq Banks 225 226 227



TITLE: Zynq Banks 225 226 227
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0
ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 10 OF 58	DRAWN BY: BF

SOC_DA6_FFVC1156_IRONWOOD

BANK 500
XCZU7EVFFVC1156

PS_MIO25_D29	D29	MIO25_CAN_RX	
PS_MIO24_E28	E28	MIO24_CAN_TX	
PS_MIO23_B29	B29	NC	
PS_MIO22_F28	F28	NC	
PS_MIO21_C28	C28	UART1_TXD_MIO21_RXD	
PS_MIO20_E29	E29	UART1_RXD_MIO20_TXD	
PS_MIO19_B28	B28	UART0_RXD_MIO19_TXD	
PS_MIO18_F27	F27	UART0_TXD_MIO18_RXD	
PS_MIO17_C29	C29	MIO17_I2C1_SDA	
PS_MIO16_A28	A28	MIO16_I2C1_SCL	
PS_MIO15_E27	E27	NC	
PS_MIO14_A27	A27	NC	
PS_MIO13_D27	D27	NC	
PS_MIO12_C27	C27	NC	
PS_MIO11_B26	B26	NC	
PS_MIO10_F26	F26	NC	
PS_MIO9_C26	C26	NC	
PS_MIO8_D26	D26	NC	
PS_MIO7_B25	B25	NC	
PS_MIO6_A26	A26	NC	
PS_MIO5_D25	D25	MIO5_QSPI_LWR_CS_B	
PS_MIO4_A25	A25	MIO4_QSPI_LWR_DQ0	
PS_MIO3_E25	E25	MIO3_QSPI_LWR_DQ3	
PS_MIO2_B24	B24	MIO2_QSPI_LWR_DQ2	
PS_MIO1_C24	C24	MIO1_QSPI_LWR_DQ1	
PS_MIO0_A24	A24	MIO0_QSPI_LWR_CLK	

U1

SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD

BANK 502
XCZU7EVFFVC1156

PS_MIO77_L34	L34	MIO77_ENET_MDIO	
PS_MIO76_L33	L33	MIO76_ENET_MDC	
PS_MIO75_L30	L30	MIO75_ENET_RX_CTRL	
PS_MIO74_L29	L29	MIO74_ENET_RX_D3	
PS_MIO73_K34	K34	MIO73_ENET_RX_D2	
PS_MIO72_K33	K33	MIO72_ENET_RX_D1	
PS_MIO71_K32	K32	MIO71_ENET_RX_D0	
PS_MIO70_K31	K31	MIO70_ENET_RX_CLK	
PS_MIO69_K30	K30	MIO69_ENET_TX_CTRL	
PS_MIO68_K29	K29	MIO68_ENET_TX_D3	
PS_MIO67_K28	K28	MIO67_ENET_TX_D2	
PS_MIO66_J34	J34	MIO66_ENET_TX_D1	
PS_MIO65_J32	J32	MIO65_ENET_TX_D0	
PS_MIO64_J31	J31	MIO64_ENET_TX_CLK	
PS_MIO63_J30	J30	MIO63_USB_DATA7_R	
PS_MIO62_J29	J29	MIO62_USB_DATA6_R	
PS_MIO61_H34	H34	MIO61_USB_DATA5_R	
PS_MIO60_H33	H33	MIO60_USB_DATA4_R	
PS_MIO59_H32	H32	MIO59_USB_DATA3_R	
PS_MIO58_H31	H31	MIO58_USB_STP_R	
PS_MIO57_H29	H29	MIO57_USB_DATA1_R	
PS_MIO56_G34	G34	MIO56_USB_DATA0_R	
PS_MIO55_G33	G33	MIO55_USB_NXT	
PS_MIO54_G31	G31	MIO54_USB_DATA2_R	
PS_MIO53_G30	G30	MIO53_USB_DIR	
PS_MIO52_G29	G29	MIO52_USB_CLK	

U1

SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD

BANK 501
XCZU7EVFFVC1156

PS_MIO51_F34	F34	MIO51_SDIO_CLK_R	
PS_MIO50_F33	F33	MIO50_SDIO_CMD_R	
PS_MIO49_F32	F32	MIO49_SDIO_DAT3_R	
PS_MIO48_F31	F31	MIO48_SDIO_DAT2_R	
PS_MIO47_F30	F30	MIO47_SDIO_DAT1_R	
PS_MIO46_E34	E34	MIO46_SDIO_DAT0_R	
PS_MIO45_E33	E33	MIO45_SDIO_DETECT	
PS_MIO44_E32	E32	NC	
PS_MIO43_E30	E30	NC	
PS_MIO42_D34	D34	NC	
PS_MIO41_D32	D32	NC	
PS_MIO40_D31	D31	NC	
PS_MIO39_D30	D30	NC	
PS_MIO38_C34	C34	NC	
PS_MIO37_C33	C33	NC	
PS_MIO36_C32	C32	NC	
PS_MIO35_C31	C31	NC	
PS_MIO34_B34	B34	NC	
PS_MIO33_B33	B33	NC	
PS_MIO32_B31	B31	NC	
PS_MIO31_B30	B30	NC	
PS_MIO30_A33	A33	MIO30_DP_AUX_IN	
PS_MIO29_A32	A32	MIO29_DP_OE	
PS_MIO28_A31	A31	MIO28_DP_HPD	
PS_MIO27_A30	A30	MIO27_DP_AUX_OUT	
PS_MIO26_A29	A29	NC	

U1

SOC_1156_1MM_IRON

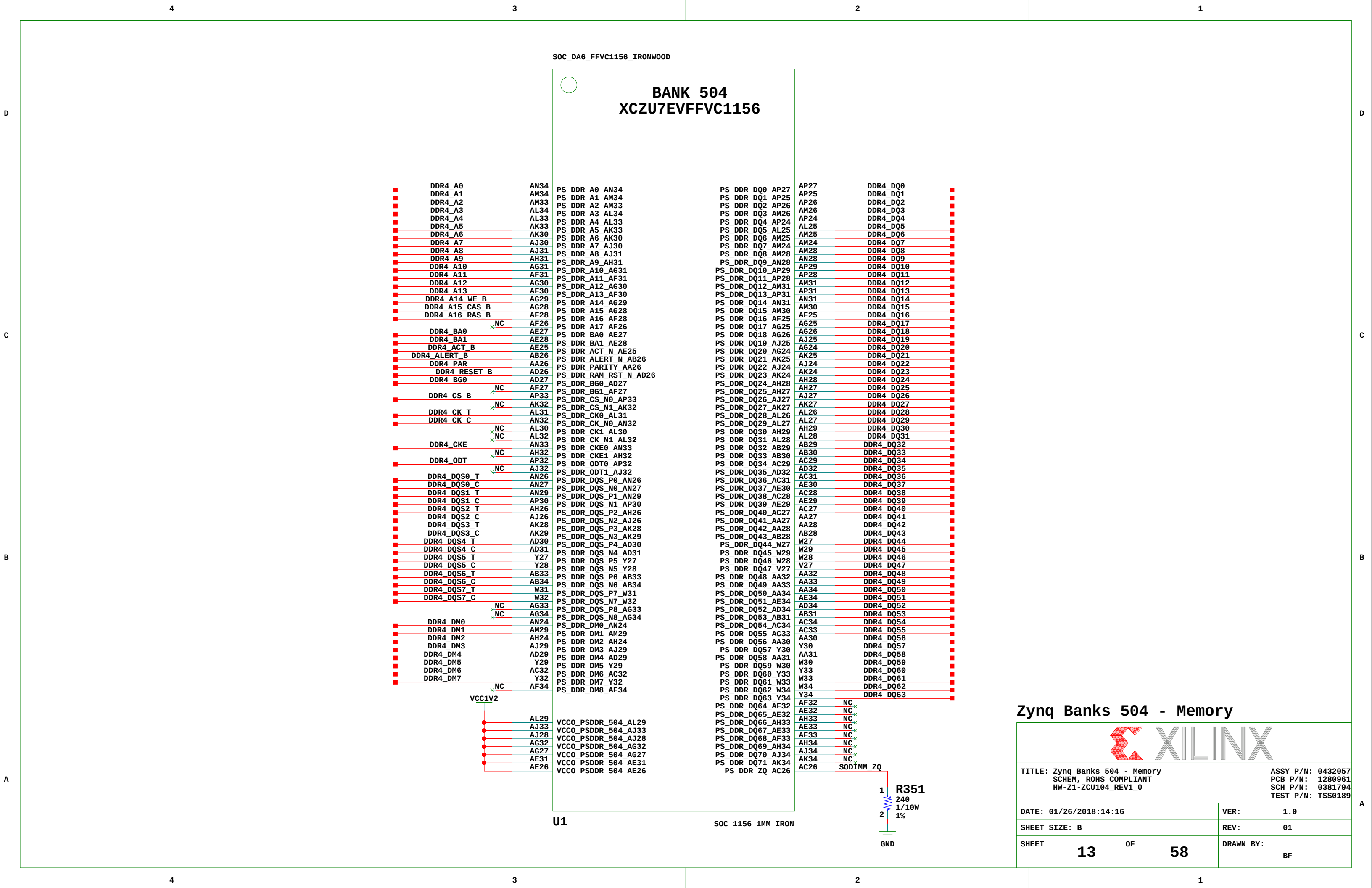
Zynq Banks 500 501 502 - MIO



TITLE: Zynq Banks 500 501 502 - MIO
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

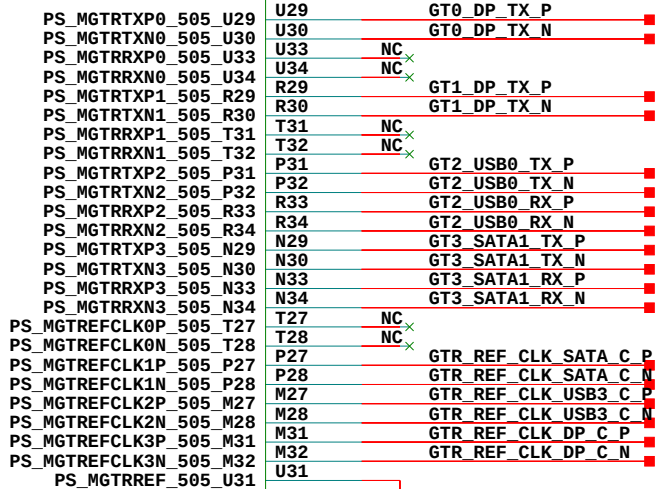
ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 11 OF 58	DRAWN BY: BF



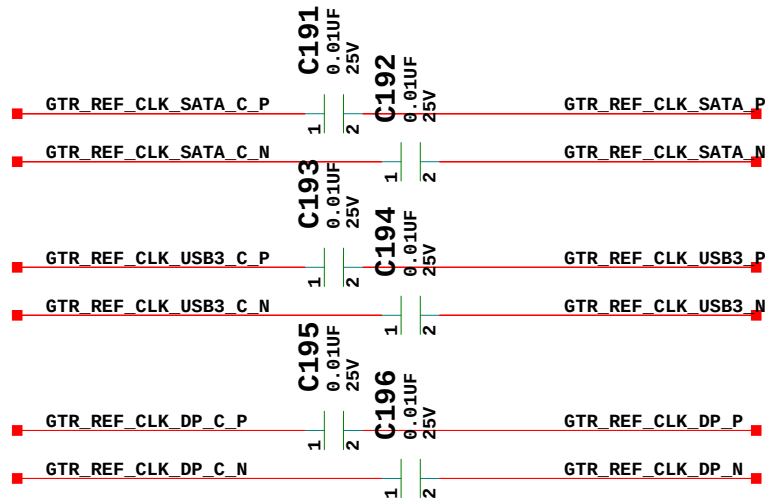
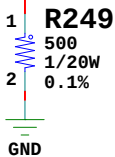
SOC_DA6_FFVC1156_IRONWOOD

BANK 505
XCZU7EVFFVC1156



U1

SOC_1156_1MM_IRON



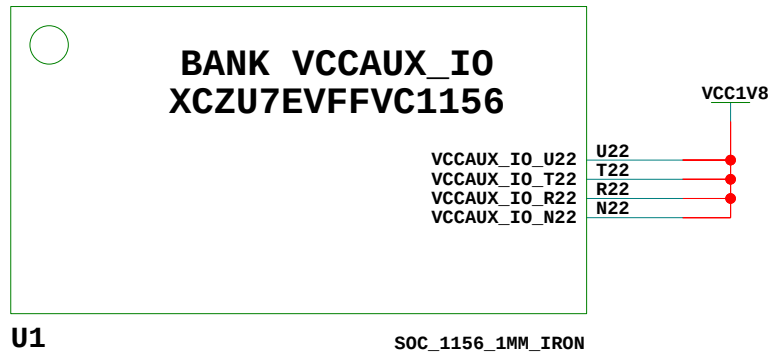
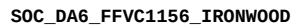
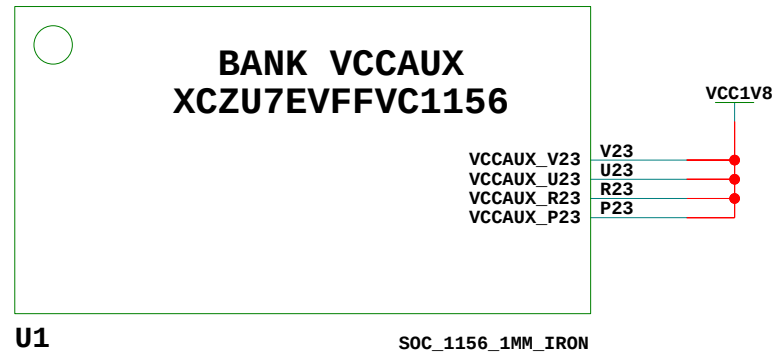
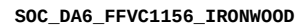
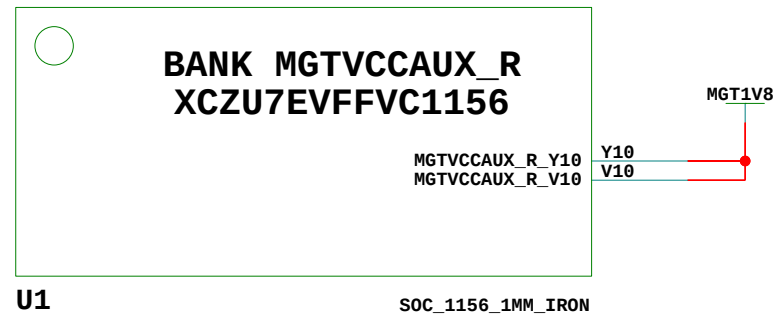
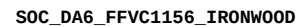
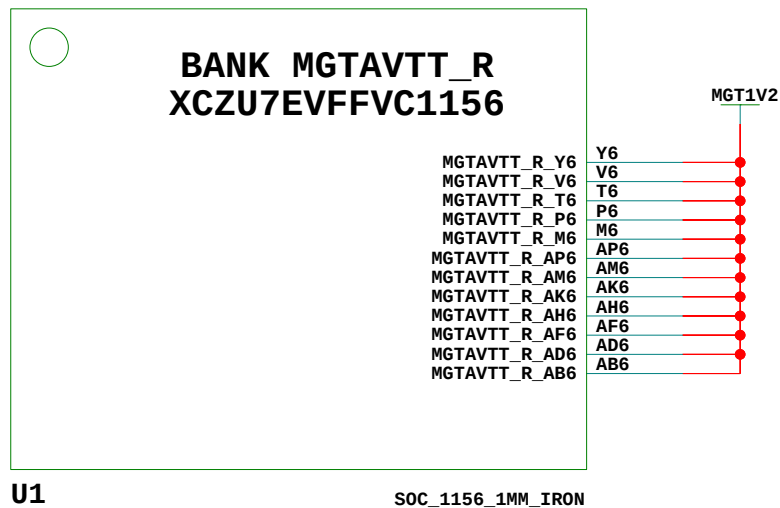
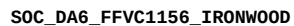
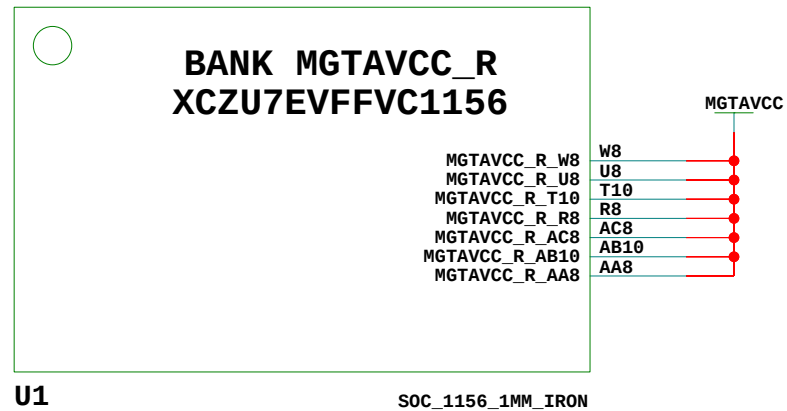
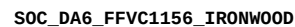
Zynq Banks 505 - GTR



TITLE: Zynq Banks 505 - GTR
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:17	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 14 OF 58	DRAWN BY: BF



Zynq Power 1



TITLE: Zynq Power 1
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16

VER: 1.0

SHEET SIZE: B

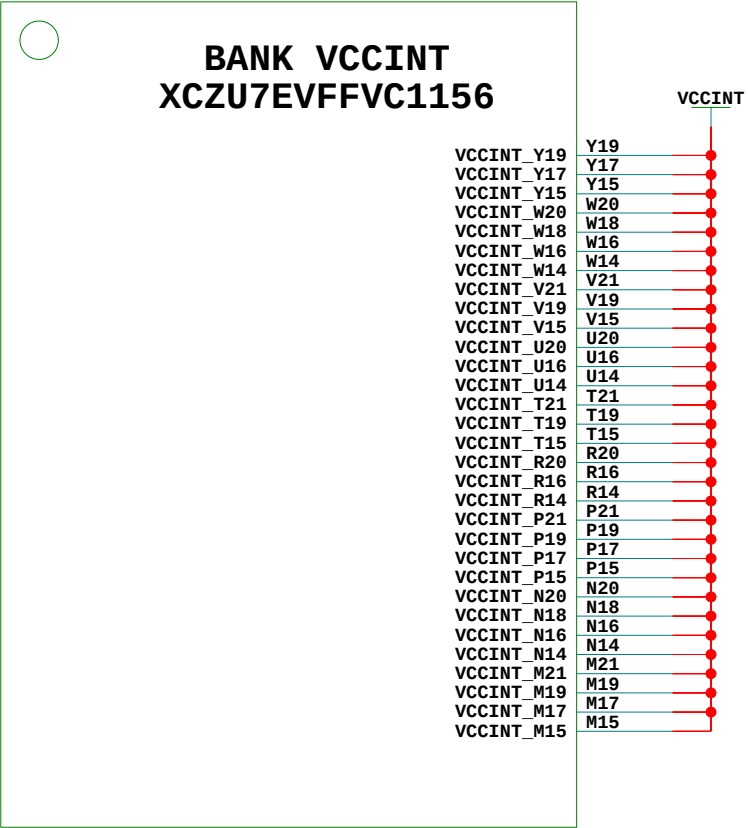
REV: 01

SHEET **15** OF **58**

DRAWN BY:

BF

SOC_DA6_FFVC1156_IRONWOOD



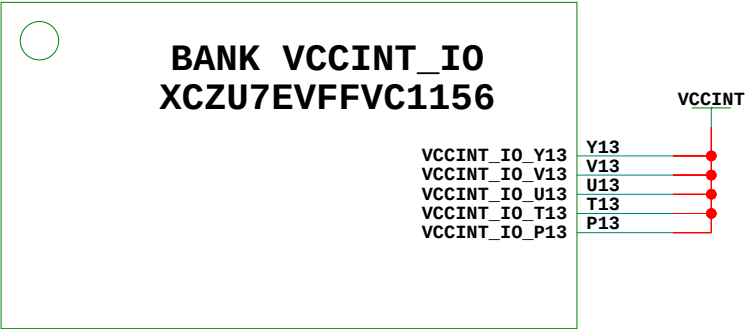
U1 SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD



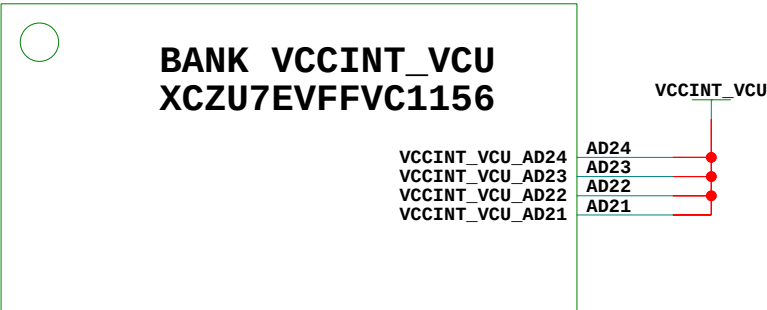
U1 SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD



U1 SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD



U1 SOC_1156_1MM_IRON

Zynq Power 2

			
TITLE: Zynq Power 2 SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	16	OF	58
		DRAWN BY:	BF

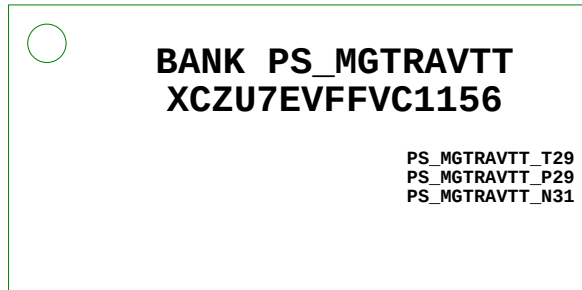
SOC_DA6_FFVC1156_IRONWOOD



U1

SOC_1156_1MM_IRON

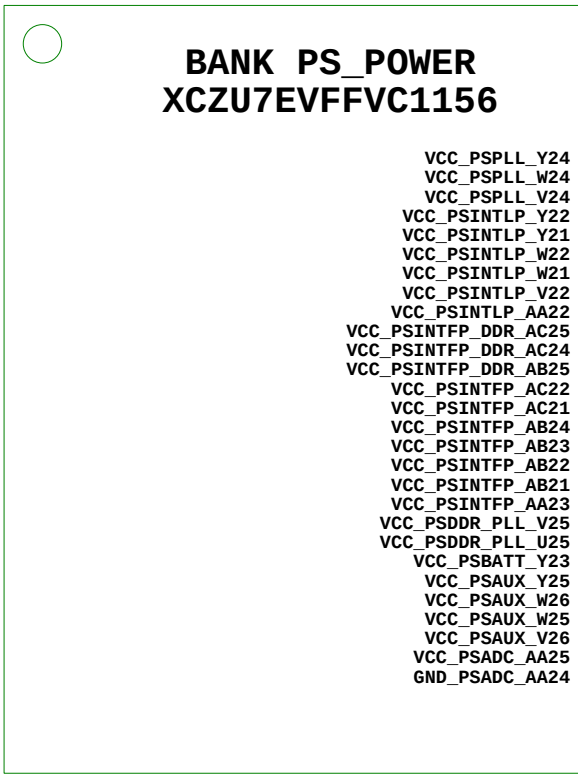
SOC_DA6_FFVC1156_IRONWOOD



U1

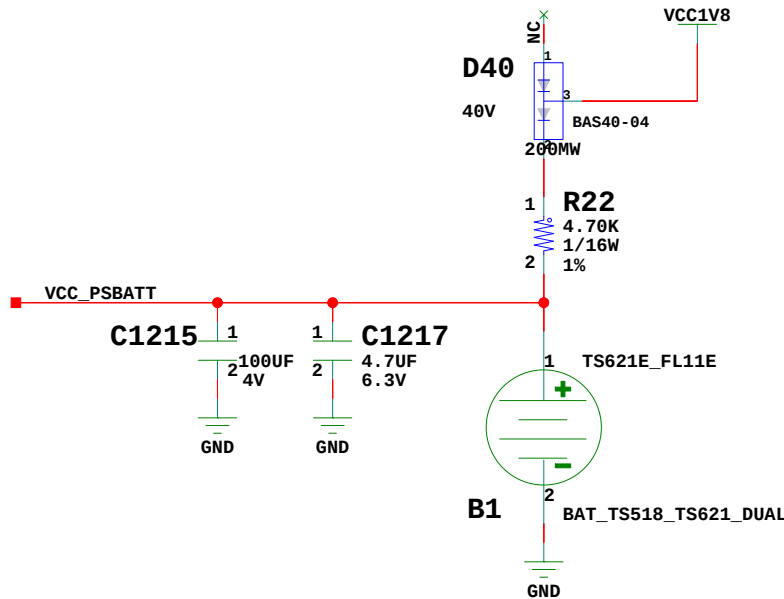
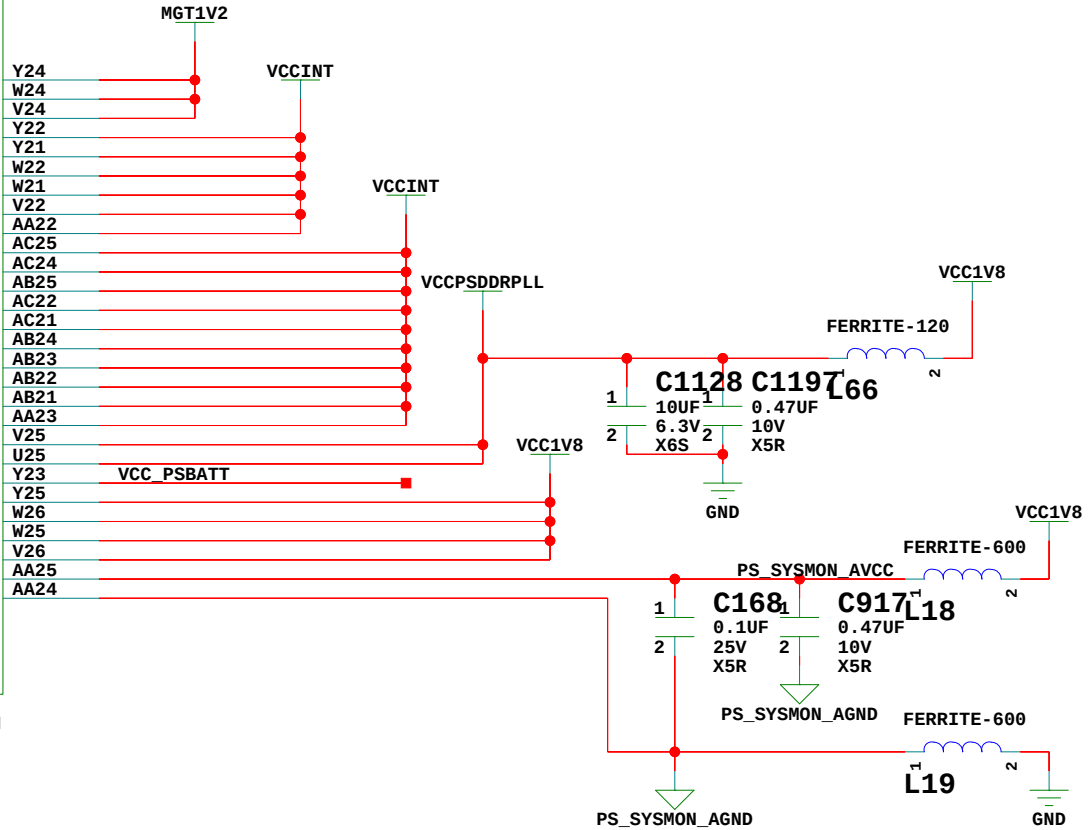
SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD



U1

SOC_1156_1MM_IRON

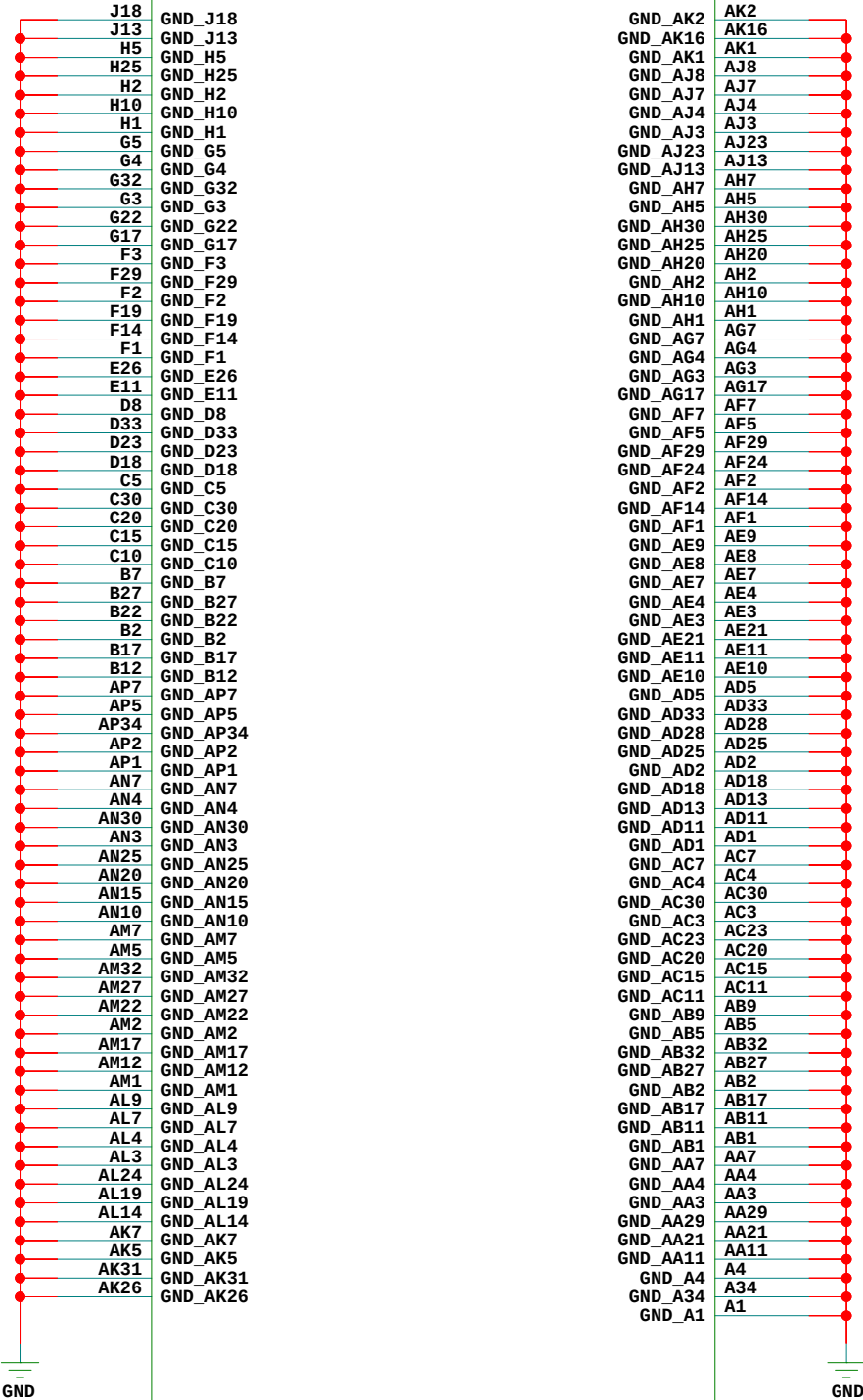


Zynq Power 3

TITLE: Zynq Power 3 SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0	
ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 17 OF 58	DRAWN BY: BF

SOC_DA6_FFVC1156_IRONWOOD

BANK GND1
XCZU7EVFFVC1156

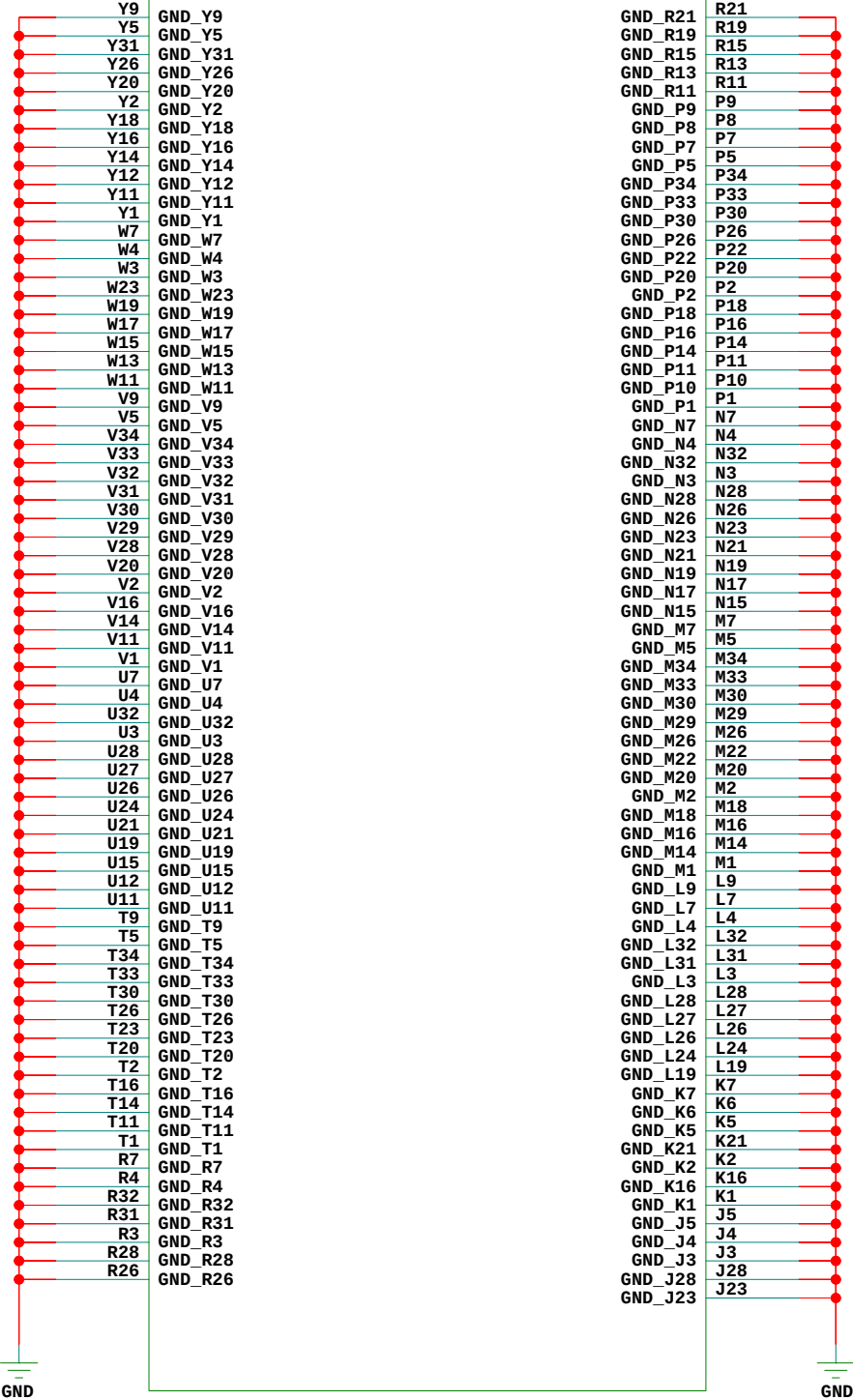


U1

SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD

BANK GND2
XCZU7EVFFVC1156



U1

SOC_1156_1MM_IRON

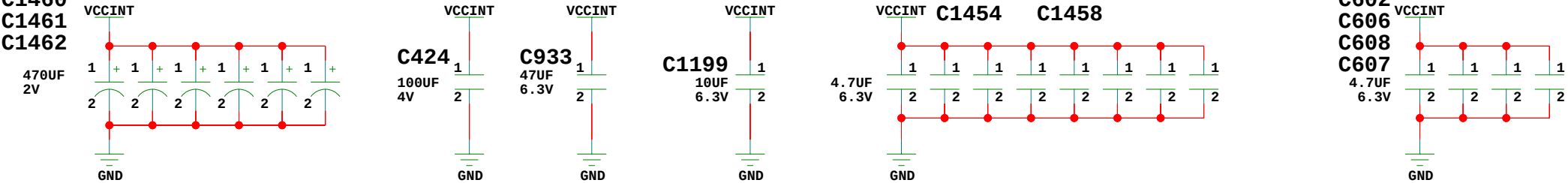
Zynq GND



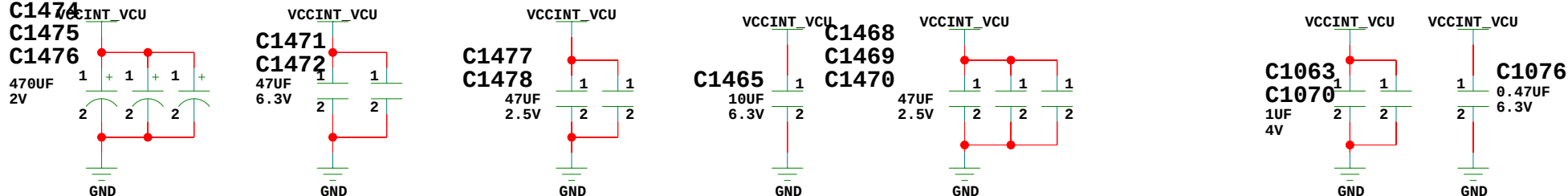
TITLE: Zynq GND SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0	ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189
---	--

DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 18 OF 58	DRAWN BY: BF

VCCINT/VCCBRAM

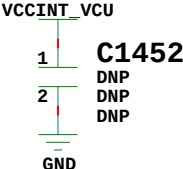
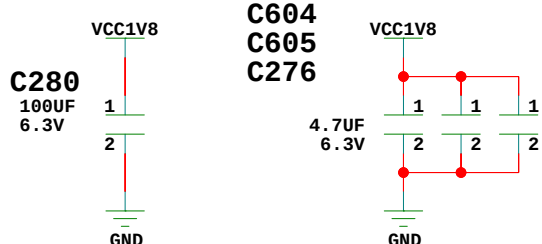


VCCINT_VCU



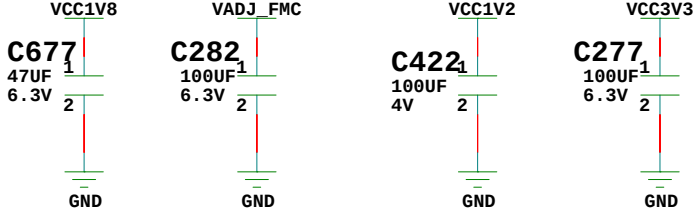
Place these 0201 capacitors directly under U1 near pins AD24/AD23/AD22/AD21. Provide a dual footprint to also support a 0402 cap

VCCAUX / VCCAUX_IO

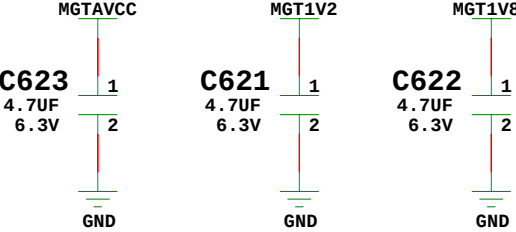


VCCINT_VCU Test Point. Place just outside U1 on bottomside

VCC0 BANKS 0 28 64 65 66 67 68 87 88

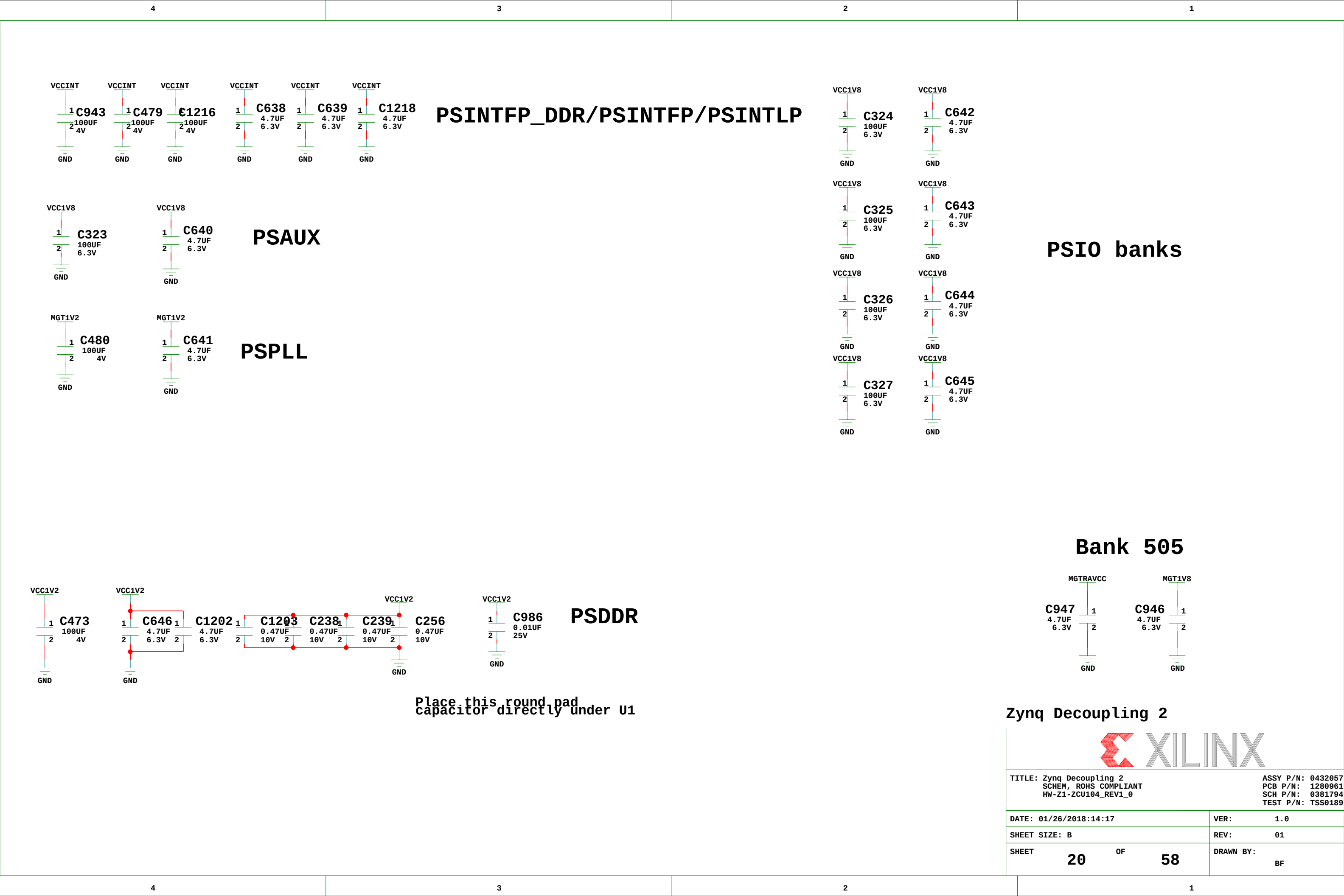


MGT Power Rails



Zynq Decoupling 1

TITLE: Zynq Decoupling 1 SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0	
DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 19 OF 58	DRAWN BY: BF



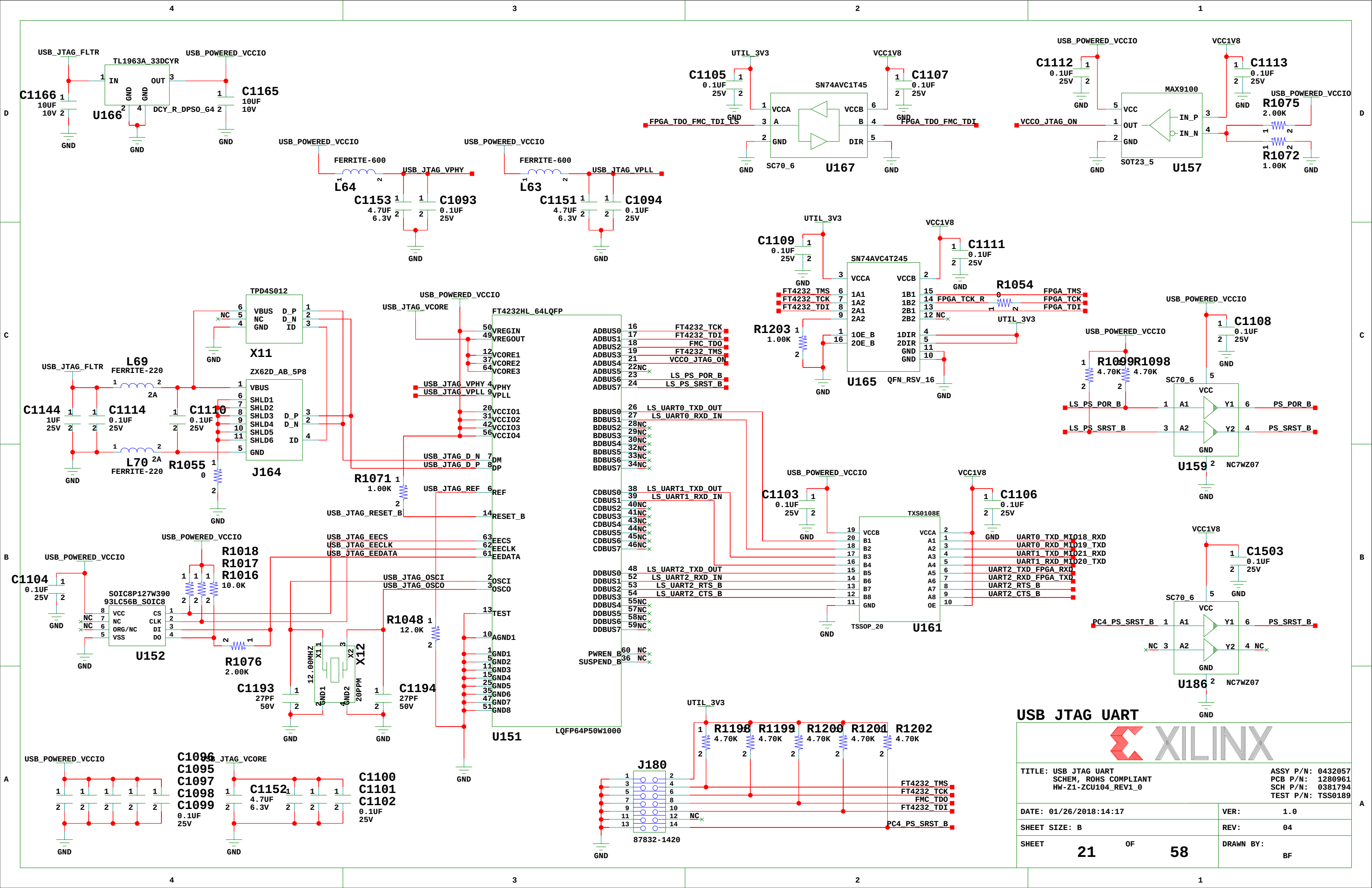
Place this round pad capacitor directly under U1



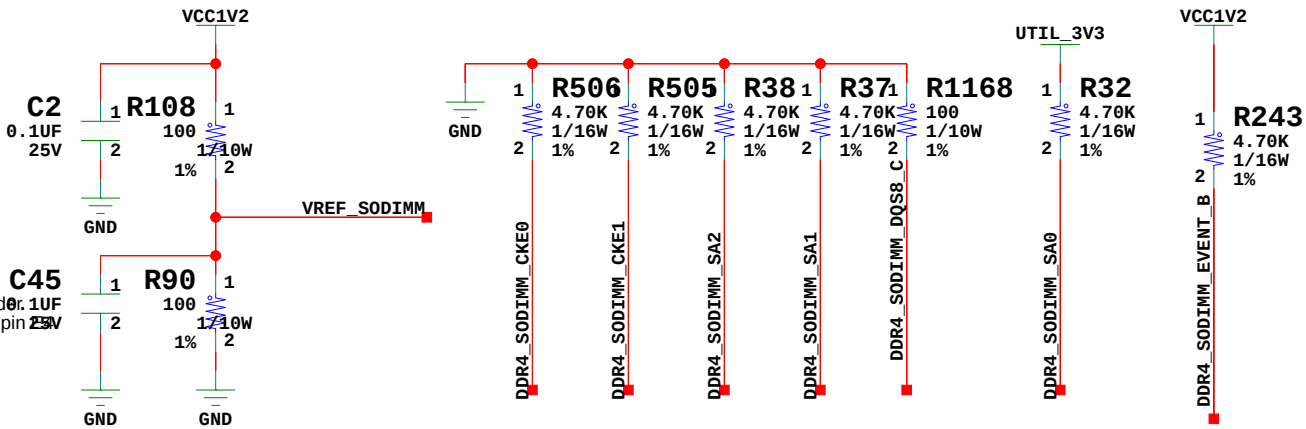
TITLE: Zynq Decoupling 2
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

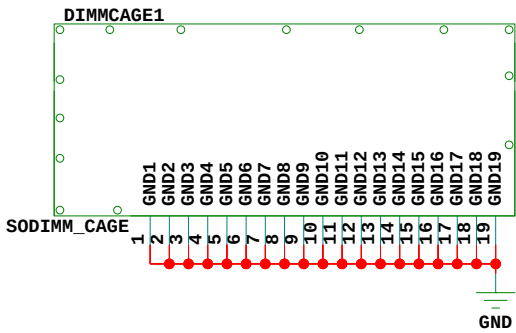
DATE: 01/26/2018:14:17	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 20 OF 58	DRAWN BY: BF



Layout Directive:
Place 0.1uF cap under 0.1uF
memory adjacent to pin 25V

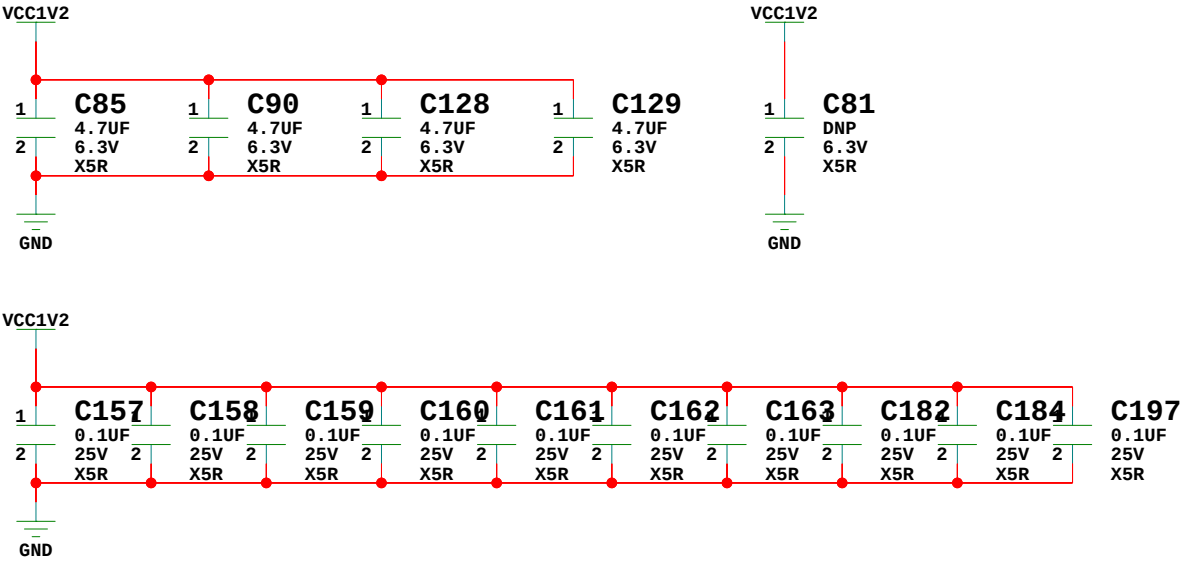


IIC Address = 0b1010001 (0x51)
SODIMM SA[2:0]=001



PL DDR4 SODIMM 64 bit

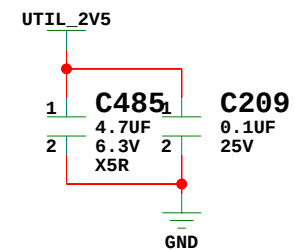
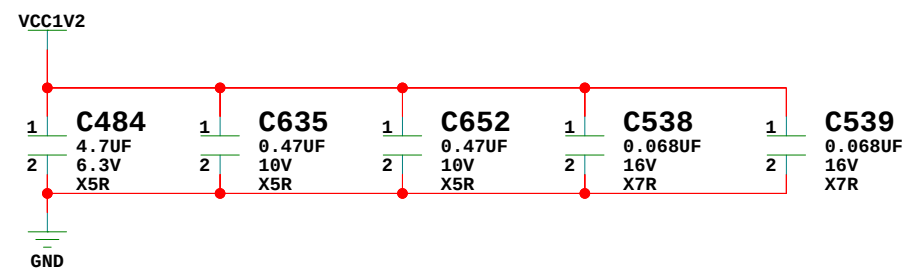
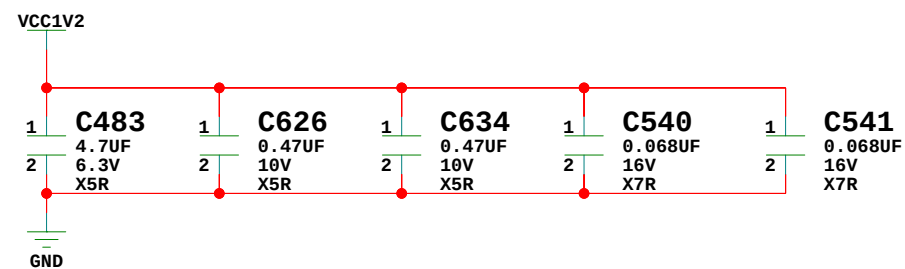
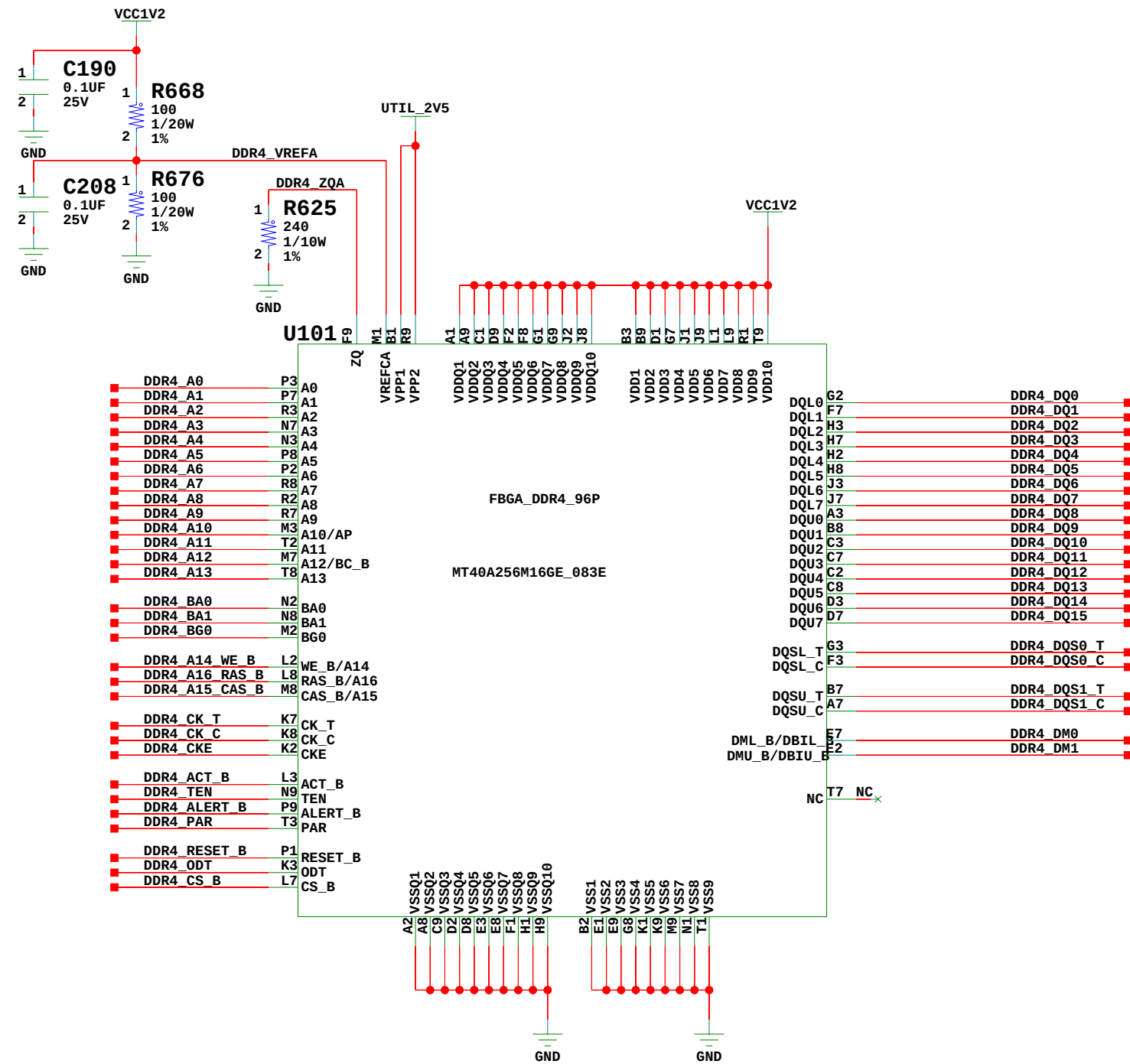
TITLE: PL DDR4 SODIMM 64 bit SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0	
ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:17	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 22 OF 58	DRAWN BY: BF



PLACE ABOVE CAPS BENEATH/CLOSE TO DIMM SOCKET

PL DDR4 SODIMM Decoupling

TITLE: PL DDR4 SODIMM Decoupling SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:17		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	23	OF	58
		DRAWN BY:	BF



PS Component DDR4 Data [15-0]



TITLE: PS Component DDR4 Data [15-0]
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:17

VER:	1.0
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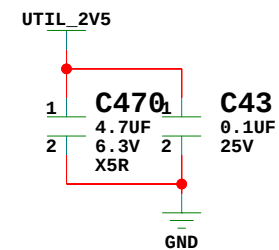
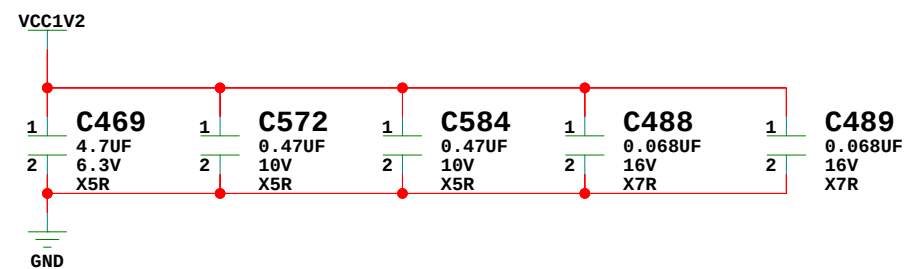
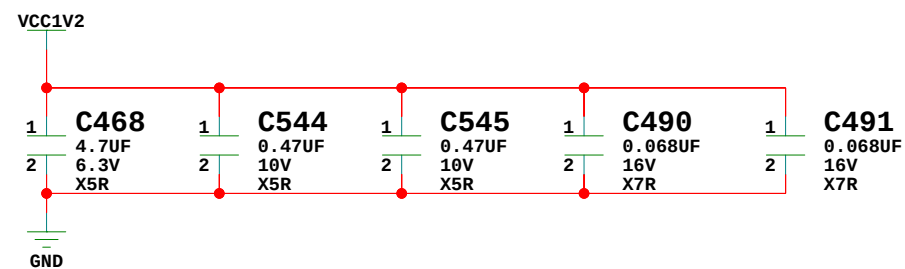
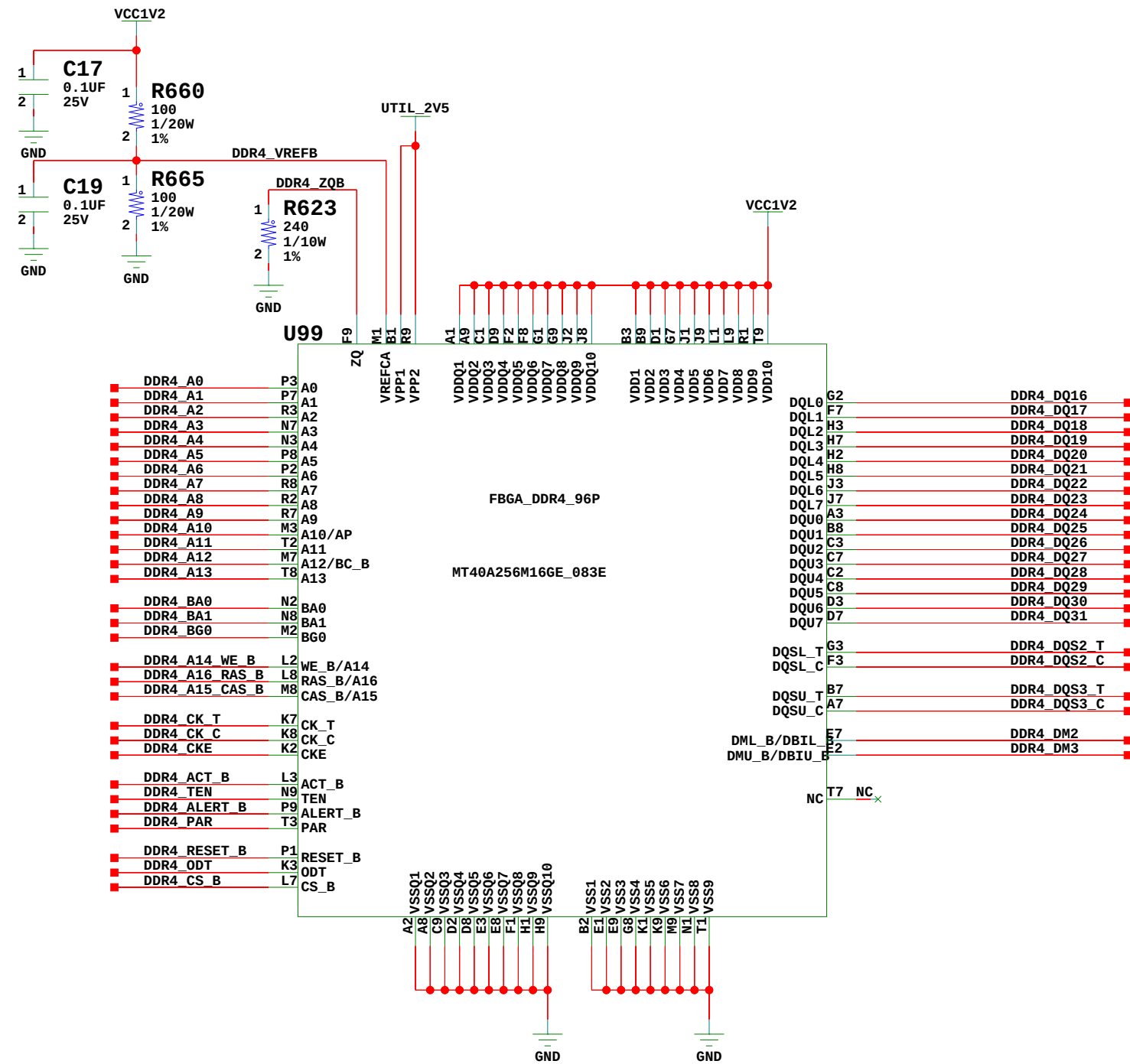
SHEET SIZE: B

REV: 01

SHEET **24** OF **58**

DRAWN BY:

BF



PS Component DDR4 Data [31-16]



TITLE: PS Component DDR4 Data [31-16]
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:17

VER:	1.0
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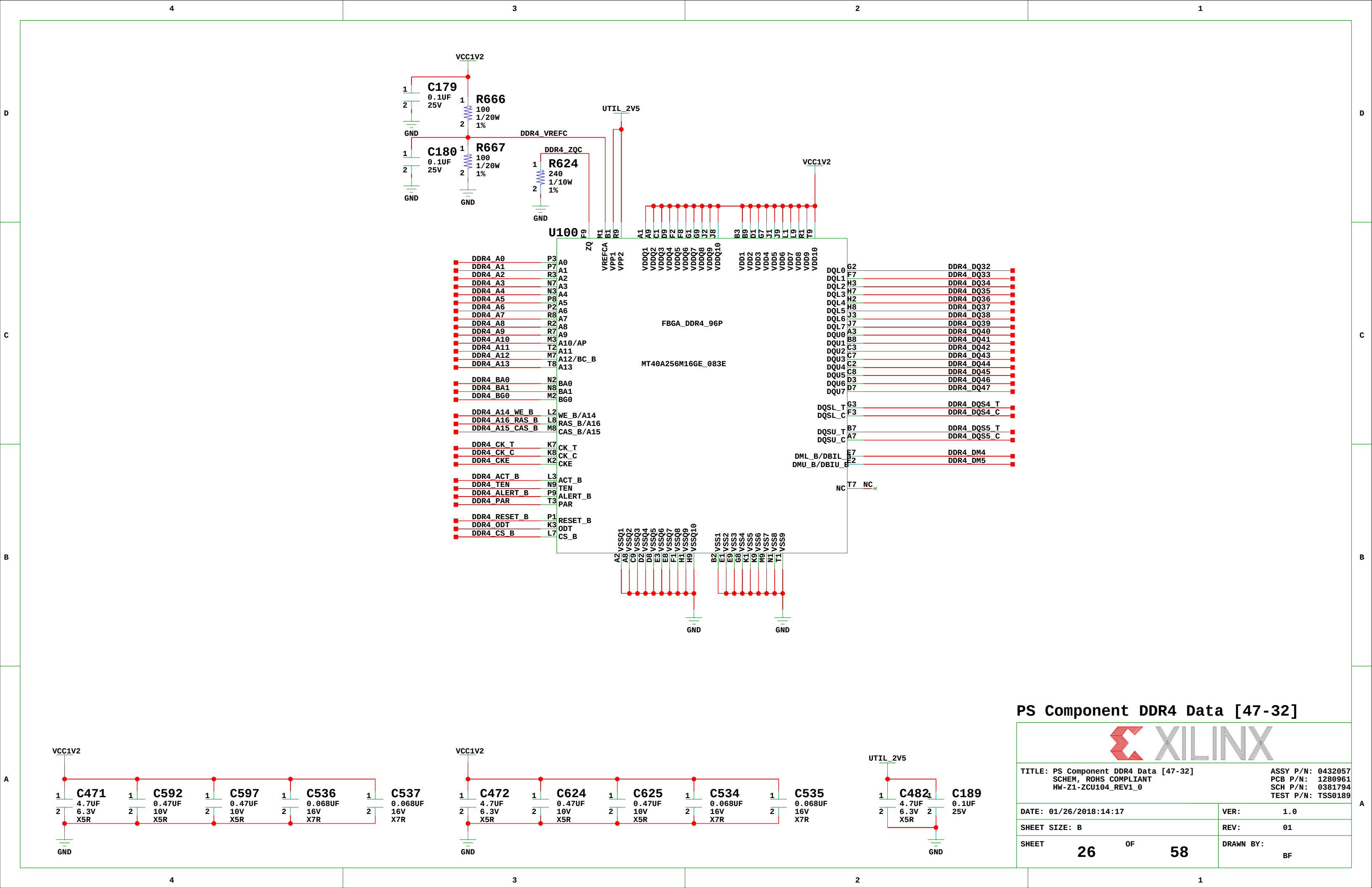
SHEET SIZE: B

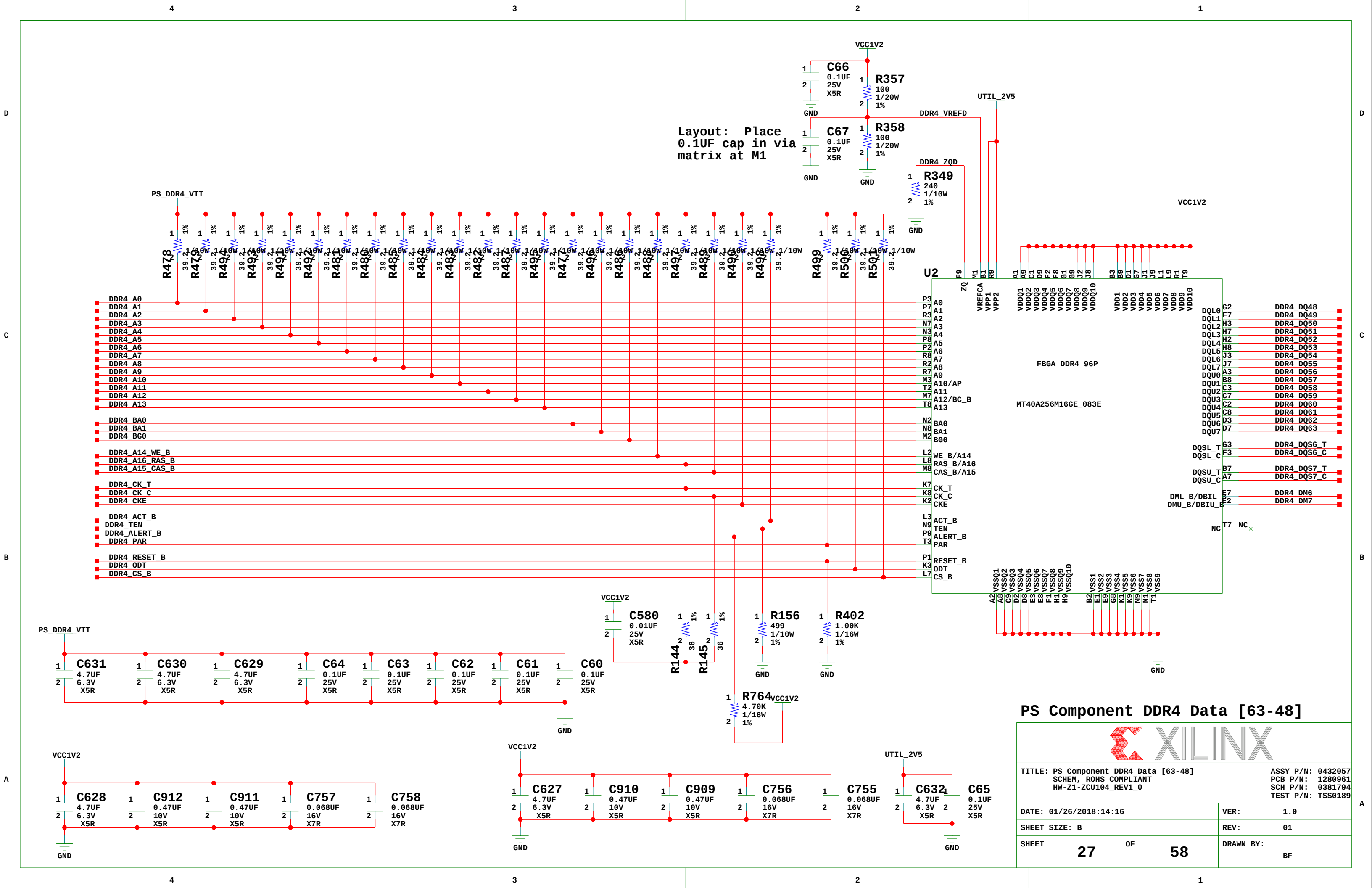
REV:	01
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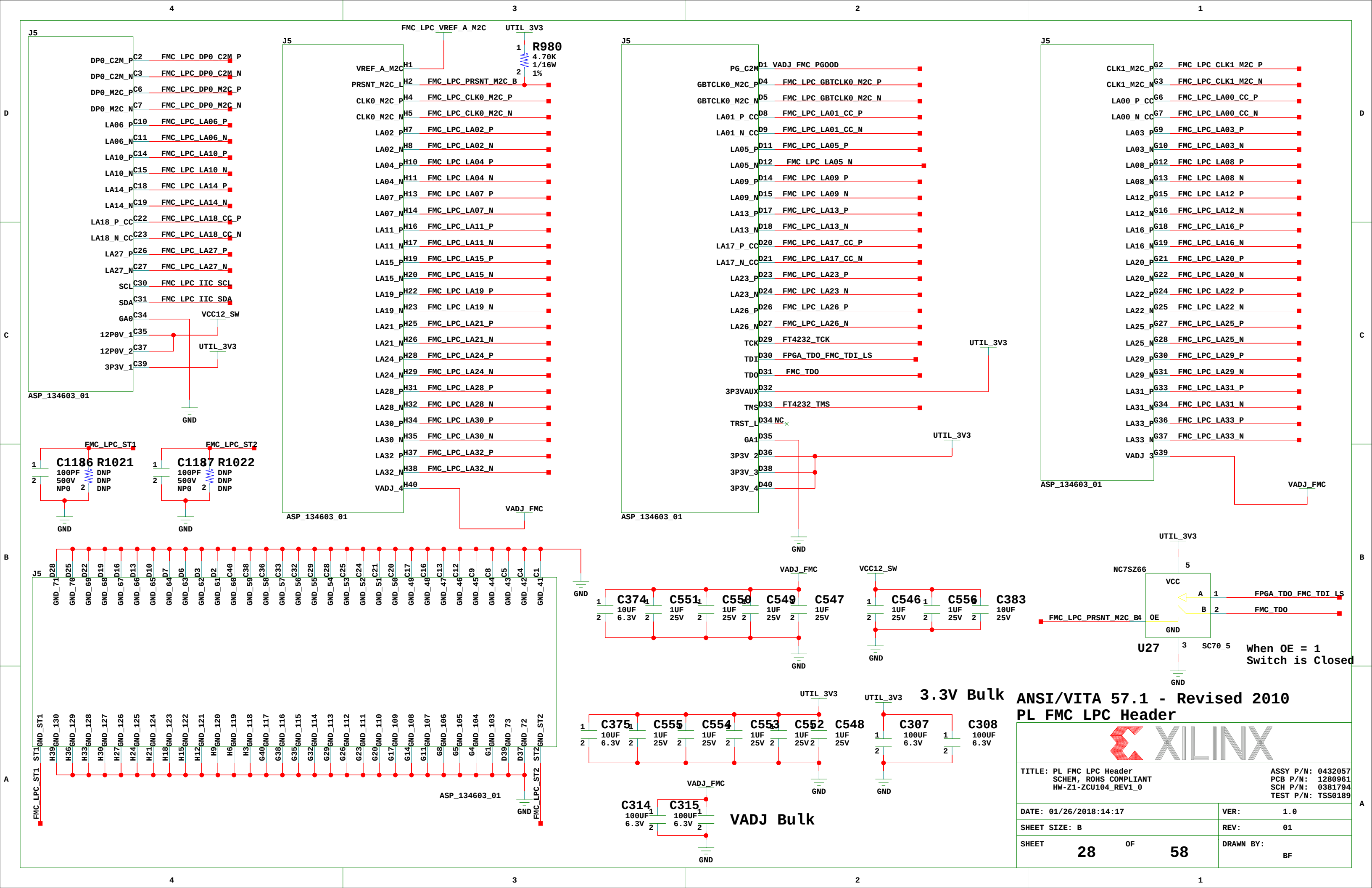
SHEET **25** OF **58**

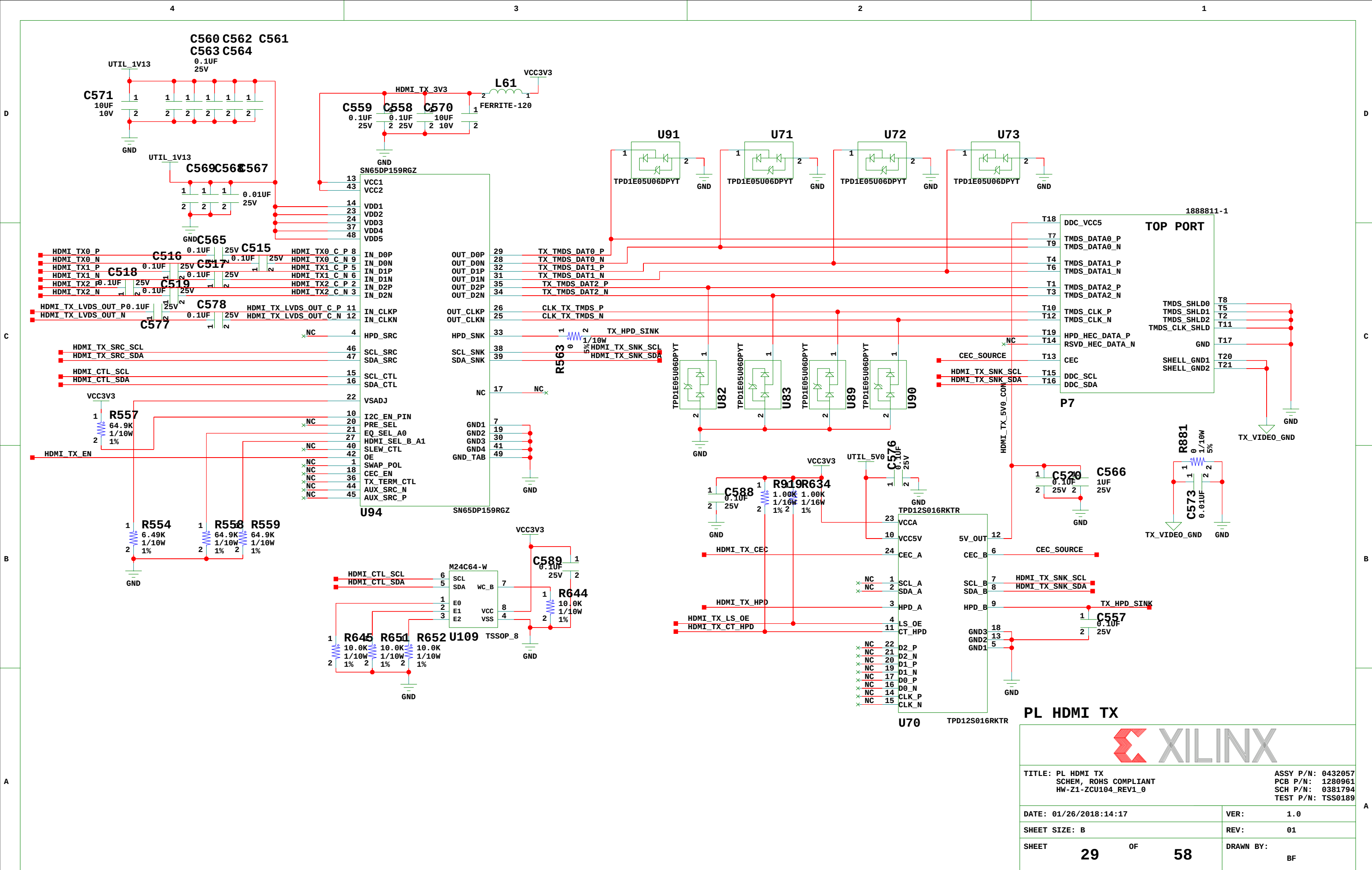
DRAWN BY:

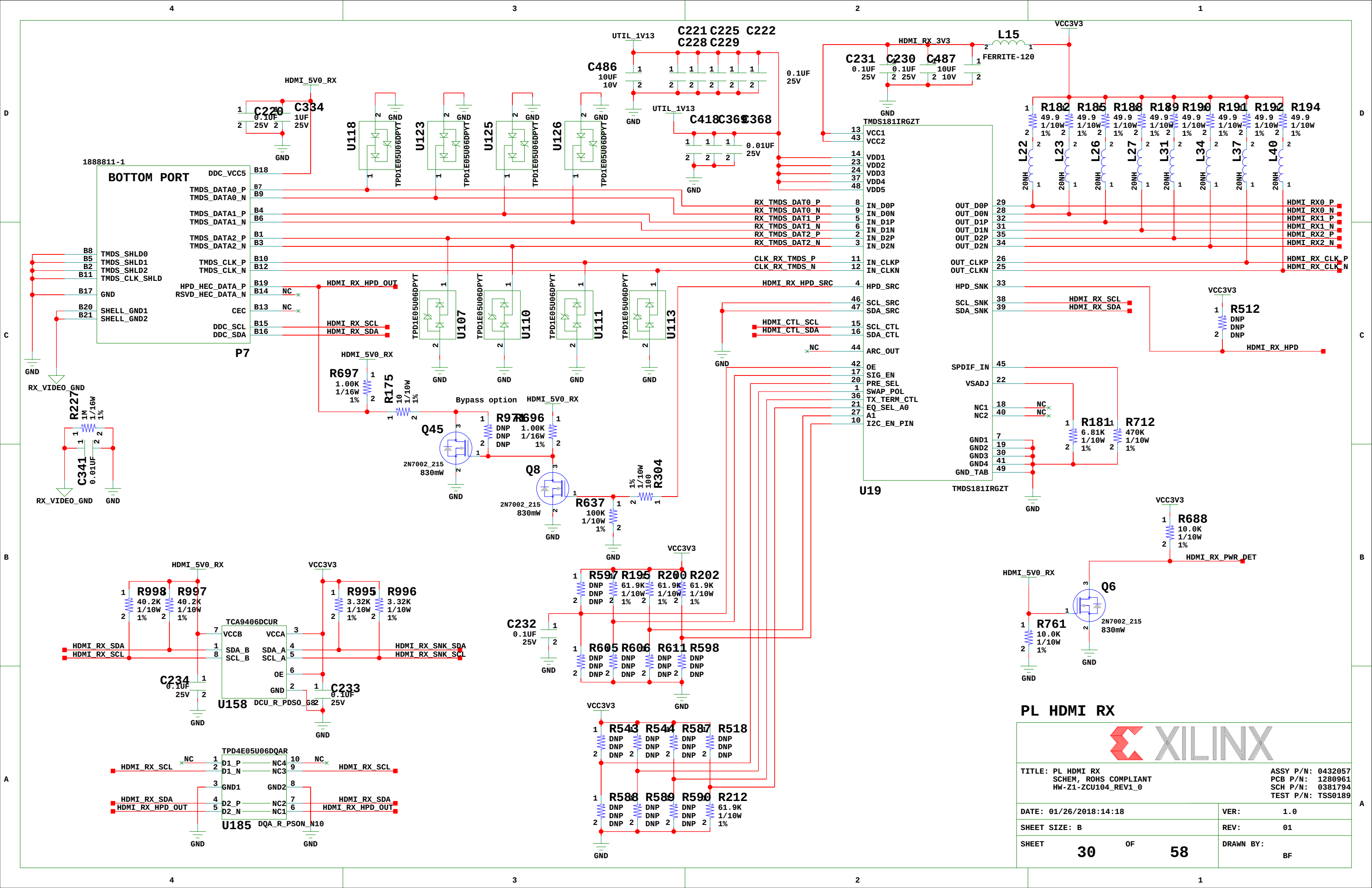
BF

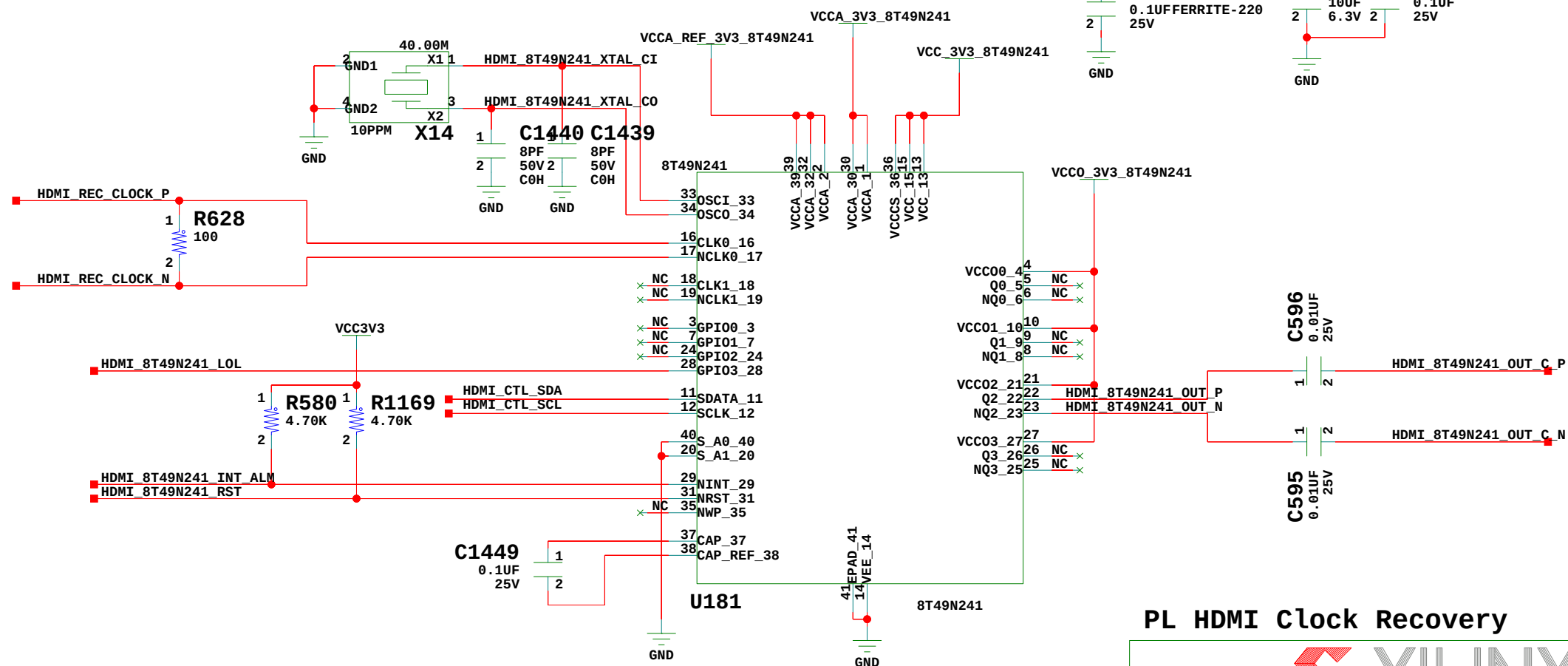
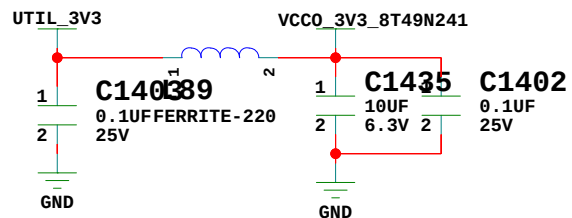
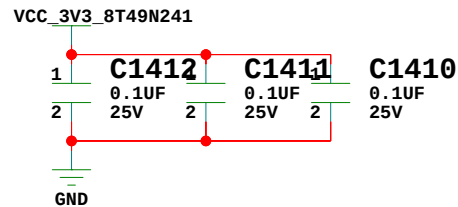
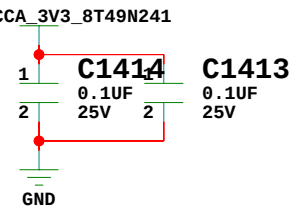
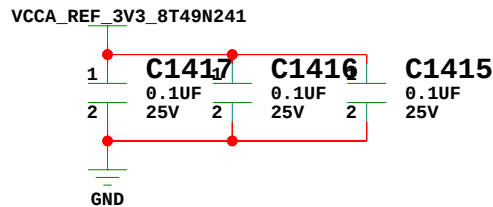
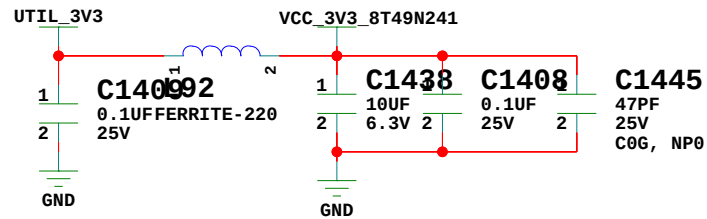
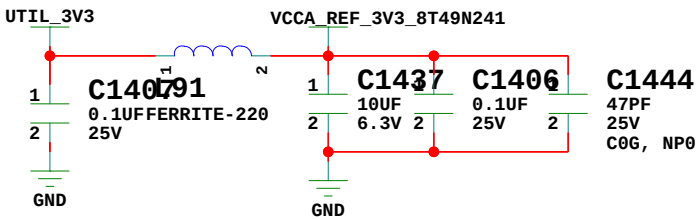
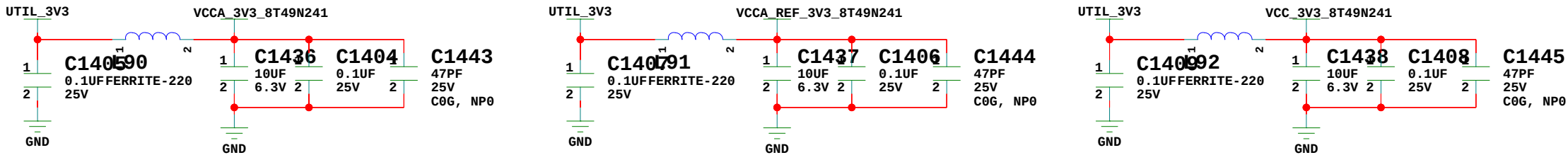












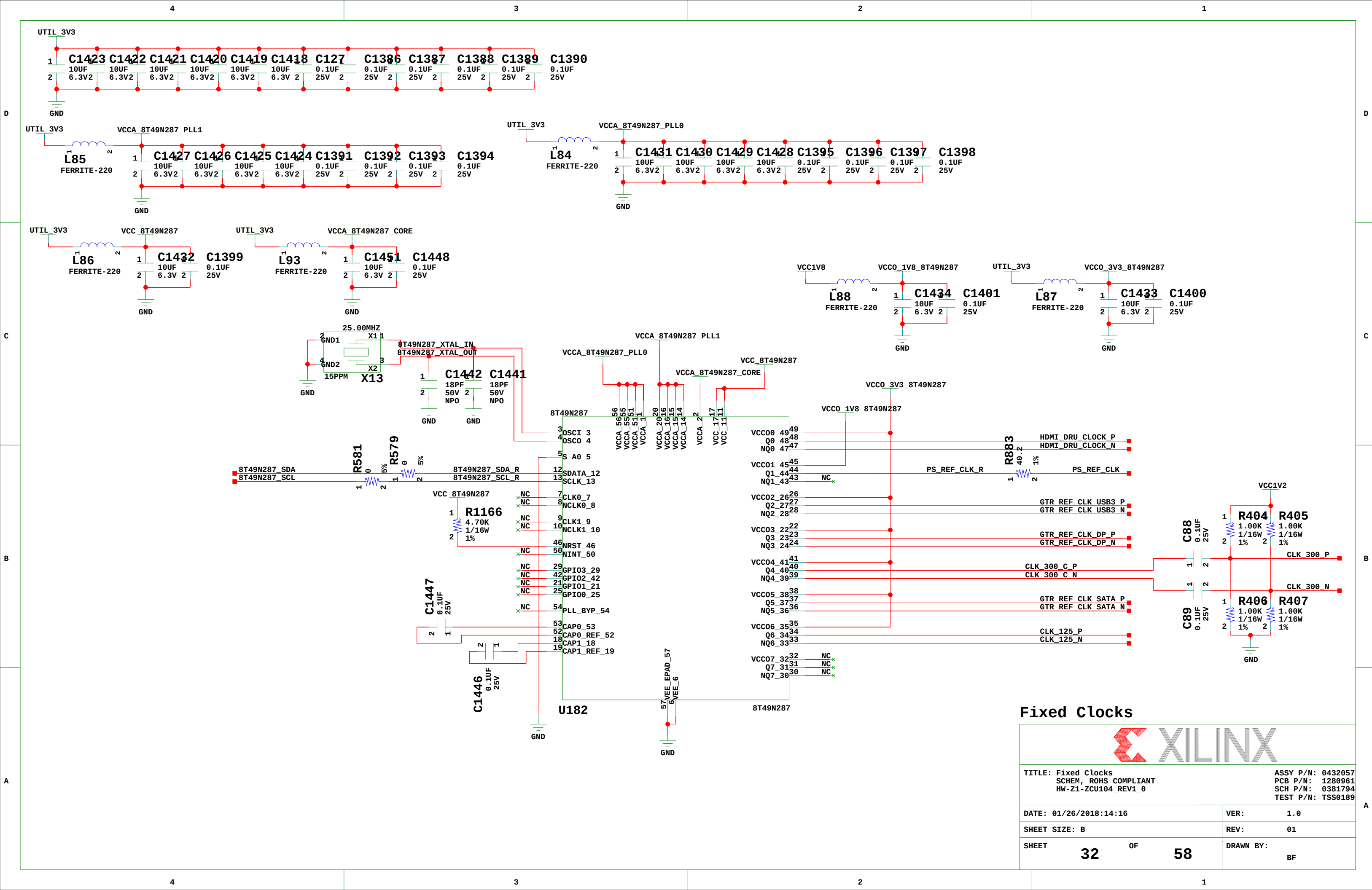
PL HDMI Clock Recovery

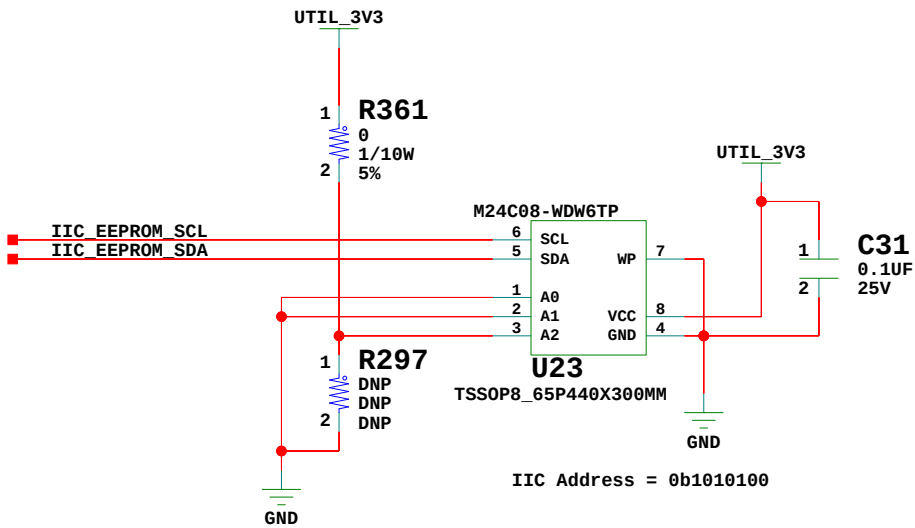


TITLE: PL HDMI Clock Recovery
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

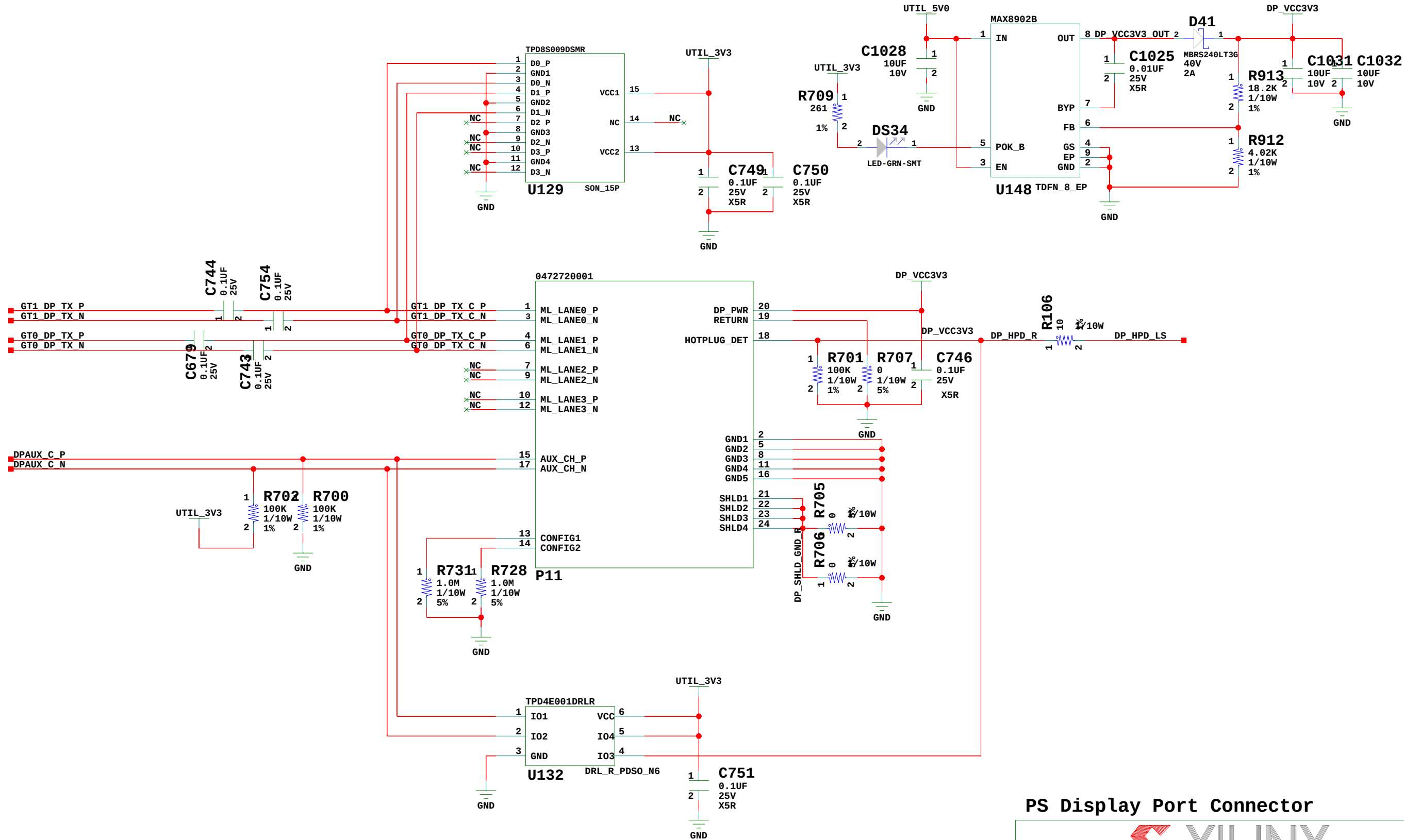
DATE: 01/26/2018:14:21	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 31 OF 58	DRAWN BY: BF





EEPROM

TITLE: EEPROM SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	33	OF	58
		DRAWN BY:	BF

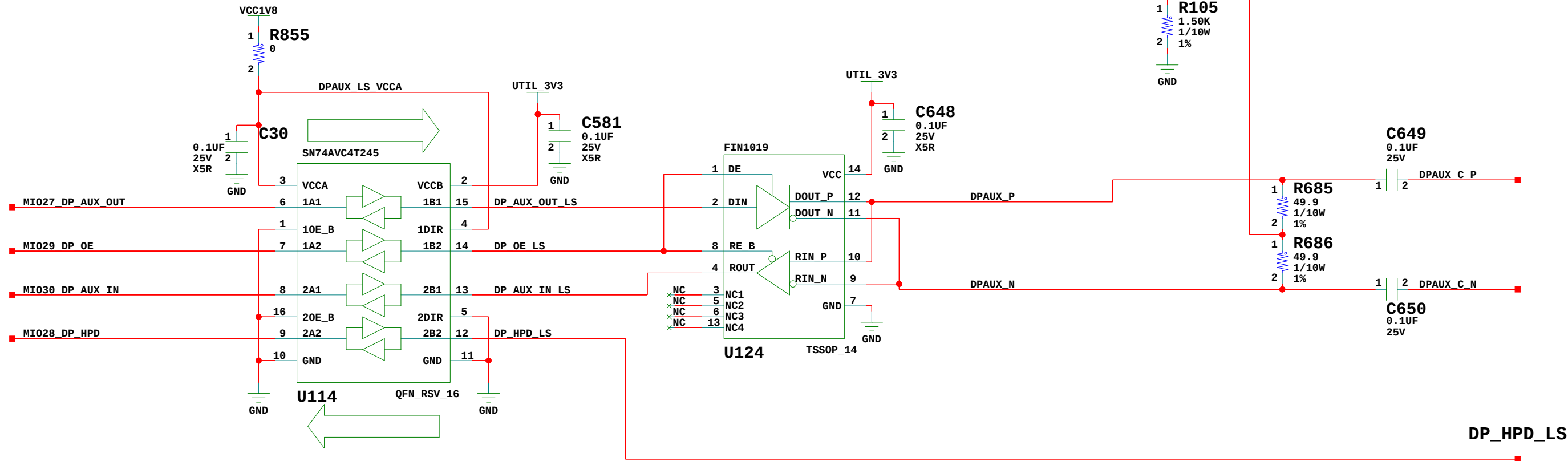


PS Display Port Connector



TITLE: PS Display Port Connector SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0	ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189
--	--

DATE: 01/26/2018:14:17	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 34 OF 58	DRAWN BY: BF



PS Display Port IO



TITLE: PS Display Port IO
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:17

VER: 1.0

SHEET SIZE: B

REV: 01

SHEET

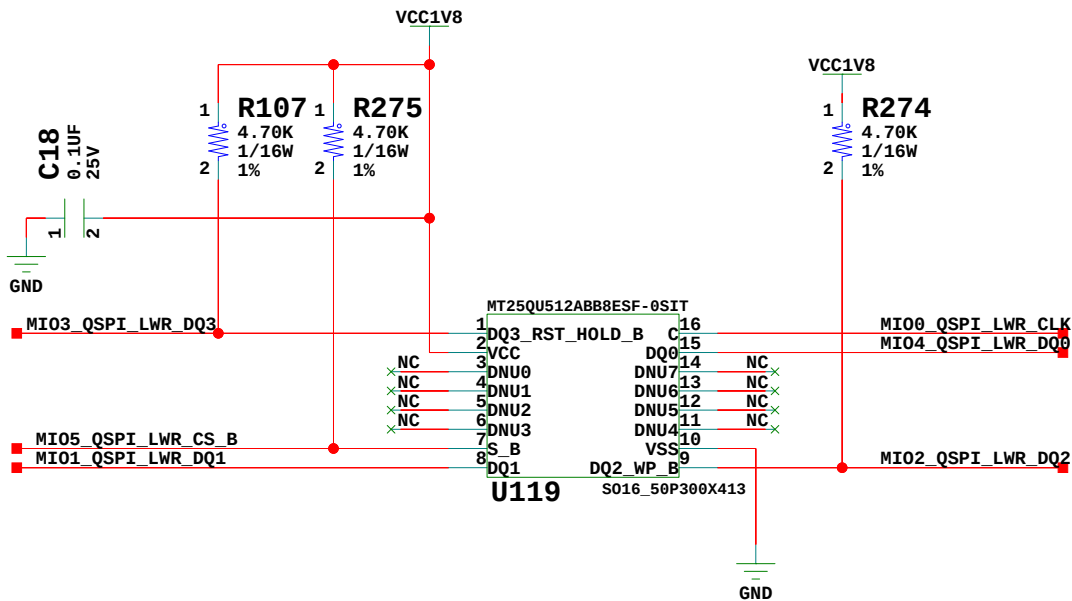
35

OF

58

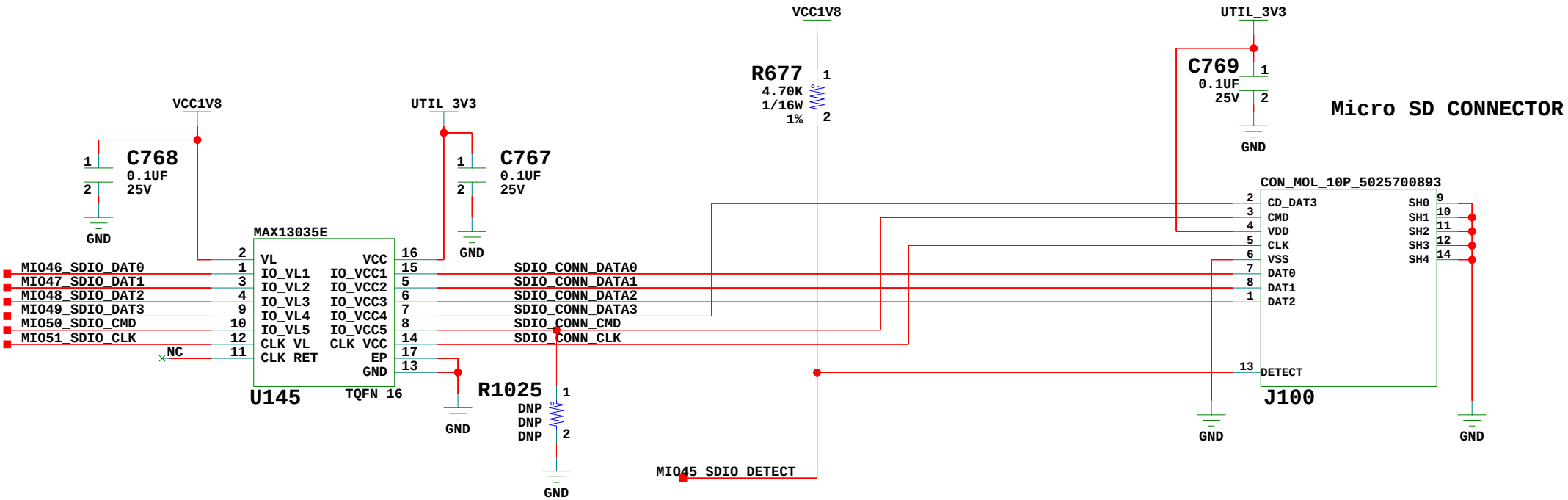
DRAWN BY:

BF



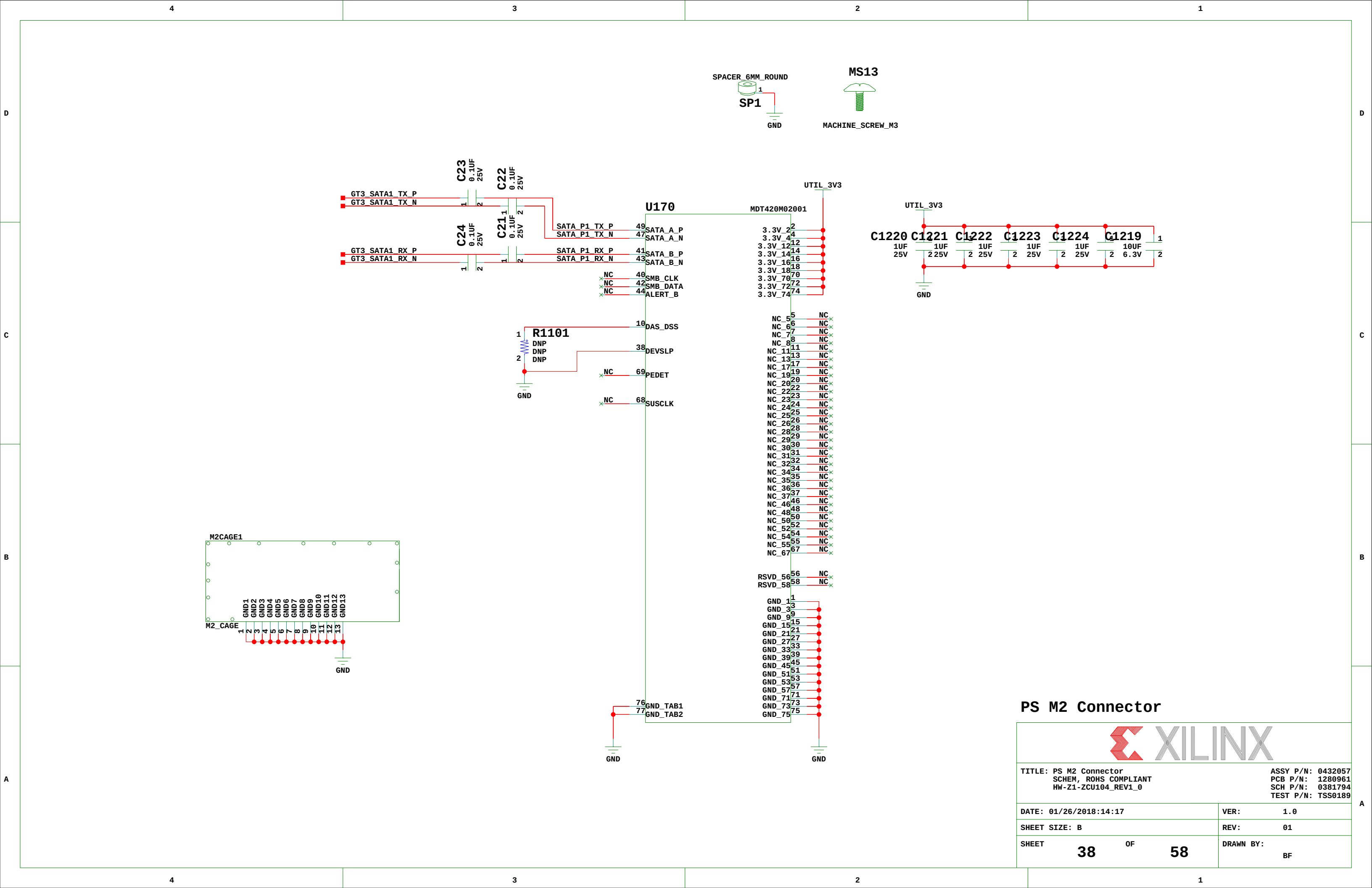
PS QSPI

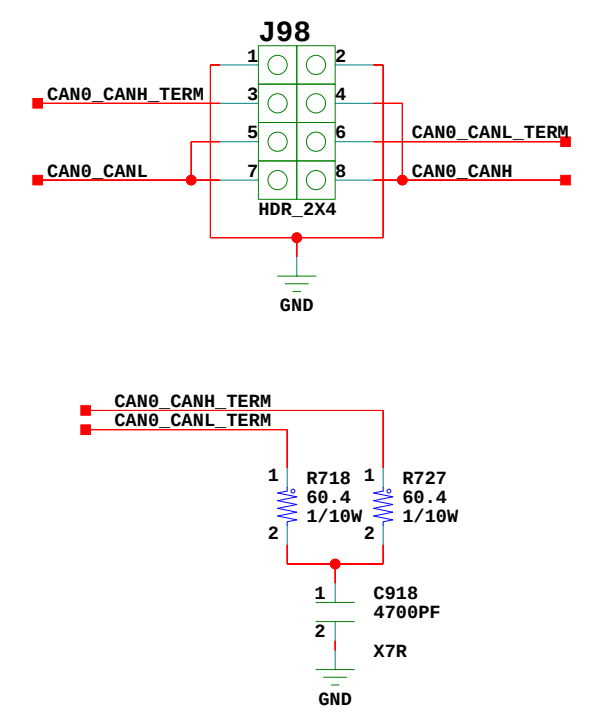
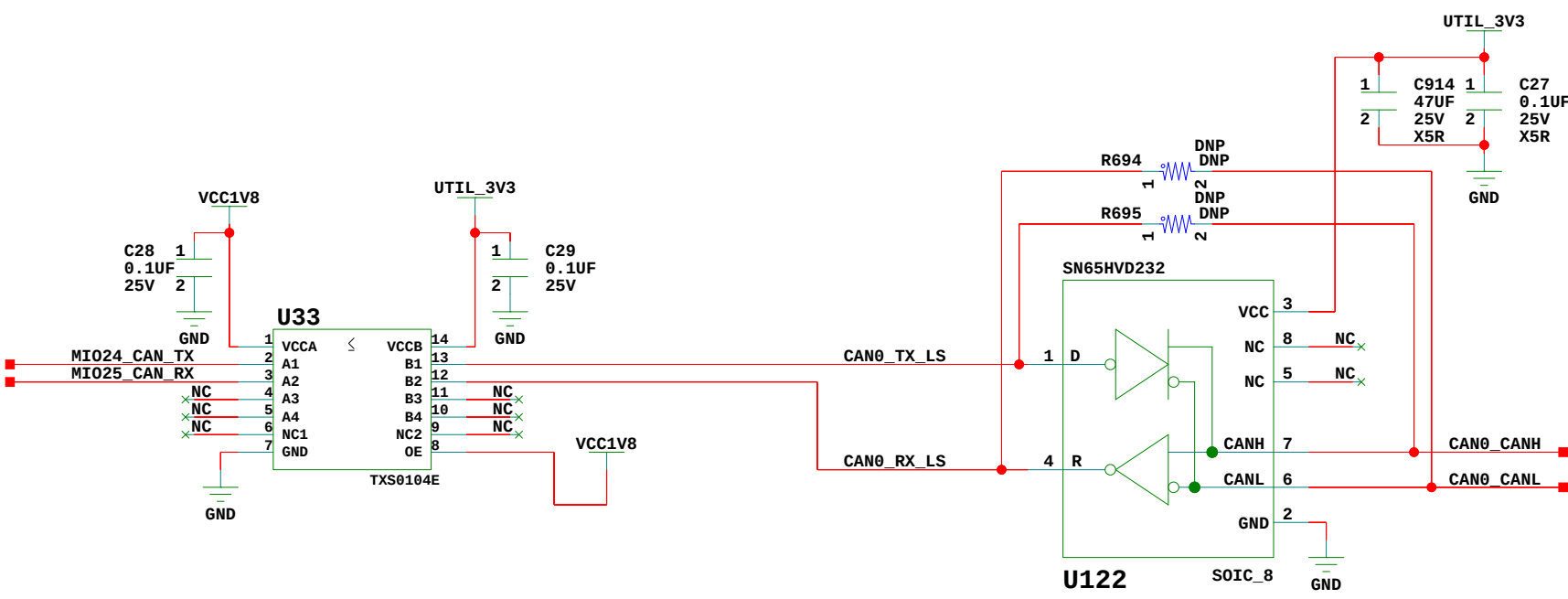
TITLE: PS QSPI SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:17		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	36	OF	58
		DRAWN BY:	BF



PS SD Card Connector

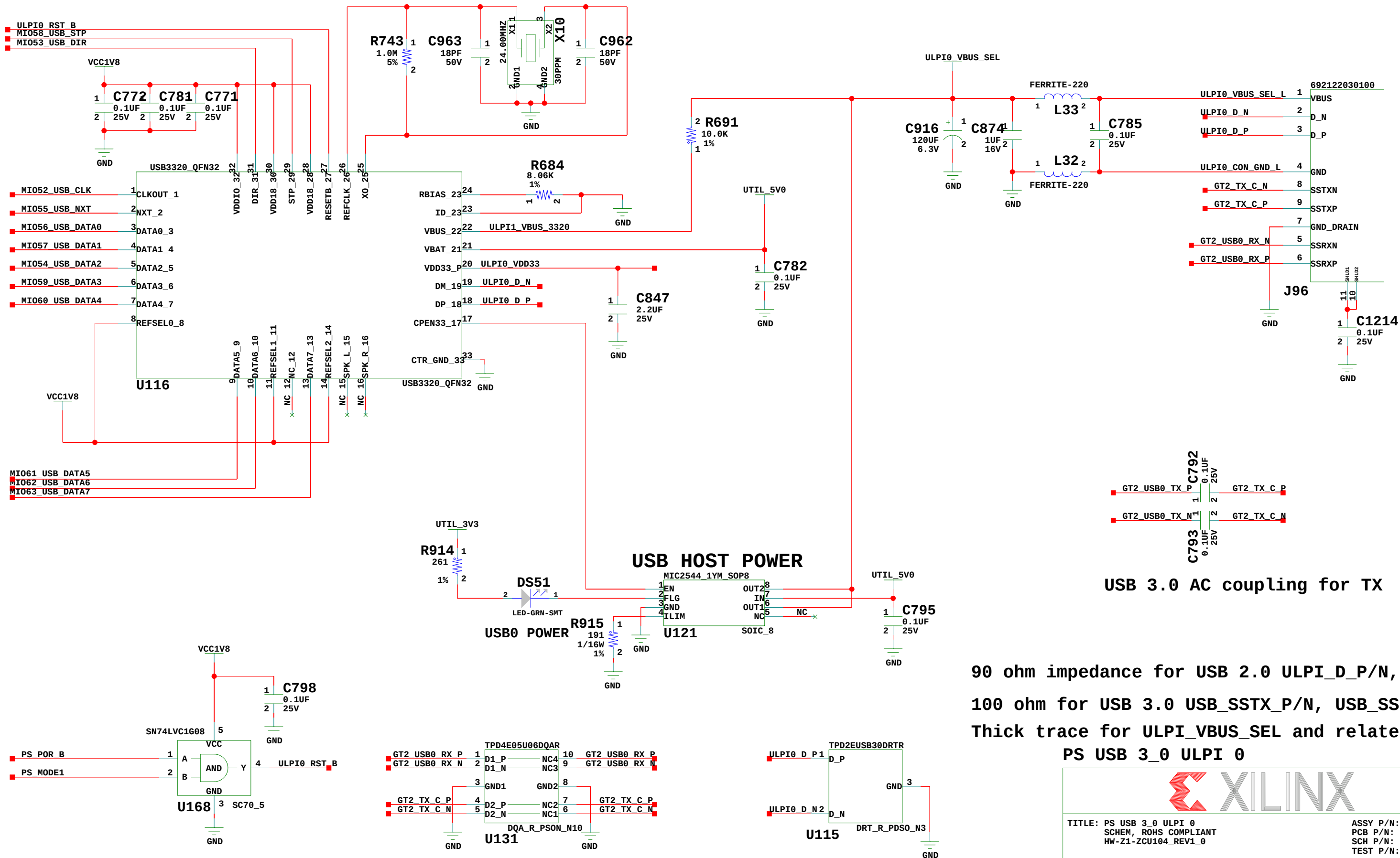
TITLE: PS SD Card Connector SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:17		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	37	OF	58
		DRAWN BY:	BF





PS CAN Bus

TITLE: PS CAN Bus SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:17		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	39	OF	58
DRAWN BY:		BF	



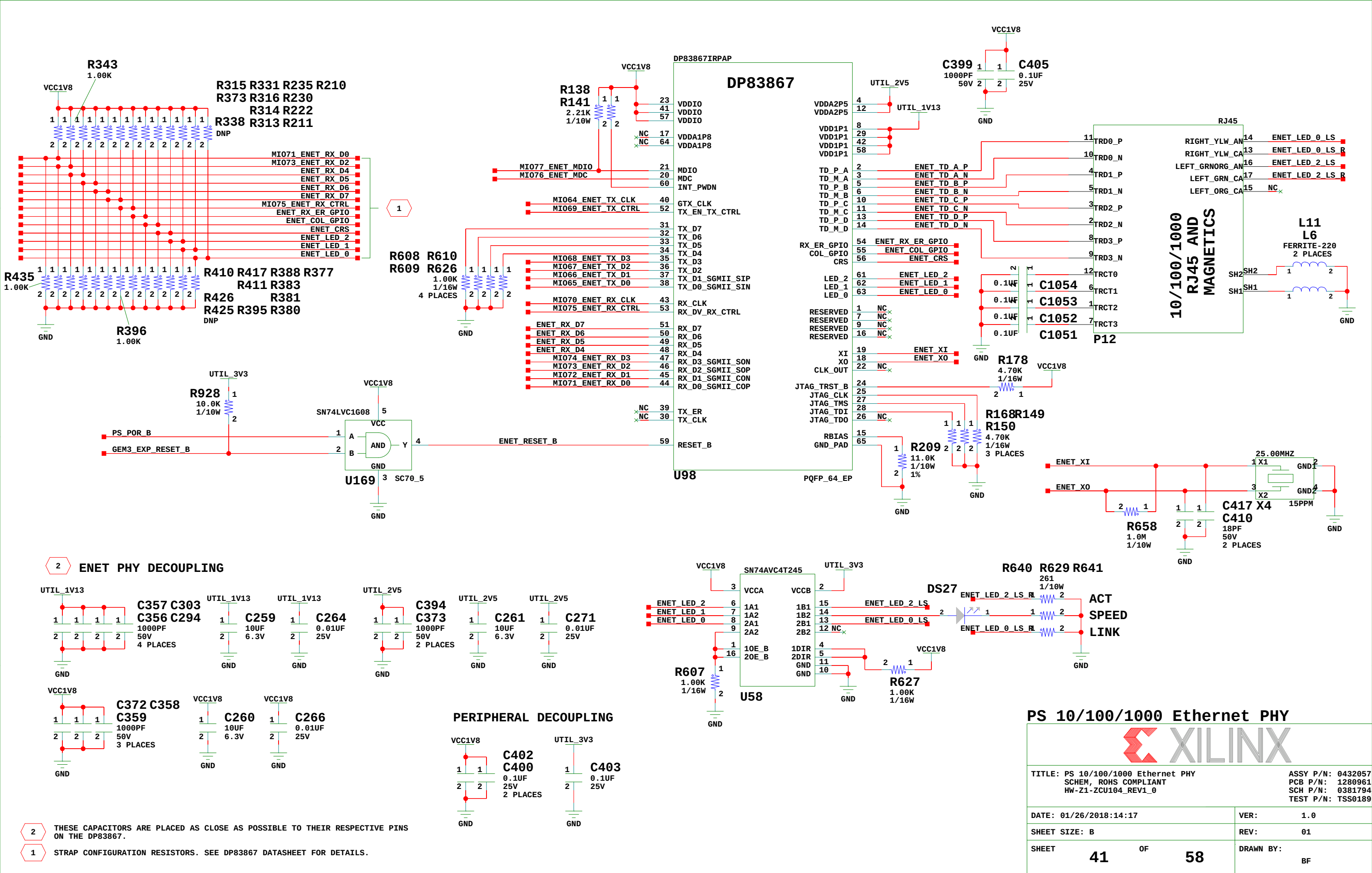
USB 3.0 AC coupling for TX

90 ohm impedance for USB 2.0 ULPI_D_P/N,
100 ohm for USB 3.0 USB_SSTX_P/N, USB_SSRX_P/N
Thick trace for ULPI_VBUS_SEL and related nets
PS USB 3_0 ULPI 0



TITLE: PS USB 3_0 ULPI 0
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0
ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

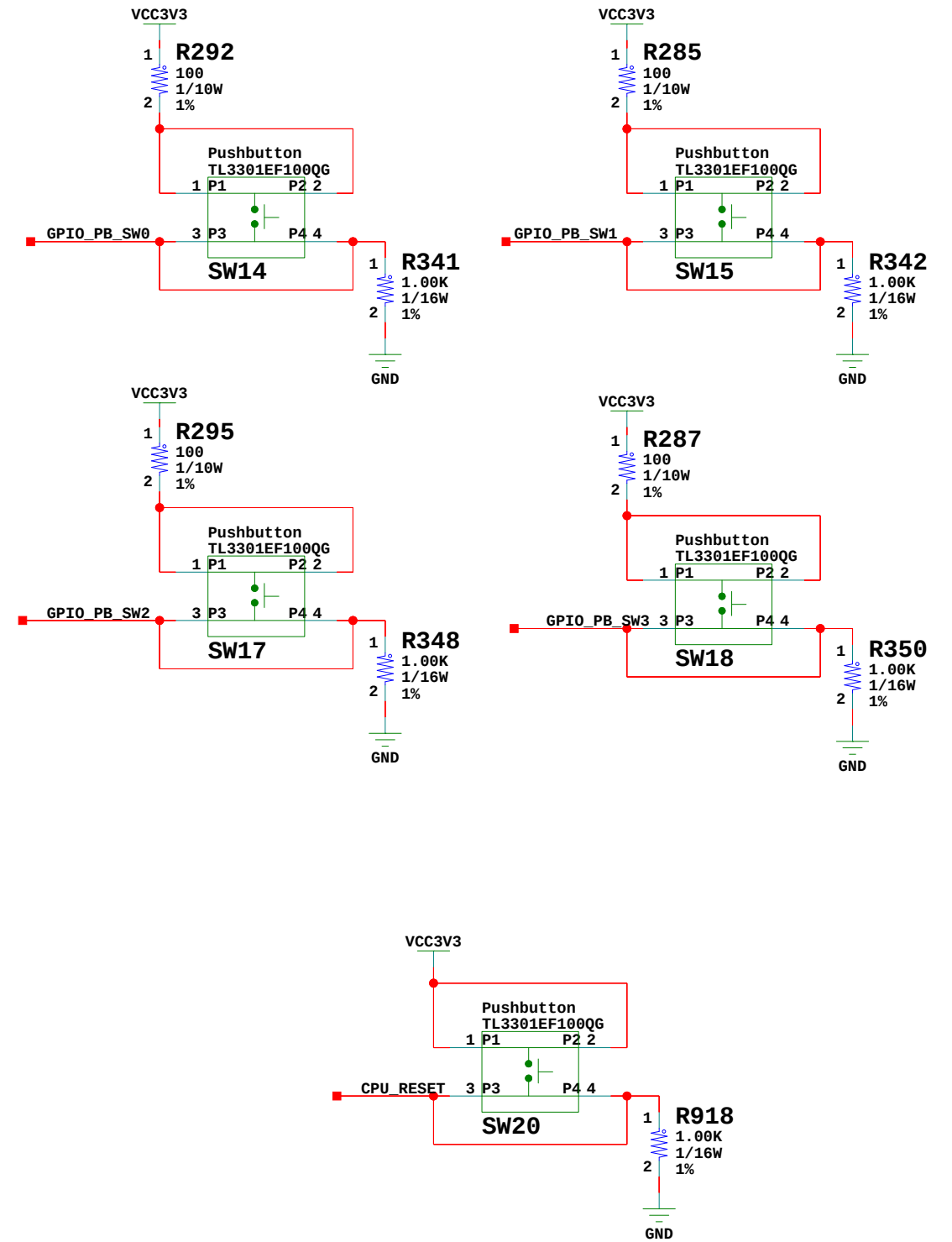
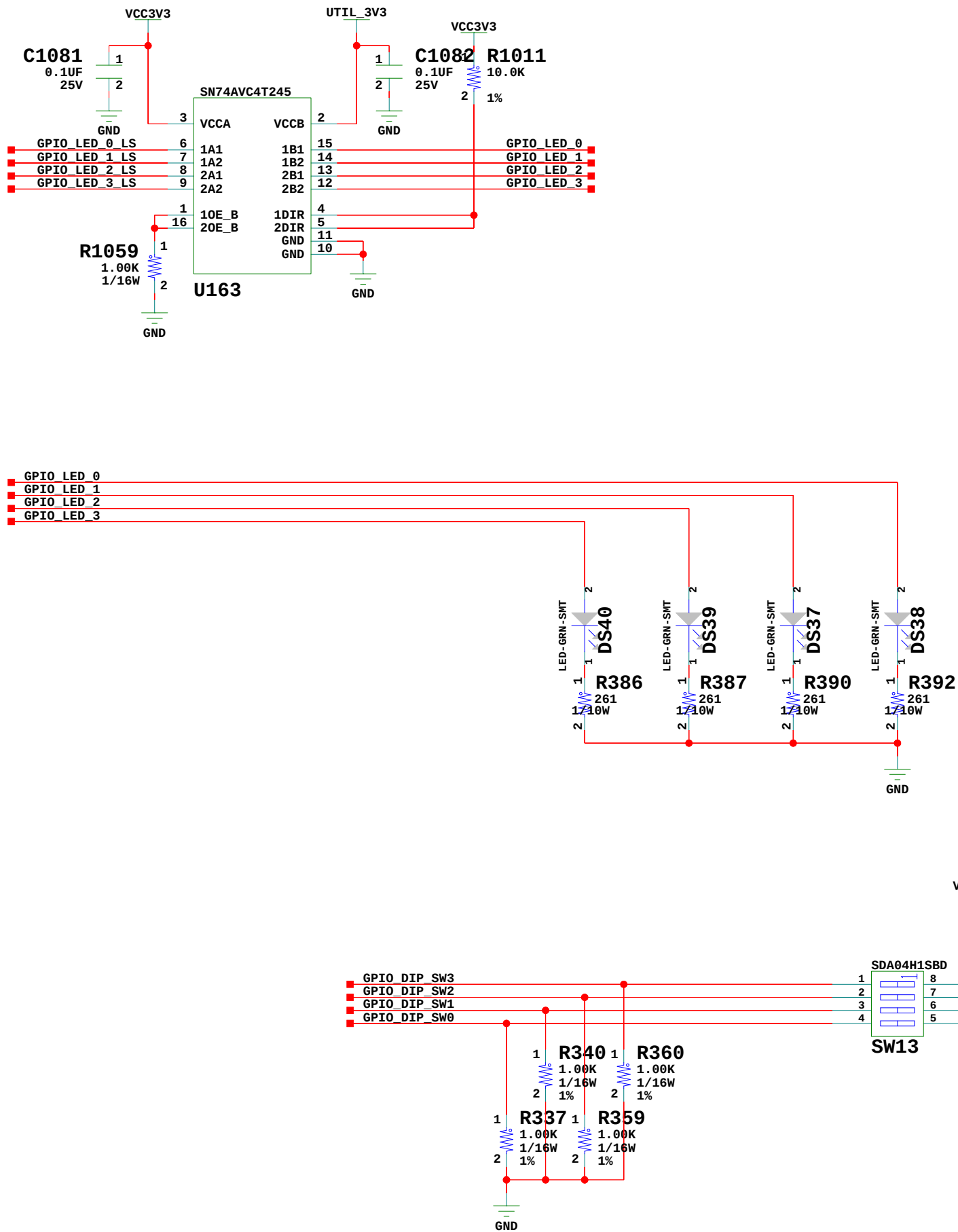
DATE: 01/26/2018:14:17	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 40 OF 58	DRAWN BY: BF



2 THESE CAPACITORS ARE PLACED AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE PINS ON THE DP83867.

1 STRAP CONFIGURATION RESISTORS. SEE DP83867 DATASHEET FOR DETAILS.

PS 10/100/1000 Ethernet PHY			
TITLE: PS 10/100/1000 Ethernet PHY SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:17		VER: 1.0	
SHEET SIZE: B		REV: 01	
SHEET 41 OF 58		DRAWN BY: BF	



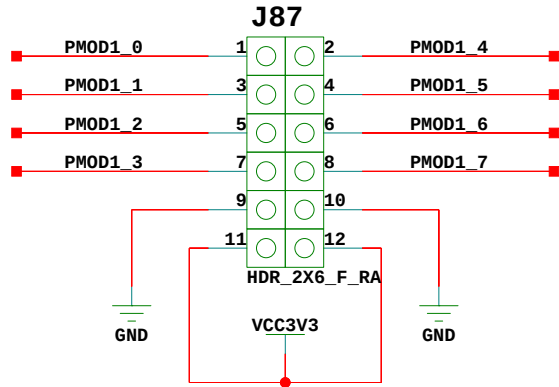
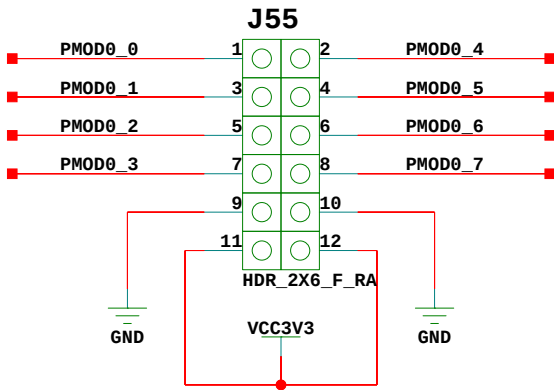
PL Buttons - Switches - LEDs



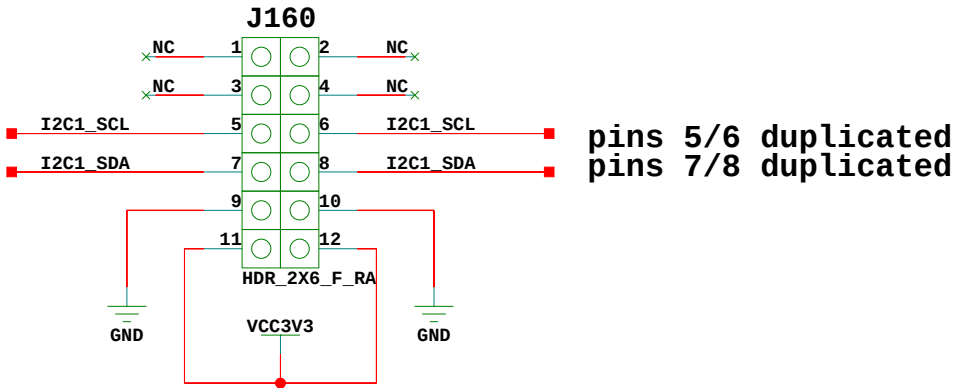
TITLE: PL Buttons - Switches - LEDs
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

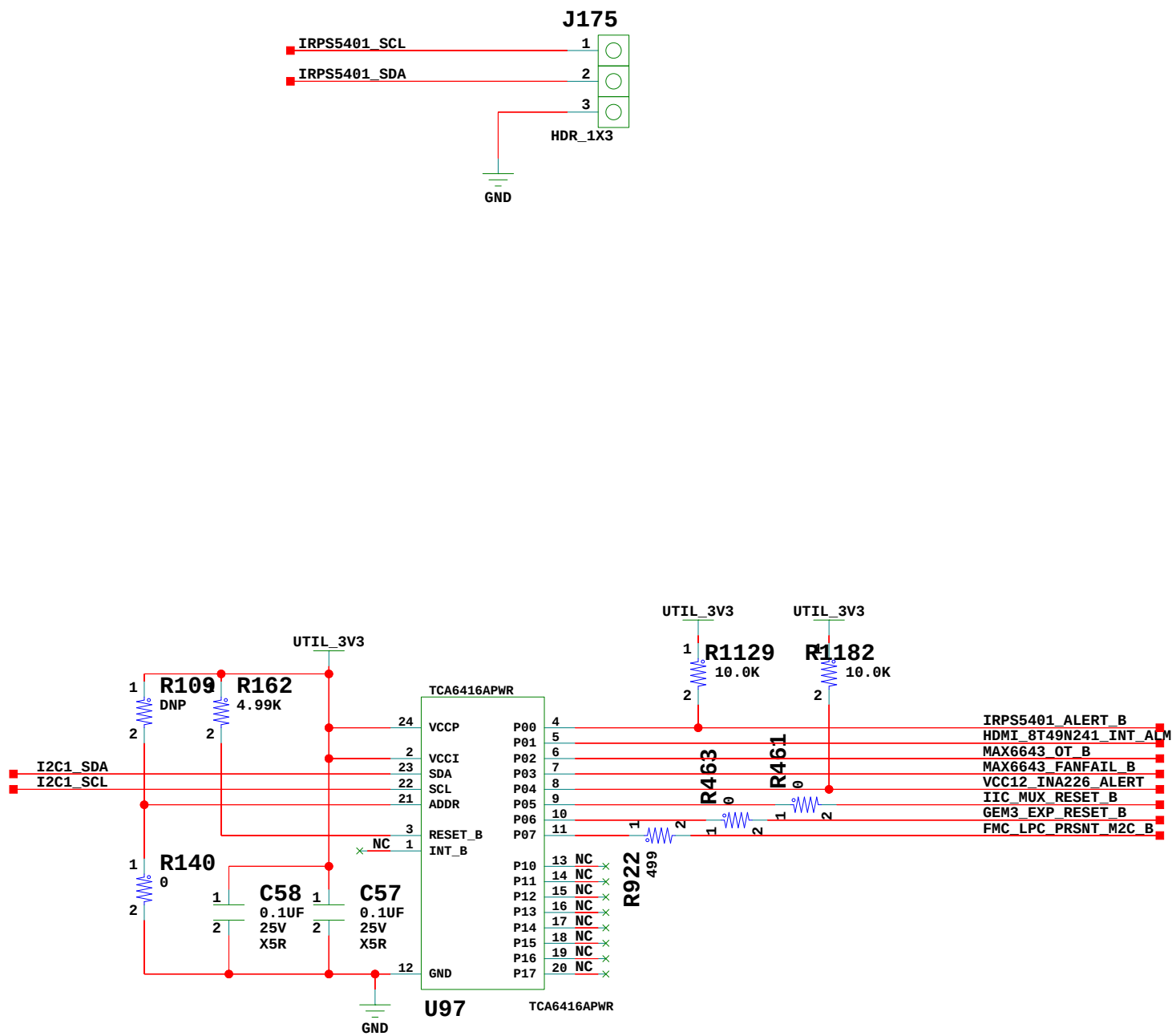
DATE: 01/26/2018:14:17	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 42 OF 58	DRAWN BY: BF



Connects I2C to R.A. Female 2x6 PMOD-style receptacle

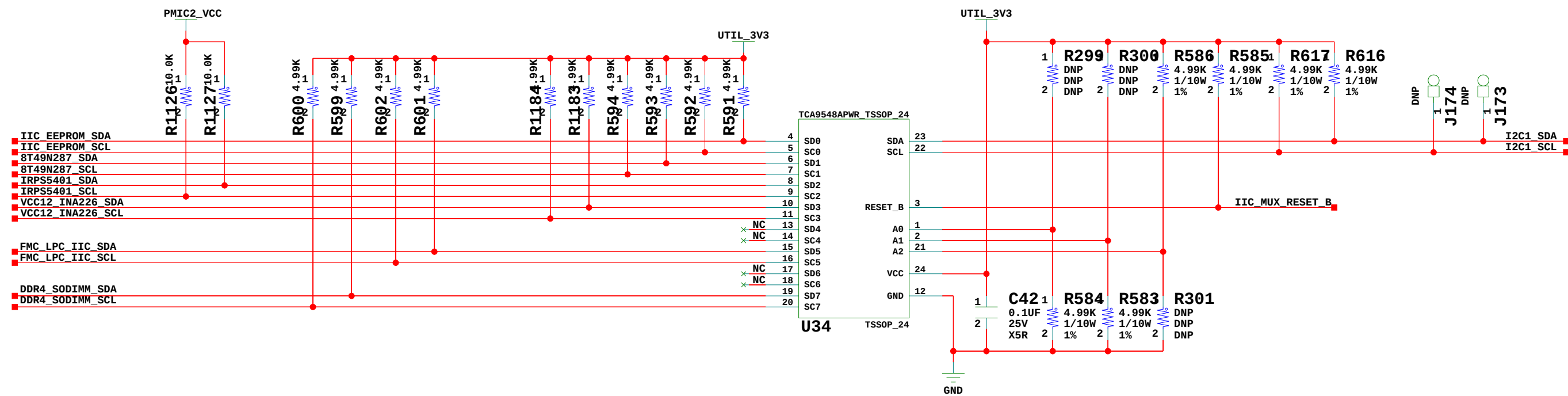


TITLE: PL PMODs SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:17		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	43	OF	58
DRAWN BY:		BF	

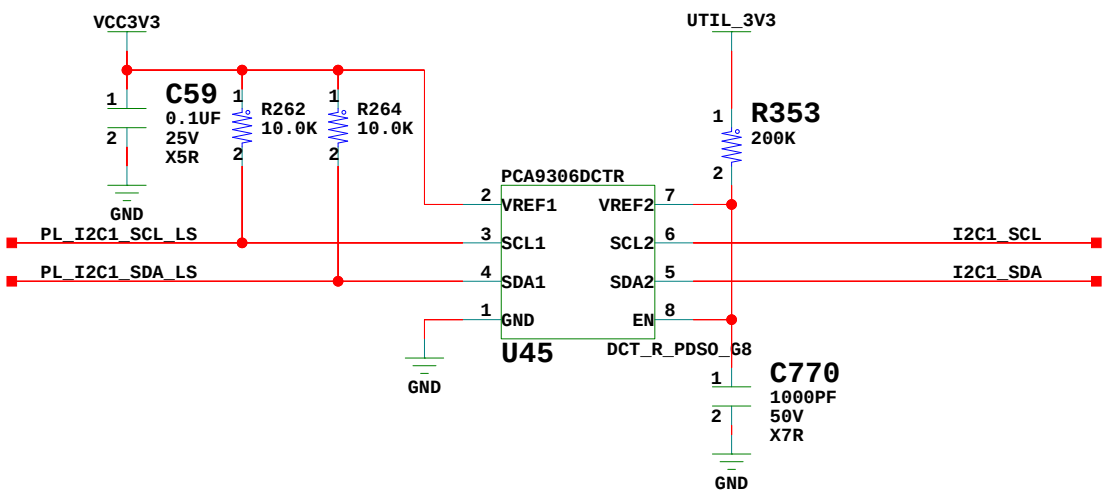


IO Expander PMBUS Header

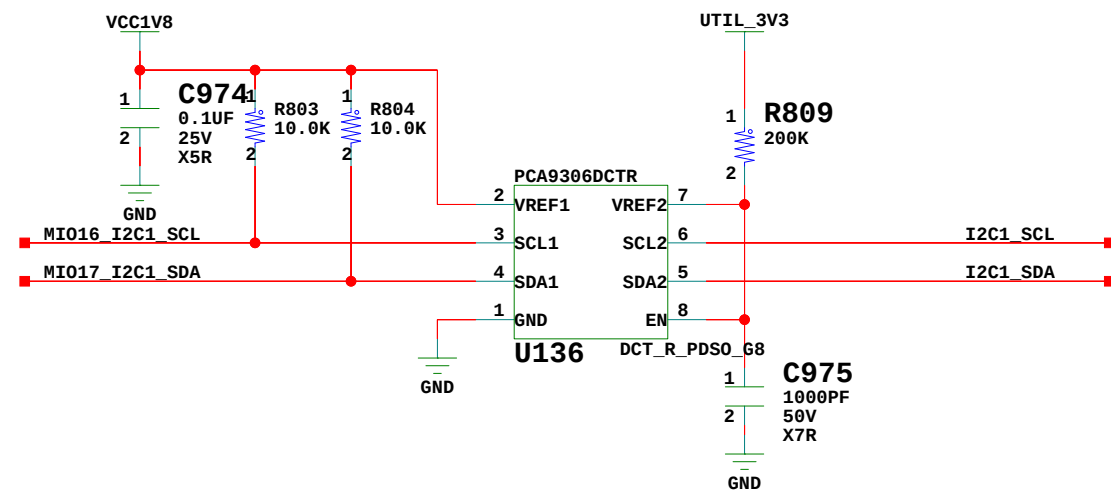
TITLE: IO Expander PMBUS Header SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	44	OF	58
DRAWN BY:		BF	



PL I2C Level Shifter (disabled if VREF1 is off)



PS I2C Level Shifter (I2C1)



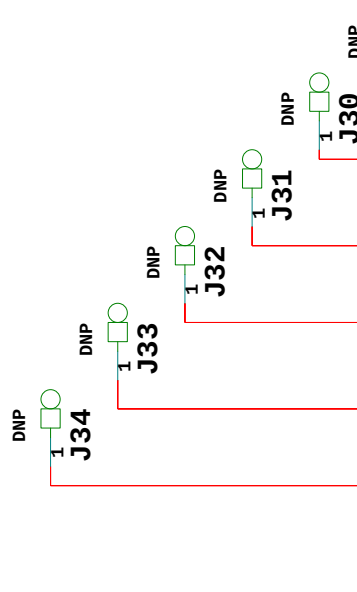
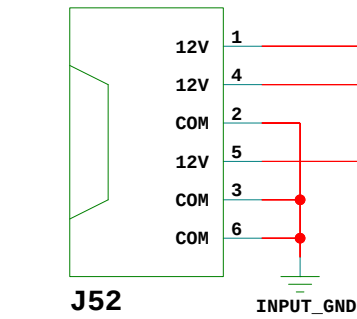
I2C1 MUX and Level Shifters

TITLE: I2C1 MUX and Level Shifters
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

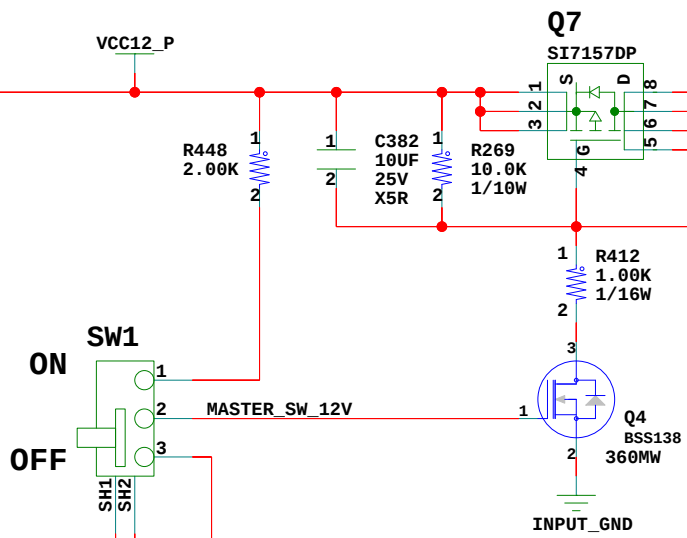
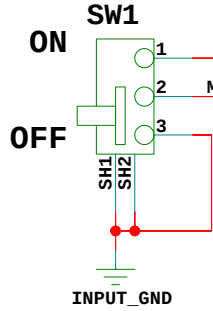
ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 45 OF 58	DRAWN BY: BF

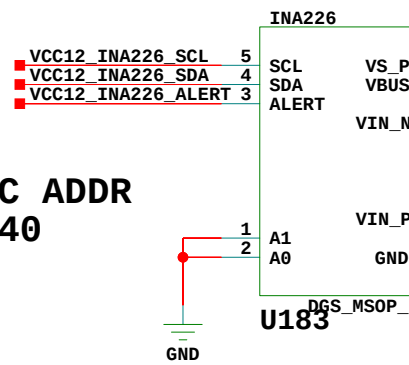
6-PIN MINI-FIT
AC ADAPTER (BRICK)



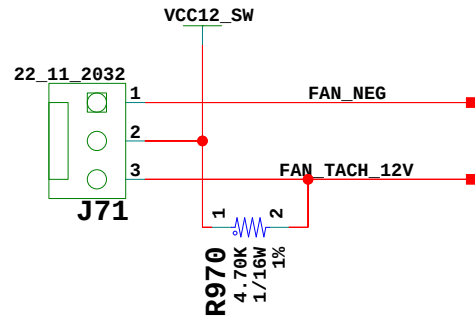
GND Test points



I2C ADDR
0x40



Keyed Fan Header



12V Power Connectors Switch

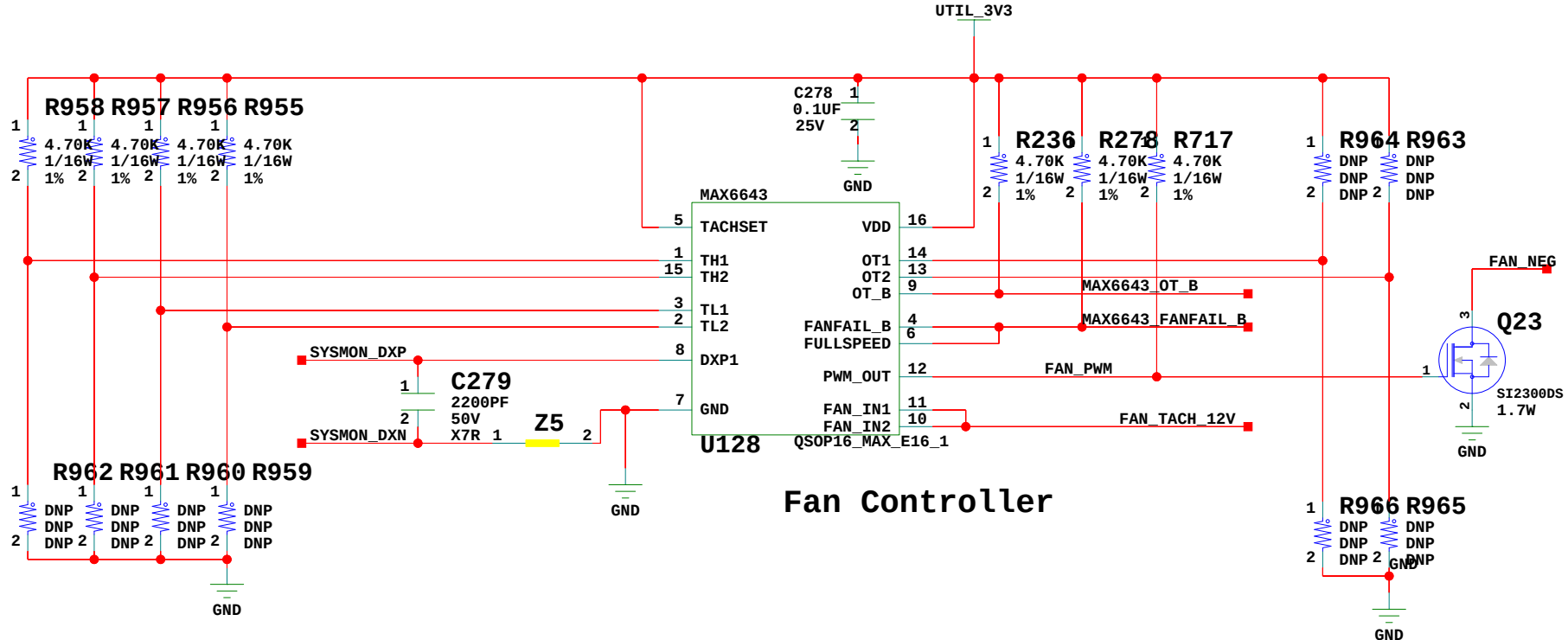


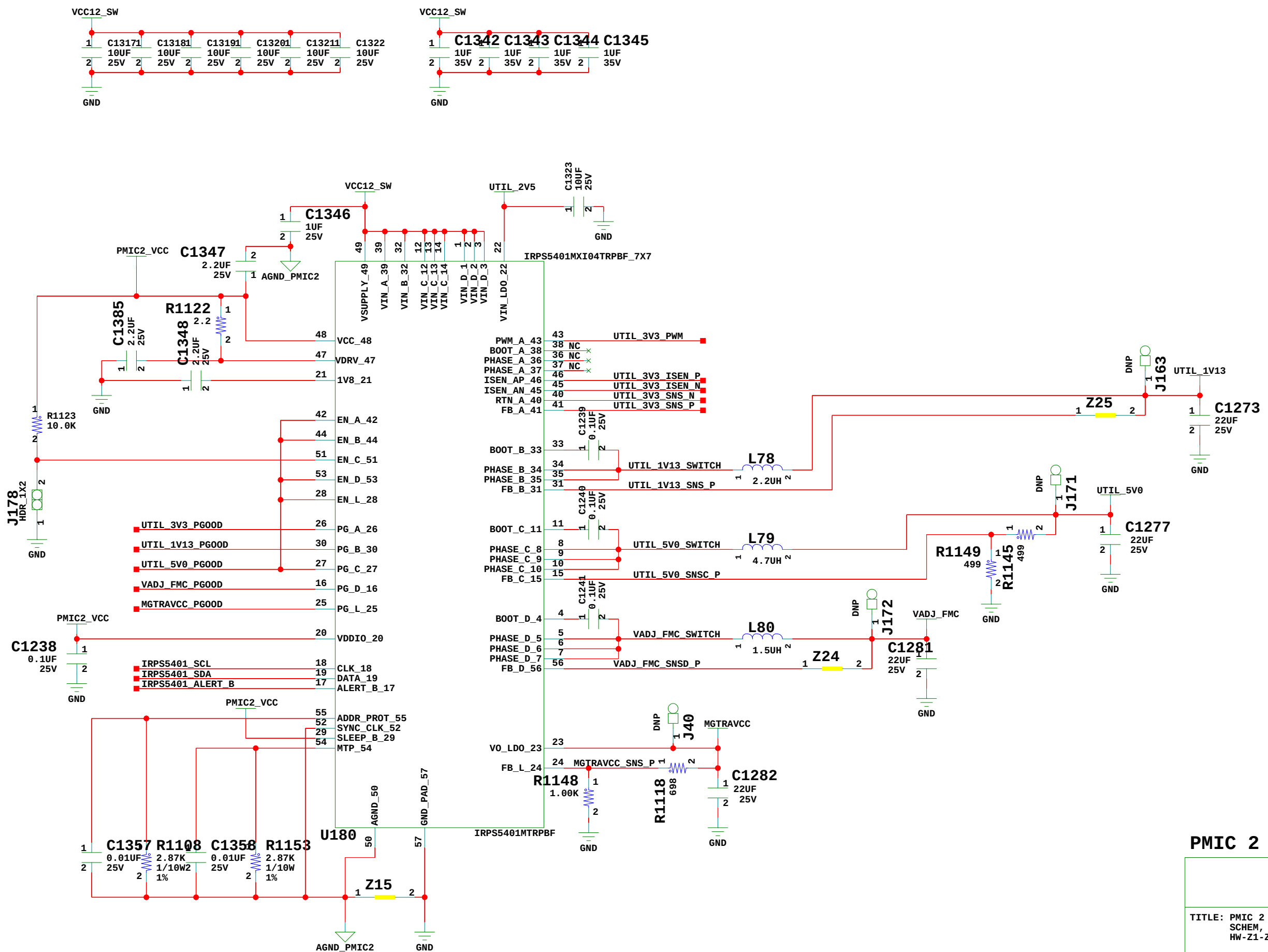
TITLE: 12V Power Connectors Switch
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 46 OF 58	DRAWN BY: BF

Fan Controller





7-BIT PMBUS ADDR: 0x44
I2C ADDR: 0x14

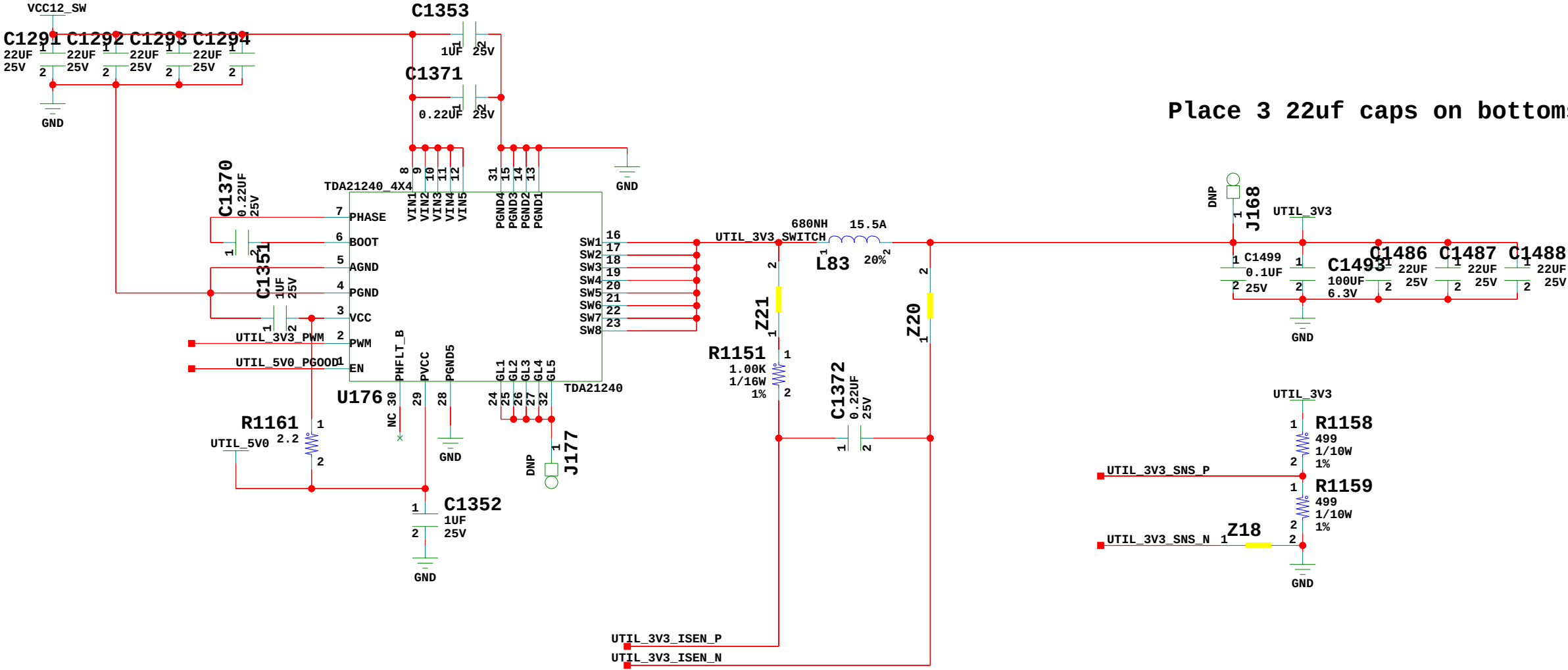
PMIC 2



TITLE: PMIC 2
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

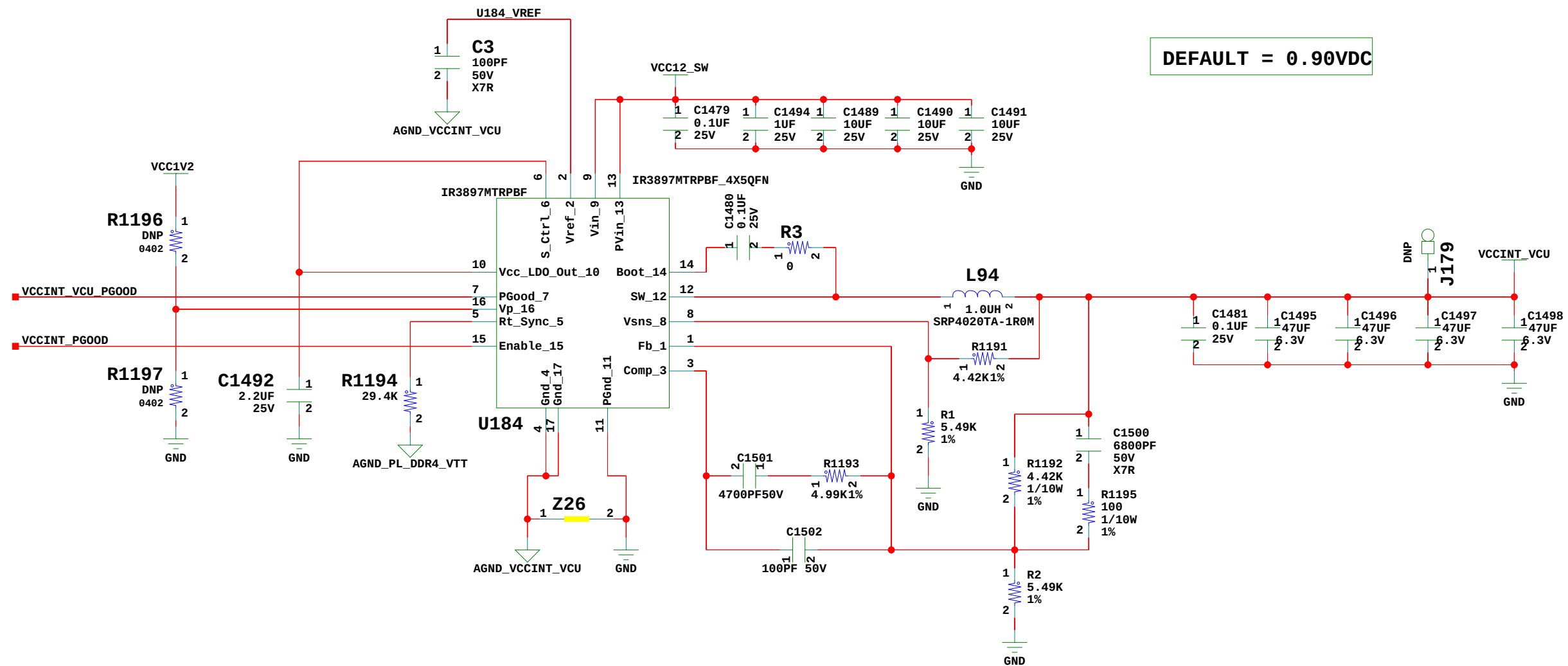
ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 49 OF 58	DRAWN BY: BF



PMIC 2 Power Stage

TITLE: PMIC 2 Power Stage SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:17		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	50	OF	58
DRAWN BY:		BF	



These VALUES need to change for 0.9V
and voltage sense line needs to be identified

DN update 8-11-17 per Rick L
VCCINT_VCU 3A Regulator



TITLE: VCCINT_VCU 3A Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:17

VER: 1.0

SHEET SIZE: B

REV: 01

SHEET

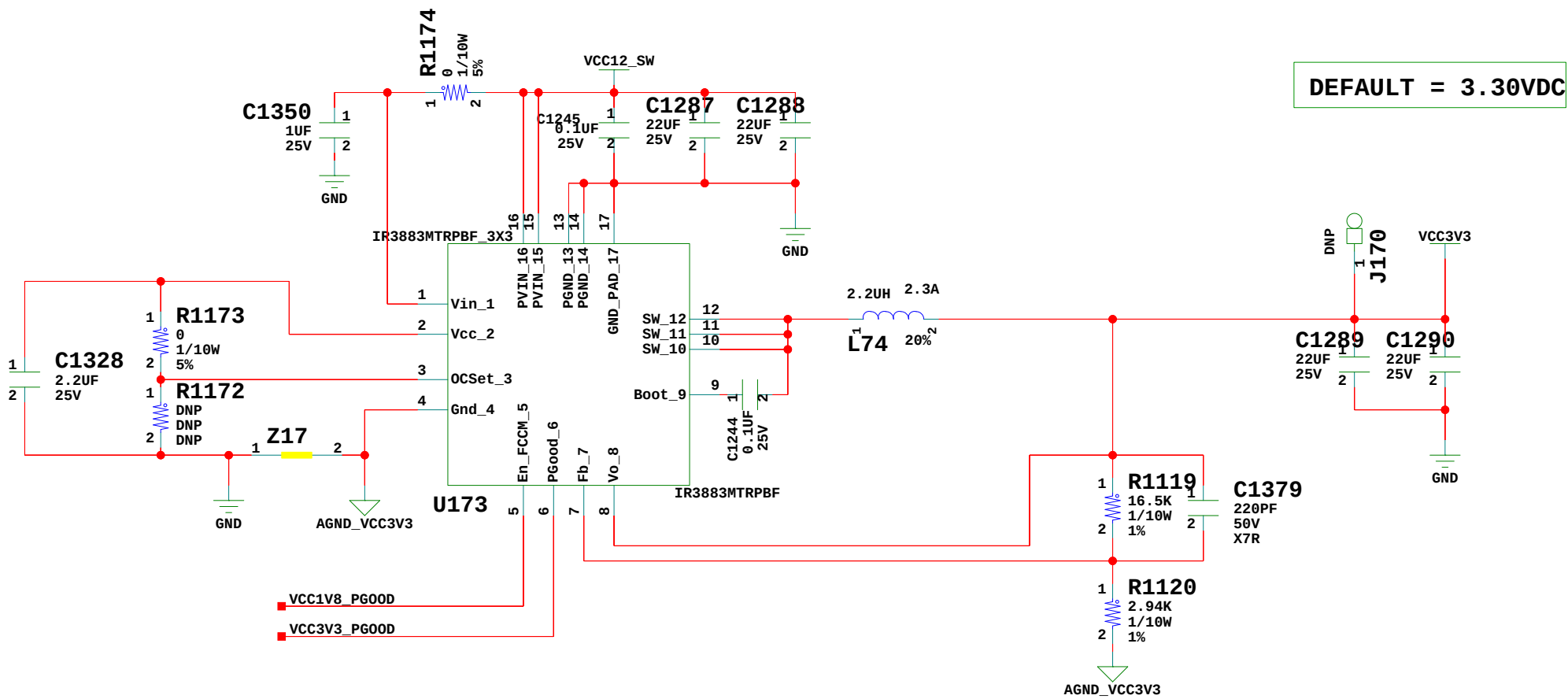
51

OF

58

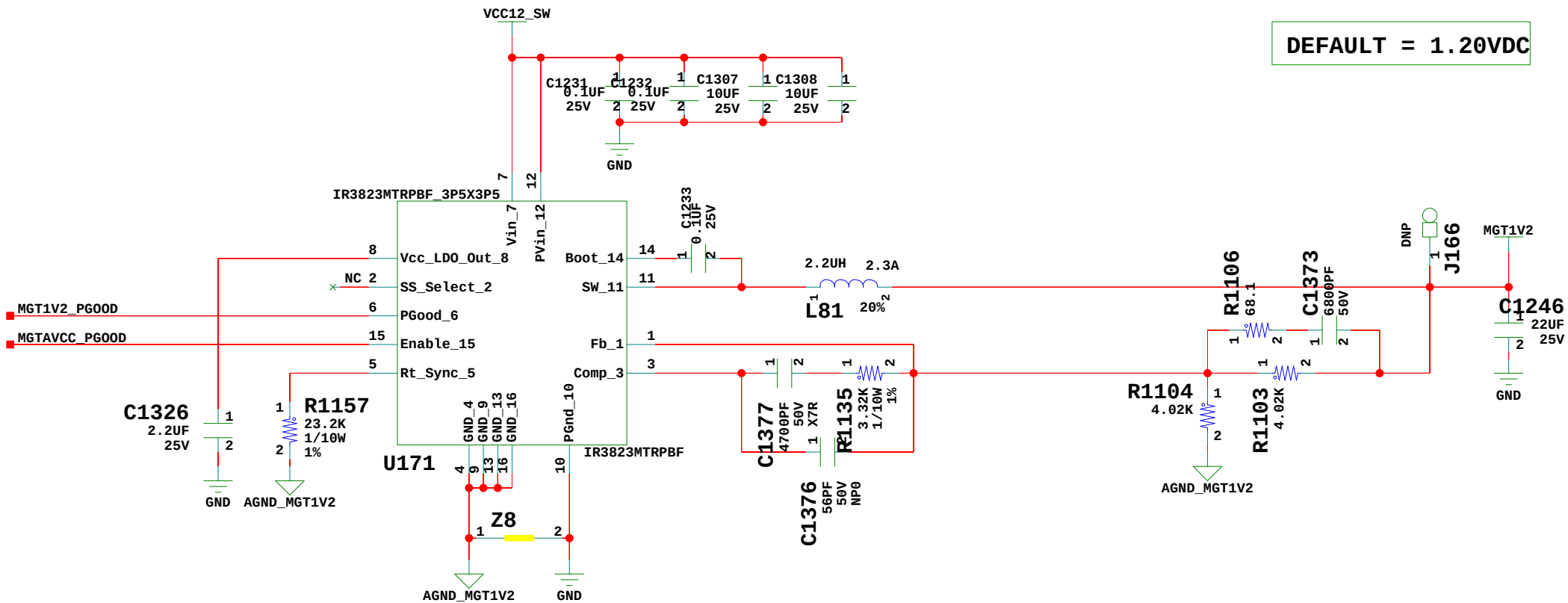
DRAWN BY:

BF



VCC3V3 500mA Regulator

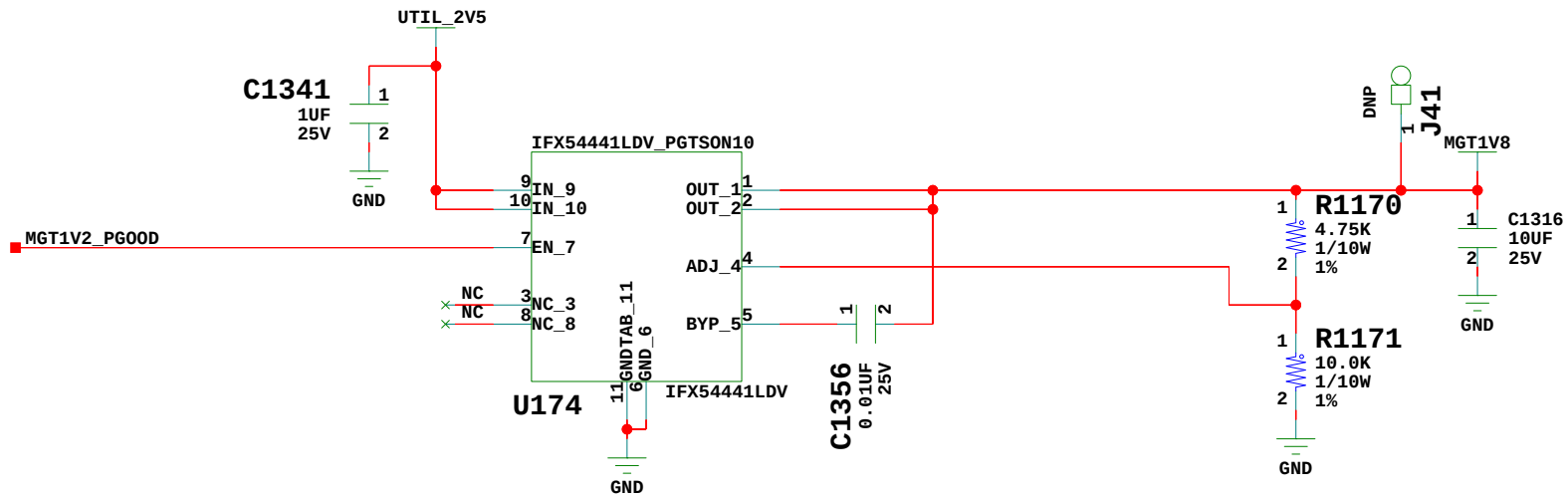
TITLE: VCC3V3 500mA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0	
ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:17	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 52 OF 58	DRAWN BY: BF



MGT1V2 1A Regulator

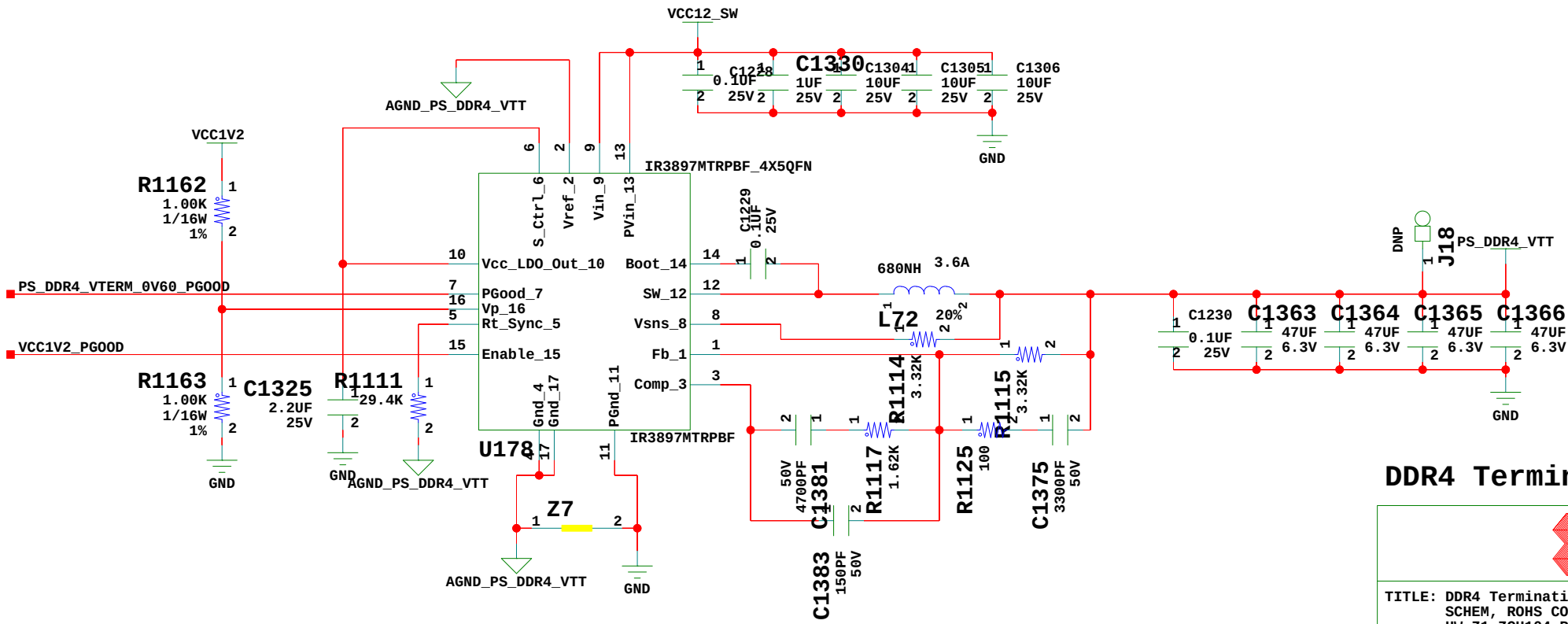
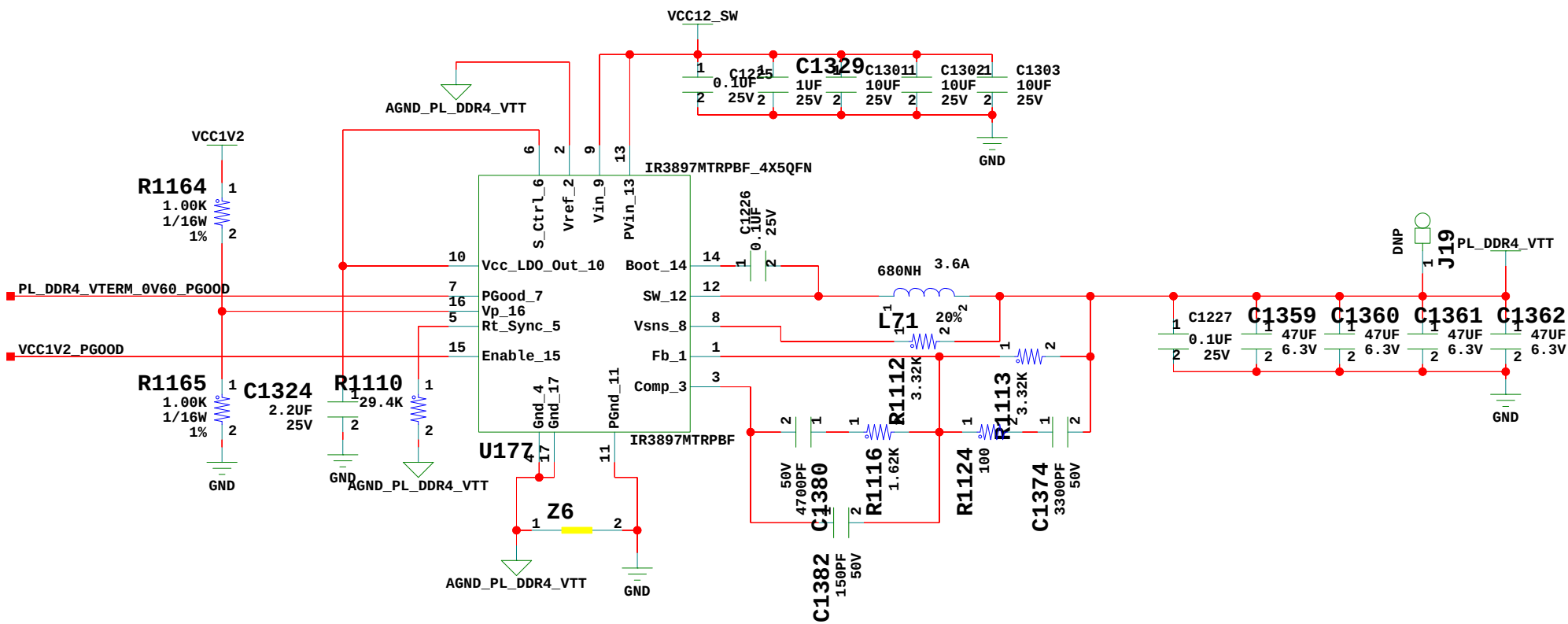
TITLE: MGT1V2 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	53	OF	58
DRAWN BY:		BF	

DEFAULT = 1.81VDC



MGT1V8 100mA Regulator

			
TITLE: MGT1V8 100mA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET	54	OF	58
DRAWN BY:		BF	



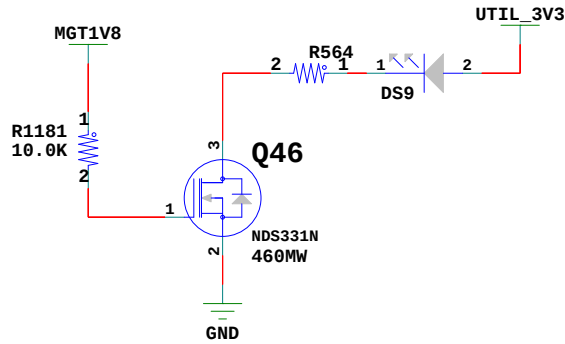
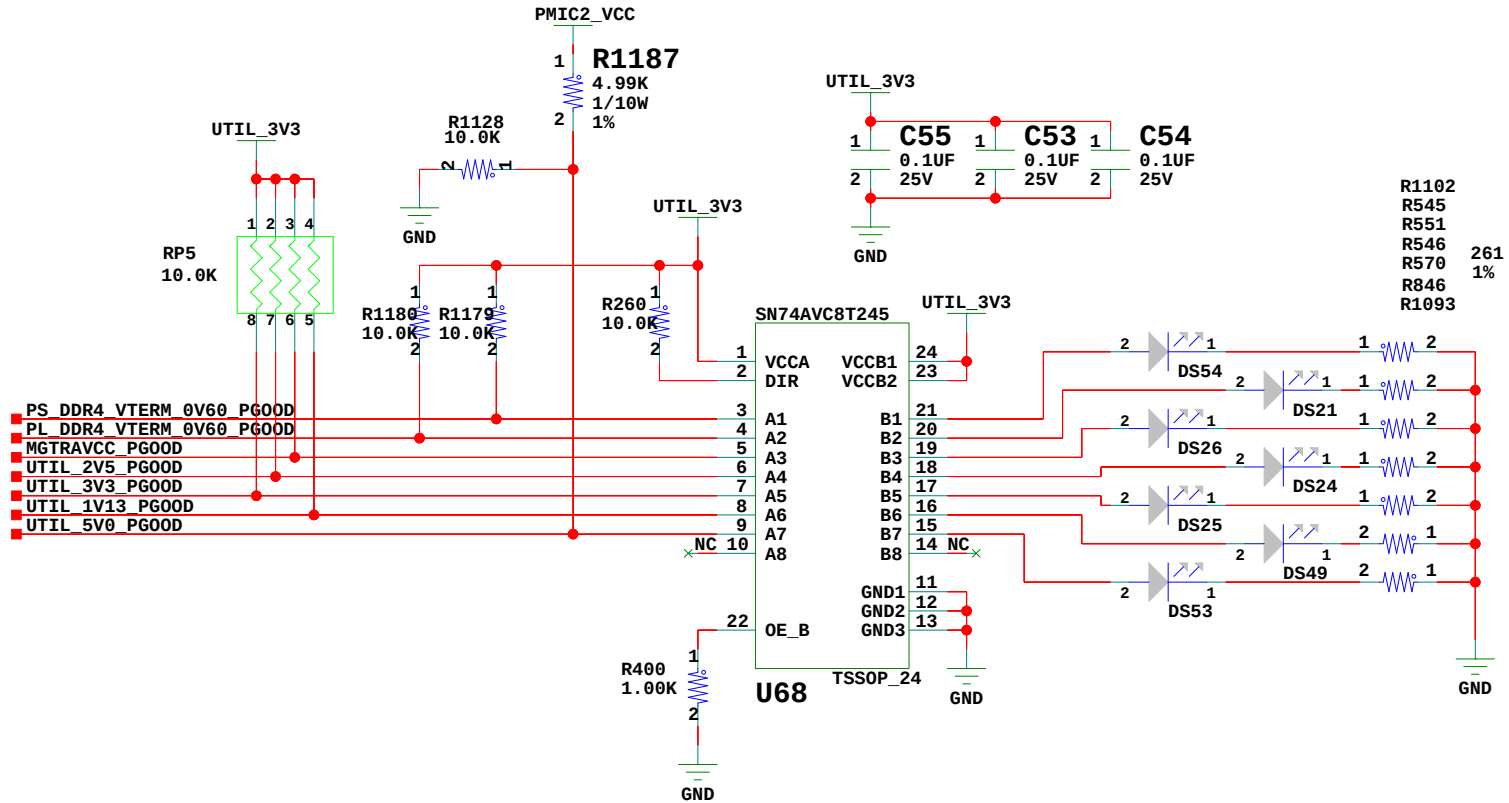
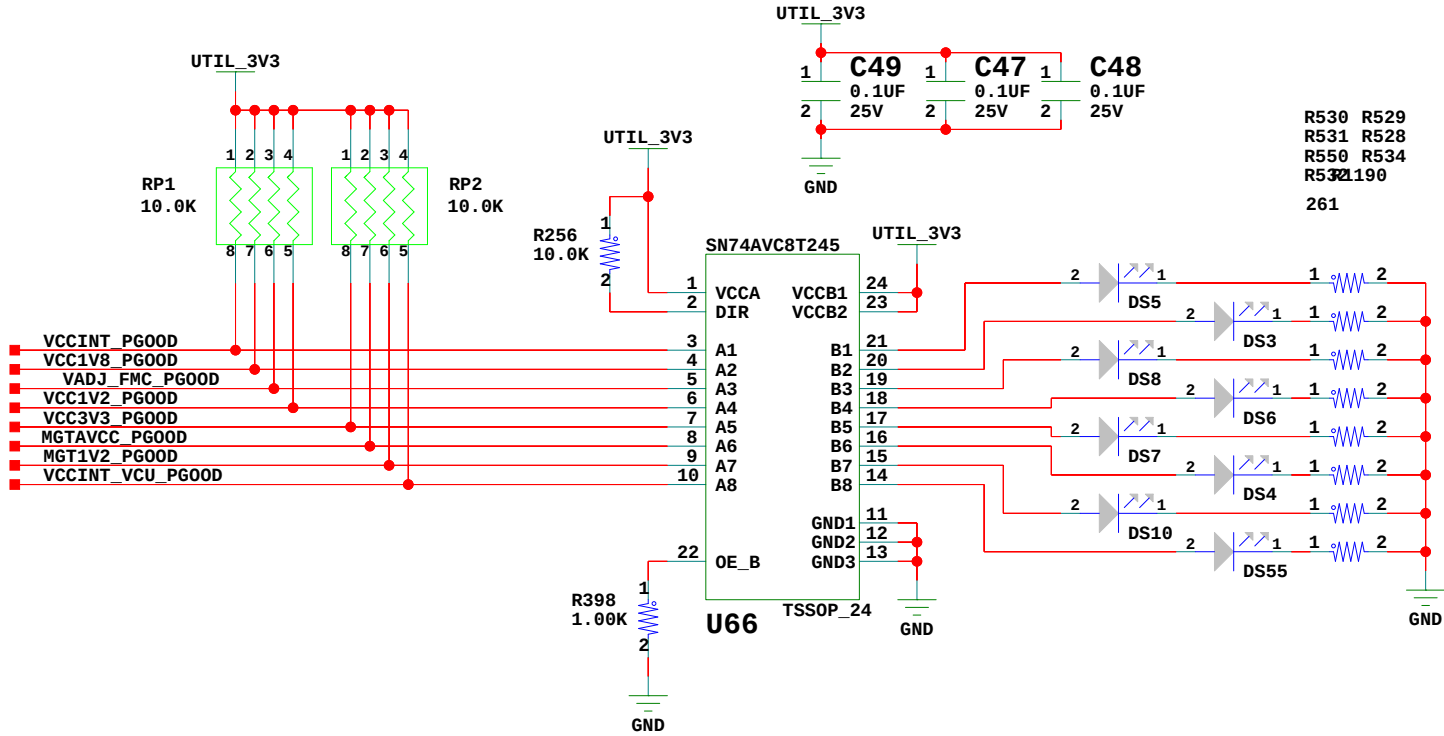
DDR4 Termination Supplies



TITLE: DDR4 Termination Supplies
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0

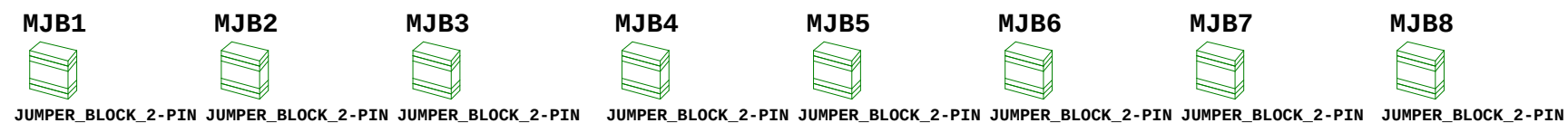
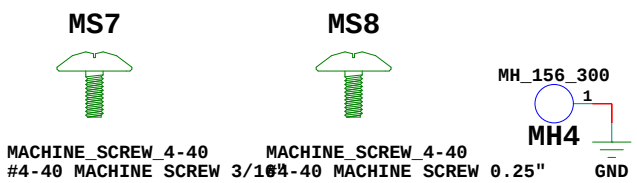
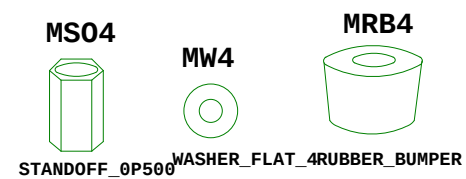
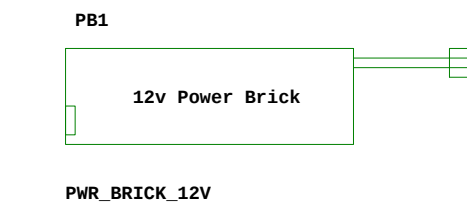
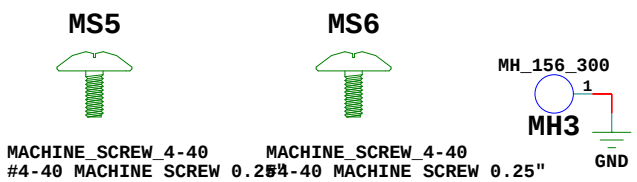
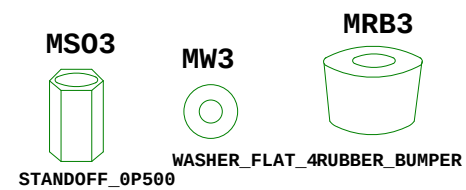
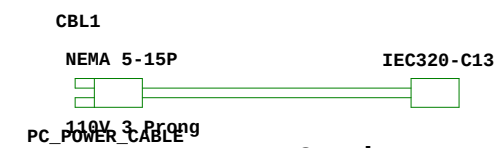
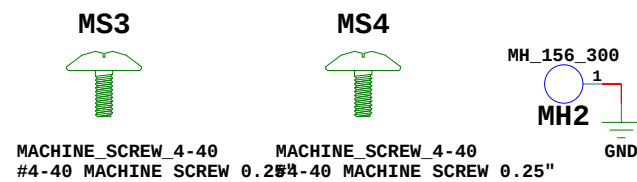
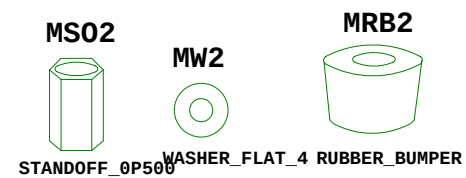
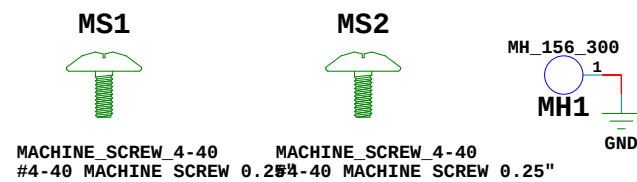
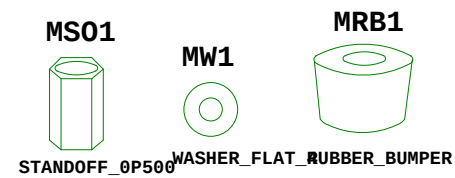
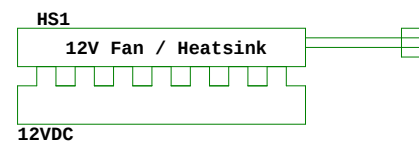
ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:21	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 56 OF 58	DRAWN BY: BF



Power Status LEDs

			
TITLE: Power Status LEDs SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16		VER:	1.0
SHEET SIZE: B		REV:	01
SHEET 57 OF 58		DRAWN BY: BF	



Mechanical Components



**TITLE: Mechanical Components
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU104_REV1_0**

ASSY P/N: 0432057
PCB P/N: 1280961
SCH P/N: 0381794
TEST P/N: TSS0189

DATE: 01/26/2018:14:16

VER:	1.0
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SHEET SIZE: B

REV:	01
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SHEET **58** OF **58**

DRAWN BY:

BF